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RTL8211F(D)(I)
RTL8211FS(I)(-VS)
RTL8211FG(I)(-VS)

INTEGRATED 10/100/1000M ETHERNET TRANSCEIVER

WAKE-ON-LAN (WOL) APPLICATION NOTE

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2014/04/02	First release.
1.1	2014/04/12	Corrected minor typing error.
1.2	2015/04/22	Corrected minor typing errors. Refined the WOL Reset and Maximum Packet Bytes Register description, page 5.
1.3	2017/12/22	Added section 5.2 Masked Bytes, page 13.

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1. Introduction

The RTL8211F series can monitor the network for a link change event, a Wake-Up Frame, or a Magic Packet, and notify the system via the INTB/PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The INTB/PMEB pin needs to be connected with a 4.7k ohm resistor and pulled up to 3.3V. When the Wake-Up Frame or a Magic Packet is sent to the PHY, the INTB/PMEB pin will be set low to notify the system to wake up. This pin with PMEB mode configured (refer to the 'Usage of INTB/PMEB Pin' section in the datasheets of the RTL8211F Series) can accept Active Low Wake-Up waveform format, or Pulse Low Wake-Up waveform format (details in section 6, page 20).

A Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the PHY, e.g., a broadcast, multicast, or unicast packet addressed to the PHY.
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches, i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the PHY, e.g., a broadcast, multicast, or unicast address to the current RTL8211F.
- The received Wake-Up Frame does not contain a CRC error.
- The 16-bit CRC* of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Otherwise, the PHY is configured to allow direct packet wake up, e.g., a broadcast, multicast, or unicast network packet, and even a non-specific packet is also supported.

**Note: 16-bit CRC: The RTL8211F supports up to eight long Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC-16 polynomial = $x^{16} + x^{12} + x^5 + 1$.*

2. Wake-On-LAN (WOL) Flow Chart

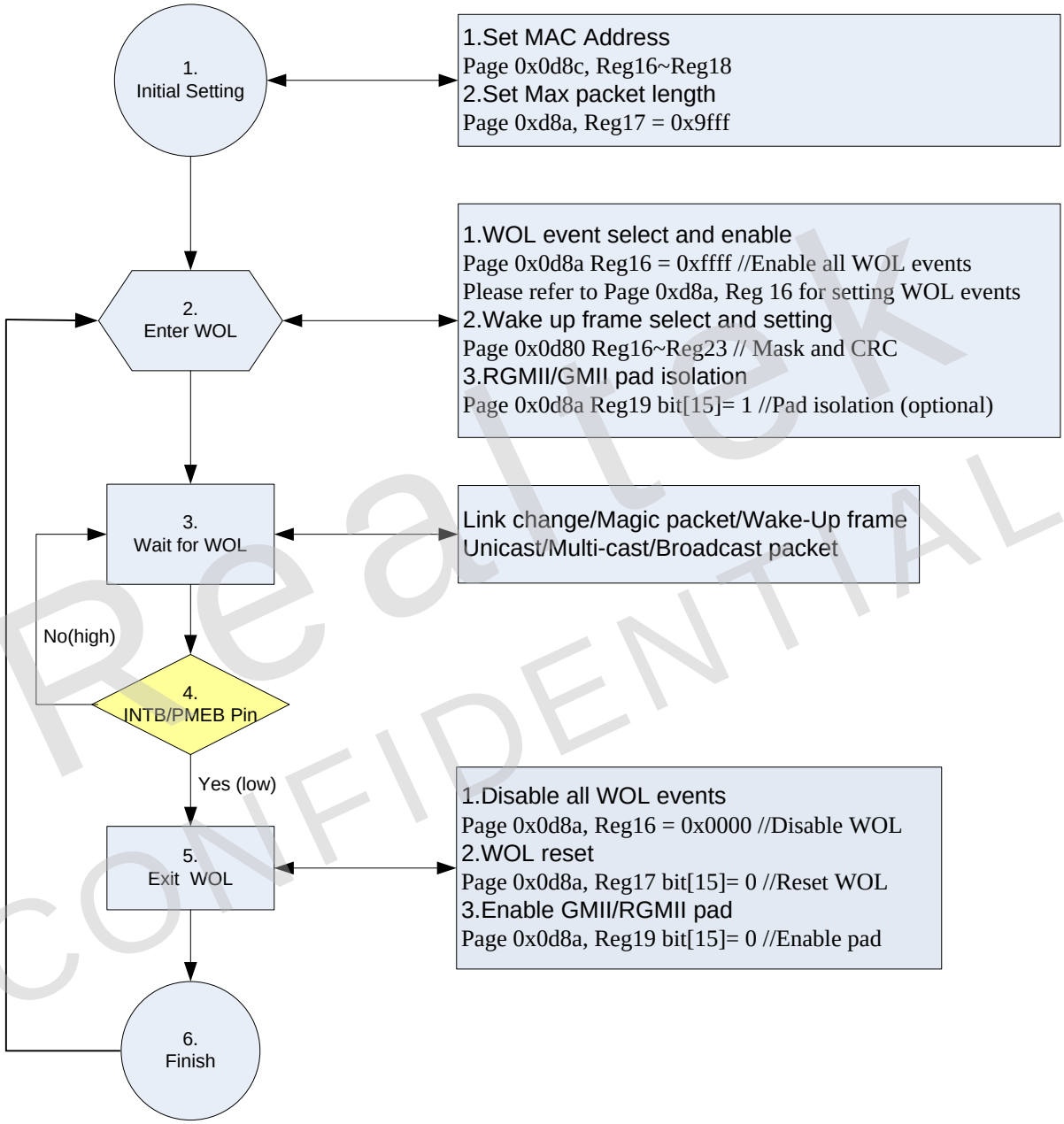


Figure 1. Wake-On-LAN (WOL) Flow Chart

3. Wake-On-LAN Register Setting (Page 0xd8a)

Enable WOL Link Change Event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0x2000 //enable Link Change Event

Enable WOL Magic Packet Event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0x1000 //enable Magic Packet Event

Enable WOL Arbitrary Packet Event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0x0800 //enable Arbitrary (non-specified) Packet Event

Enable WOL Unicast Event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0x0400 //enable Unicast Event

Enable WOL Multicast Event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0x0200 //enable Multicast Event

Enable WOL Broadcast Event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0x0100 //enable Broadcast

Enable WOL Wake-Up Frame Event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0x0001 //enable Wake-Up Frame 0 Event

Write Register 16, Data = 0x0002 //enable Wake-Up Frame 1 Event

Write Register 16, Data = 0x0004 //enable Wake-Up Frame 2 Event

Write Register 16, Data = 0x0008 //enable Wake-Up Frame 3 Event

Write Register 16, Data = 0x0010 //enable Wake-Up Frame 4 Event

Write Register 16, Data = 0x0020 //enable Wake-Up Frame 5 Event

Write Register 16, Data = 0x0040 //enable Wake-Up Frame 6 Event

Write Register 16, Data = 0x0080 //enable Wake-Up Frame 7 Event

Enable All WOL Events

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 16, Data = 0xffff //enable all Wake-On-LAN Events

Table 1. Page 109, Register 16

Bit	Name	Type	Description	Default Value
15:14	RSVD	RO	Reserved	00
13	linkchg_wol_en	RW	PMEB asserted due to detection of a change in the network link state	0
12	magic_en	RW	PMEB asserted due to receiving a magic packet	0
11	awf_en	RW	PMEB asserted due to receiving an arbitrary (non-specified) network packet (MAC destination address is don't-care)	0
10	uwf_en	RW	PMEB asserted due to receiving a network unicast packet that was sent to a local device (MAC destination address should be matched)	0
9	mwf_en	RW	PMEB asserted due to receiving a network multicast packet that was sent to a local device	0
8	bwf_en	RW	PMEB asserted due to receiving a network broadcast packet	0
7	enwakeup7	RW	PMEB asserted due to receiving a network wake-up frame #7	0
6	enwakeup6	RW	PMEB asserted due to receiving a network wake-up frame #6	0
5	enwakeup5	RW	PMEB asserted due to receiving a network wake-up frame #5	0
4	enwakeup4	RW	PMEB asserted due to receiving a network wake-up frame #4	0
3	enwakeup3	RW	PMEB asserted due to receiving a network wake-up frame #3	0
2	enwakeup2	RW	PMEB asserted due to receiving a network wake-up frame #2	0
1	enwakeup1	RW	PMEB asserted due to receiving a network wake-up frame #1	0
0	enwakeup0	RW	PMEB asserted due to receiving a network wake-up frame #0	0

WOL Reset and Maximum Packet Bytes Register (Page 0xd8a)

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 17, Data = 0x1fff //reset the WOL events and set maximum receive packet length

Note 1: The INTB/PMEB pin goes low when a WOL event occurs.
In PMEB mode, write Page 0xd8a, Register 17, Data = 0x1fff to reset the WOL status and set the INTB/PMEB pin back to default status); while in INTB mode, except for setting Page 0xd8a, Register 17, the interrupt status register (INSR) in Page 0xa43, Register 29 should also be read in order to reset the INTB/PMEB pin state. See the 'Interrupt' section in the RTL8211F series datasheet for more information.

Note 2: All the other registers will NOT be affected when a WOL reset is enabled. Instead, a power-on reset or hardware reset (PHYRSTB pin = low) will reset all registers back to original values.

Table 2. Page 0xd8a, Register 17

Bit	Name	Type	Description	Default Value
15	rg_rstb	W	Reset Wake-On-LAN by Register. Active low.	1
14:0	Rmsq	RW	Define the Maximum Received Packet Bytes.	0x1fff

4. Unique Physical Address & Multicast Register (Page 0xd8c, Registers 16~22)

The RTL8211F series support unicast and multicast events. For unicast applications it needs to write the MAC address to PHY register 16~18 (page 0xd8c).

Refer to Figure 3, page 7 and Table 3, page 8 for multicast application.

//Unicast Example: Set MAC Address=00:12:34:56:78:9a

Write Register 31, Data = 0x0d8c //select page 0xd8c

Write Register 16, Data = 0x1200

Write Register 17, Data = 0x5634

Write Register 18, Data = 0x9a78

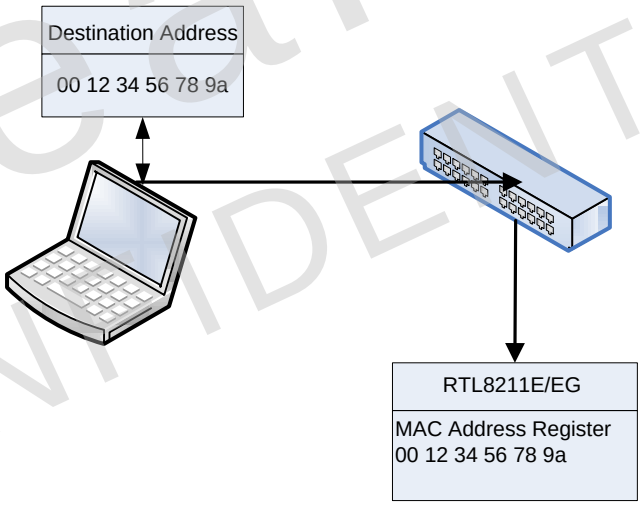


Figure 2. Unicast Application

//Multicast Example: Set Multicast Register=01:00:00:00:00:00:00:00

(Destination address is 01, 02, 3C, 00, 00, 00)

Write Register 31, Data = 0x0d8c //select page 0xd8c

Write Register 19, Data=0x0000

Write Register 20, Data=0x0000

Write Register 21, Data=0x0000

Write Register 22, Data=0x0100

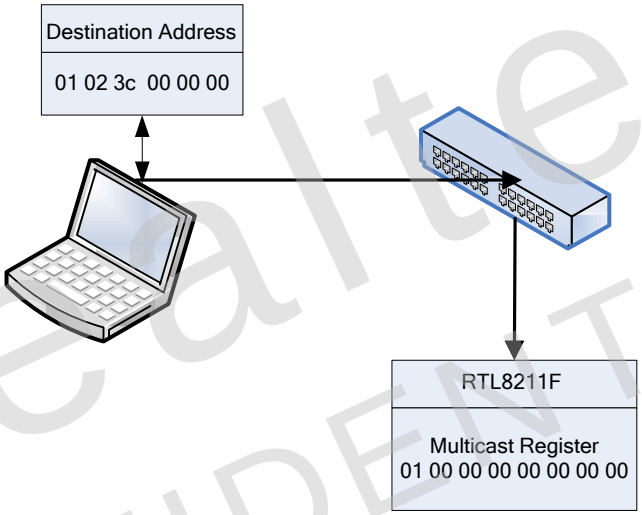


Figure 3. Multicast Application

Table 3. Multicast Pattern and Register

No.	Multicast Pattern	Multicast Register
0	01, 02, 3C, 00, 00, 00	01, 00, 00, 00, 00, 00, 00, 00
1	01, 02, 07, 00, 00, 00	02, 00, 00, 00, 00, 00, 00, 00
2	01, 02, 1F, 00, 00, 00	04, 00, 00, 00, 00, 00, 00, 00
3	01, 02, 24, 00, 00, 00	08, 00, 00, 00, 00, 00, 00, 00
4	01, 02, 28, 00, 00, 00	10, 00, 00, 00, 00, 00, 00, 00
5	01, 02, 13, 00, 00, 00	20, 00, 00, 00, 00, 00, 00, 00
6	01, 02, 0B, 00, 00, 00	40, 00, 00, 00, 00, 00, 00, 00
7	01, 02, 30, 00, 00, 00	80, 00, 00, 00, 00, 00, 00, 00
8	01, 02, 0D, 00, 00, 00	00, 01, 00, 00, 00, 00, 00, 00
9	01, 02, 36, 00, 00, 00	00, 02, 00, 00, 00, 00, 00, 00
10	01, 02, 2E, 00, 00, 00	00, 04, 00, 00, 00, 00, 00, 00
11	01, 02, 15, 00, 00, 00	00, 08, 00, 00, 00, 00, 00, 00
12	01, 02, 19, 00, 00, 00	00, 10, 00, 00, 00, 00, 00, 00
13	01, 02, 22, 00, 00, 00	00, 20, 00, 00, 00, 00, 00, 00
14	01, 02, 3A, 00, 00, 00	00, 40, 00, 00, 00, 00, 00, 00
15	01, 02, 01, 00, 00, 00	00, 80, 00, 00, 00, 00, 00, 00
16	01, 02, 21, 00, 00, 00	00, 00, 01, 00, 00, 00, 00, 00
17	01, 02, 1A, 00, 00, 00	00, 00, 02, 00, 00, 00, 00, 00
18	01, 02, 02, 00, 00, 00	00, 00, 04, 00, 00, 00, 00, 00
19	01, 02, 39, 00, 00, 00	00, 00, 08, 00, 00, 00, 00, 00
20	01, 02, 35, 00, 00, 00	00, 00, 10, 00, 00, 00, 00, 00
21	01, 02, 0E, 00, 00, 00	00, 00, 20, 00, 00, 00, 00, 00
22	01, 02, 16, 00, 00, 00	00, 00, 40, 00, 00, 00, 00, 00
23	01, 02, 2D, 00, 00, 00	00, 00, 80, 00, 00, 00, 00, 00
24	01, 02, 10, 00, 00, 00	00, 00, 00, 01, 00, 00, 00, 00
25	01, 02, 2B, 00, 00, 00	00, 00, 00, 02, 00, 00, 00, 00
26	01, 02, 33, 00, 00, 00	00, 00, 00, 04, 00, 00, 00, 00
27	01, 02, 08, 00, 00, 00	00, 00, 00, 08, 00, 00, 00, 00
28	01, 02, 04, 00, 00, 00	00, 00, 00, 10, 00, 00, 00, 00

No.	Multicast Pattern	Multicast Register
29	01, 02, 3F, 00, 00, 00	00, 00, 00, 20, 00, 00, 00, 00
30	01, 02, 27, 00, 00, 00	00, 00, 00, 40, 00, 00, 00, 00
31	01, 02, 1C, 00, 00, 00	00, 00, 00, 80, 00, 00, 00, 00
32	01, 02, 37, 00, 00, 00	00, 00, 00, 00, 01, 00, 00, 00
33	01, 02, 0C, 00, 00, 00	00, 00, 00, 00, 02, 00, 00, 00
34	01, 02, 14, 00, 00, 00	00, 00, 00, 00, 04, 00, 00, 00
35	01, 02, 2F, 00, 00, 00	00, 00, 00, 00, 08, 00, 00, 00
36	01, 02, 23, 00, 00, 00	00, 00, 00, 00, 10, 00, 00, 00
37	01, 02, 18, 00, 00, 00	00, 00, 00, 00, 20, 00, 00, 00
38	01, 02, 00, 00, 00, 00	00, 00, 00, 00, 40, 00, 00, 00
39	01, 02, 3B, 00, 00, 00	00, 00, 00, 00, 80, 00, 00, 00
40	01, 02, 06, 00, 00, 00	00, 00, 00, 00, 00, 01, 00, 00
41	01, 02, 3D, 00, 00, 00	00, 00, 00, 00, 00, 02, 00, 00
42	01, 02, 25, 00, 00, 00	00, 00, 00, 00, 00, 04, 00, 00
43	01, 02, 1E, 00, 00, 00	00, 00, 00, 00, 00, 08, 00, 00
44	01, 02, 12, 00, 00, 00	00, 00, 00, 00, 00, 10, 00, 00
45	01, 02, 29, 00, 00, 00	00, 00, 00, 00, 00, 20, 00, 00
46	01, 02, 31, 00, 00, 00	00, 00, 00, 00, 00, 40, 00, 00
47	01, 02, 0A, 00, 00, 00	00, 00, 00, 00, 00, 80, 00, 00
48	01, 02, 2A, 00, 00, 00	00, 00, 00, 00, 00, 00, 01, 00
49	01, 02, 11, 00, 00, 00	00, 00, 00, 00, 00, 00, 02, 00
50	01, 02, 09, 00, 00, 00	00, 00, 00, 00, 00, 00, 04, 00
51	01, 02, 32, 00, 00, 00	00, 00, 00, 00, 00, 00, 08, 00
52	01, 02, 3E, 00, 00, 00	00, 00, 00, 00, 00, 00, 10, 00
53	01, 02, 05, 00, 00, 00	00, 00, 00, 00, 00, 00, 20, 00
54	01, 02, 1D, 00, 00, 00	00, 00, 00, 00, 00, 00, 40, 00
55	01, 02, 26, 00, 00, 00	00, 00, 00, 00, 00, 00, 80, 00
56	01, 02, 1B, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 01
57	01, 02, 20, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 02
58	01, 02, 38, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 04

No.	Multicast Pattern	Multicast Register
59	01, 02, 03, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 08
60	01, 02, 0F, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 10
61	01, 02, 34, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 20
62	01, 02, 2C, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 40
63	01, 02, 17, 00, 00, 00	00, 00, 00, 00, 00, 00, 00, 80

Note that Table 3 lists some examples to show the mapping of Multicast Patterns to Multicast Registers.

Here is the detailed flow of how to determine the Multicast Register from a specified Multicast Address:

1. Choose a multicast address

Example: 01, 02, 1F, 00, 00, 00 (take the No.2 in Table 3 for example)

2. Proceed with the CRC-32 calculation of the address

E.g., the result of the CRC-32 calculation is 0x082466AF

3. Extract MSBs from the result of CRC-32 calculation

A = bit [28:26]

B = bit [31:29]

Example: 0x082466*AF* → 0xAF = 10*101* *111*

So, A = bit [31:29] = $(111)_2$; B = bit [28:26] = $(101)_2$*

**Note: The endian difference between PHY and MAC is here.*

4. The combination of A and B represents which bit in the Multicast Register should be set to '1'

(i) The **A-th byte** of the Multicast Register (start from byte [0] from the right)

(ii) The **B-th bit** in the byte indicated by A (start from bit [0] from the left)

Example: A = $(111)_2$ represents the 7^{th} byte of the Multicast Register; B = $(101)_2$ represents the 5^{th} bit of this byte should be set to '1'

The Multicast Register would be: **04**, 00, 00, 00, 00, 00, 00, 00

(7^{th} byte)↓

0000 0**1**00 (the 5^{th} bit, starts from the left)

That is, while the multicast address is '01, 02, 1F, 00, 00, 00', then the WOL multicast event should be armed by the setting below:

Write Register 31, Data = 0x0d8c //select page 0xd8c

Write Register 19, Data=0x0000

Write Register 20, Data=0x0000

Write Register 21, Data=0x0000

Write Register 22, Data=0x0400

Table 4. Page 0xd8c Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	uni_phy_addr[15:0]	RW	Unique Physical Address (MAC Address)	0
17	15:0	uni_phy_addr[31:16]	RW	Unique Physical Address (MAC Address)	0
18	15:0	uni_phy_addr[47:32]	RW	Unique Physical Address (MAC Address)	0
19	15:0	multicast_register[15:0]	RW	Multicast Register	0
20	15:0	multicast_register[31:16]	RW	Multicast Register	0
21	15:0	multicast_register[47:32]	RW	Multicast Register	0
22	15:0	multicast_register[63:48]	RW	Multicast Register	0

5. Wake-Up Frame Mask & CRC Setting

Pages 0xd80~0xd87 are Wake-Up frame mask registers that support Wake-Up frame 0 to Wake-Up frame 7. The Wake-Up frame CRC registers are located in page 0xd88.

5.1. Set Wake-Up Frame Mask

Example: Set Wake-Up Frame Mask = 0x00 00 03 C0 00 20 30 00

Packet Data: (Red-dotted line is the MASK)

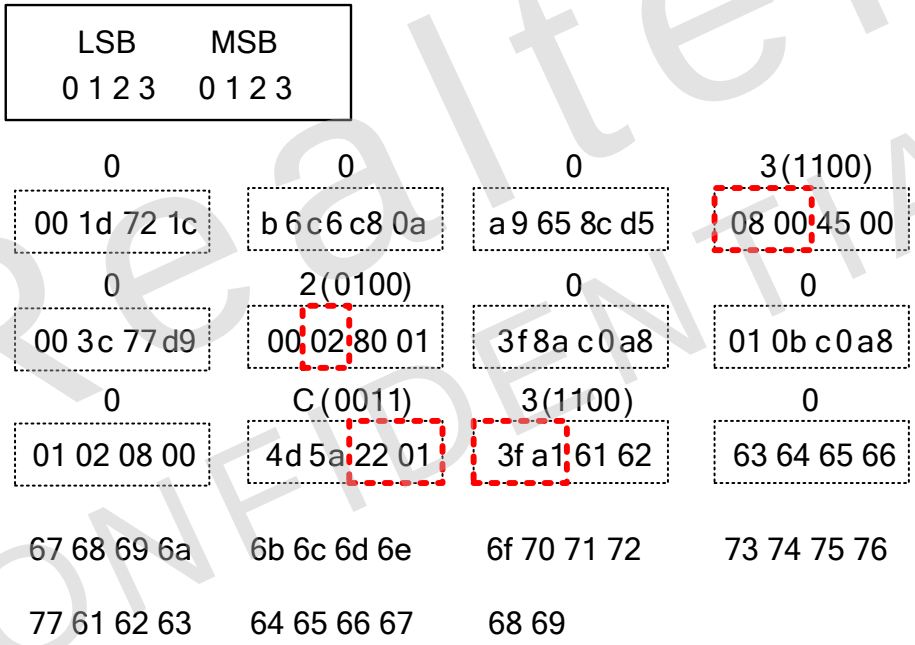


Figure 4. Set Wake-Up Frame Mask

5.2. Masked Bytes

0x08, 0x00, 0x02, 0x22, 0x01, 0x3f, 0xa1 are Masked Bytes.

Reflect the Masked Bytes for calculating the CRC:

0x08 (0000 1000) reflects to 0x10 (0001 0000)

0x00 (0000 0000) reflects to 0x00 (0000 0000)

0x02 (0000 0010) reflects to 0x40 (0100 0000)

0x22 (0010 0010) reflects to 0x44 (0100 0100)

0x01 (0000 0001) reflects to 0x80 (1000 0000)

0x3f (0011 1111) reflects to 0xfc (1111 1100)

0xa1 (1010 0001) reflects to 0x85 (1000 0101)

0x10, 0x00, 0x40, 0x44, 0x80, 0xfc, 0x85 are used to calculate the CRC, which will get 0xdf6b.

5.3. Write Register for Wake-Up Frame Mask

Write Register 31, Data = 0x0d80 //select page 0xd80 (Wake-Up frame mask 0)

Write Register 16, Data = 0x3000

Write Register 17, Data = 0x0020

Write Register 18, Data = 0x03c0

Write Register 19, Data = 0x0000

Write Register 20, Data = 0x0000

Write Register 21, Data = 0x0000

Write Register 22, Data= 0x0000

Write Register 23, Data = 0x0000

Table 5. Page 0xd80 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf0[15:0]	RW	Byte masks of wake-up frame #0 for power management	0
17	15:0	byte_msk_wf0[31:16]	RW	Byte masks of wake-up frame #0 for power management	0
18	15:0	byte_msk_wf0[47:32]	RW	Byte masks of wake-up frame #0 for power management	0
19	15:0	byte_msk_wf0[63:48]	RW	Byte masks of wake-up frame #0 for power management	0
20	15:0	byte_msk_wf0[79:64]	RW	Byte masks of wake-up frame #0 for power management	0
21	15:0	byte_msk_wf0[95:80]	RW	Byte masks of wake-up frame #0 for power management	0
22	15:0	byte_msk_wf0[111:96]	RW	Byte masks of wake-up frame #0 for power management	0
23	15:0	byte_msk_wf0[127:112]	RW	Byte masks of wake-up frame #0 for power management	0

Table 6. Page 0xd81 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf1[15:0]	RW	Byte masks of wake-up frame #1 for power management	0
17	15:0	byte_msk_wf1[31:16]	RW	Byte masks of wake-up frame #1 for power management	0
18	15:0	byte_msk_wf1[47:32]	RW	Byte masks of wake-up frame #1 for power management	0
19	15:0	byte_msk_wf1[63:48]	RW	Byte masks of wake-up frame #1 for power management	0
20	15:0	byte_msk_wf1[79:64]	RW	Byte masks of wake-up frame #1 for power management	0
21	15:0	byte_msk_wf1[95:80]	RW	Byte masks of wake-up frame #1 for power management	0
22	15:0	byte_msk_wf1[111:96]	RW	Byte masks of wake-up frame #1 for power management	0
23	15:0	byte_msk_wf1[127:112]	RW	Byte masks of wake-up frame #1 for power management	0

Table 7. Page 0xd82 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf2[15:0]	RW	Byte masks of wake-up frame #2 for power management	0
17	15:0	byte_msk_wf2[31:16]	RW	Byte masks of wake-up frame #2 for power management	0
18	15:0	byte_msk_wf2[47:32]	RW	Byte masks of wake-up frame #2 for power management	0
19	15:0	byte_msk_wf2[63:48]	RW	Byte masks of wake-up frame #2 for power management	0
20	15:0	byte_msk_wf2[79:64]	RW	Byte masks of wake-up frame #2 for power management	0
21	15:0	byte_msk_wf2[95:80]	RW	Byte masks of wake-up frame #2 for power management	0
22	15:0	byte_msk_wf2[111:96]	RW	Byte masks of wake-up frame #2 for power management	0
23	15:0	byte_msk_wf2[127:112]	RW	Byte masks of wake-up frame #2 for power management	0

Table 8. Page 0xd83 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf3[15:0]	RW	Byte masks of wake-up frame #3 for power management	0
17	15:0	byte_msk_wf3[31:16]	RW	Byte masks of wake-up frame #3 for power management	0
18	15:0	byte_msk_wf3[47:32]	RW	Byte masks of wake-up frame #3 for power management	0
19	15:0	byte_msk_wf3[63:48]	RW	Byte masks of wake-up frame #3 for power management	0
20	15:0	byte_msk_wf3[79:64]	RW	Byte masks of wake-up frame #3 for power management	0
21	15:0	byte_msk_wf3[95:80]	RW	Byte masks of wake-up frame #3 for power management	0
22	15:0	byte_msk_wf3[111:96]	RW	Byte masks of wake-up frame #3 for power management	0
23	15:0	byte_msk_wf3[127:112]	RW	Byte masks of wake-up frame #3 for power management	0

Table 9. Page 0xd84 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf4[15:0]	RW	Byte masks of wake-up frame #4 for power management	0
17	15:0	byte_msk_wf4[31:16]	RW	Byte masks of wake-up frame #4 for power management	0
18	15:0	byte_msk_wf4[47:32]	RW	Byte masks of wake-up frame #4 for power management	0
19	15:0	byte_msk_wf4[63:48]	RW	Byte masks of wake-up frame #4 for power management	0
20	15:0	byte_msk_wf4[79:64]	RW	Byte masks of wake-up frame #4 for power management	0
21	15:0	byte_msk_wf4[95:80]	RW	Byte masks of wake-up frame #4 for power management	0
22	15:0	byte_msk_wf4[111:96]	RW	Byte masks of wake-up frame #4 for power management	0
23	15:0	byte_msk_wf4[127:112]	RW	Byte masks of wake-up frame #4 for power management	0

Table 10. Page 0xd85 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf5[15:0]	RW	Byte masks of wake-up frame #5 for power management	0
17	15:0	byte_msk_wf5[31:16]	RW	Byte masks of wake-up frame #5 for power management	0
18	15:0	byte_msk_wf5[47:32]	RW	Byte masks of wake-up frame #5 for power management	0
19	15:0	byte_msk_wf5[63:48]	RW	Byte masks of wake-up frame #5 for power management	0
20	15:0	byte_msk_wf5[79:64]	RW	Byte masks of wake-up frame #5 for power management	0
21	15:0	byte_msk_wf5[95:80]	RW	Byte masks of wake-up frame #5 for power management	0
22	15:0	byte_msk_wf5[111:96]	RW	Byte masks of wake-up frame #5 for power management	0
23	15:0	byte_msk_wf5[127:112]	RW	Byte masks of wake-up frame #5 for power management	0

Table 11. Page 0xd86 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf6[15:0]	RW	Byte masks of wake-up frame #6 for power management	0
17	15:0	byte_msk_wf6[31:16]	RW	Byte masks of wake-up frame #6 for power management	0
18	15:0	byte_msk_wf6[47:32]	RW	Byte masks of wake-up frame #6 for power management	0
19	15:0	byte_msk_wf6[63:48]	RW	Byte masks of wake-up frame #6 for power management	0
20	15:0	byte_msk_wf6[79:64]	RW	Byte masks of wake-up frame #6 for power management	0
21	15:0	byte_msk_wf6[95:80]	RW	Byte masks of wake-up frame #6 for power management	0
22	15:0	byte_msk_wf6[111:96]	RW	Byte masks of wake-up frame #6 for power management	0
23	15:0	byte_msk_wf6[127:112]	RW	Byte masks of wake-up frame #6 for power management	0

Table 12. Page 0xd87 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	byte_msk_wf7[15:0]	RW	Byte masks of wake-up frame #7 for power management	0
17	15:0	byte_msk_wf7[31:16]	RW	Byte masks of wake-up frame #7 for power management	0
18	15:0	byte_msk_wf7[47:32]	RW	Byte masks of wake-up frame #7 for power management	0
19	15:0	byte_msk_wf7[63:48]	RW	Byte masks of wake-up frame #7 for power management	0
20	15:0	byte_msk_wf7[79:64]	RW	Byte masks of wake-up frame #7 for power management	0
21	15:0	byte_msk_wf7[95:80]	RW	Byte masks of wake-up frame #7 for power management	0
22	15:0	byte_msk_wf7[111:96]	RW	Byte masks of wake-up frame #7 for power management	0
23	15:0	byte_msk_wf7[127:112]	RW	Byte masks of wake-up frame #7 for power management	0

5.4. Set Wake-Up Frame CRC

Example: Set Wake-Up Frame CRC=0xdf6b

Write Register 31, Data = 0x0d88 //select extension page 108

Write Register 16, Data = 0xdf6b //set Wake-Up Frame #0 CRC=df6b

Table 13. Page 0xd88 Registers

Reg	Bit	Name	Type	Description	Default Value
16	15:0	wfcrc0	RW	16-bit CRC of wake-up frame #0	0
17	15:0	wfcrc1	RW	16-bit CRC of wake-up frame #1	0
18	15:0	wfcrc2	RW	16-bit CRC of wake-up frame #2	0
19	15:0	wfcrc3	RW	16-bit CRC of wake-up frame #3	0
20	15:0	wfcrc4	RW	16-bit CRC of wake-up frame #4	0
21	15:0	wfcrc5	RW	16-bit CRC of wake-up frame #5	0
22	15:0	wfcrc6	RW	16-bit CRC of wake-up frame #6	0
23	15:0	wfcrc7	RW	16-bit CRC of wake-up frame #7	0

5.5. Set Wake-Up Frame for WOL Example

1. Set maximum packet and WOL event

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 17, Data = 0x9fff //maximum packet length

Write Register 16, Data=0x0001 //Enable WOL Wake-Up frame 0 event

2. Set MAC address = 0x00:12:34:56:78:9a

Write Register 31, Data = 0x0d8c //select page 0xd8c

Write Register 16, Data = 0x1200

Write Register 17, Data = 0x5634

Write Register 18, Data = 0x9a78

3. Set wake-up frame mask; wake-up frame mask = 0x0000_03C0_0020_3000

Write Register 31, Data = 0x0d80 //select page 0xd80 (Wake-Up frame mask 0)

Write Register 16, Data = 0x3000

Write Register 17, Data = 0x0020

Write Register 18, Data = 0x03c0

Write Register 19, Data = 0x0000

Write Register 20, Data = 0x0000

Write Register 21, Data = 0x0000

Write Register 22, Data= 0x0000

Write Register 23, Data = 0x0000

4. Set wake-up frame CRC

Write Register 31, Data = 0x0d88 //select extension page 108

Write Register 16, Data = 0xdf6b //set Wake-Up Frame #0 CRC=df6b

5. Isolate the GMII/RGMII pads for power saving

Write Register 31, Data = 0x0d8a //select page 0xd8a

Write Register 25, bit[15], Data = 1

Write Register 31, Data=0x0000 //back to page 0

6. Pulse Low and Pad Isolation Register

6.1. Pulse Low Register

The INTB/PMEB pin of the RTL8211F series can support two waveform formats in RMEB mode* for WOL events. The default setting is ‘active low’. This can be changed to ‘pulse low’ via register. When using ‘pulse low’ the PMEB pin will return to ‘high’ after a WOL low pulse event.

**Note: These two waveform formats are available only when the INTB/PMEB pin is configured to be PMEB mode (refer to the ‘Usage of INTB/PMEB Pin’ section in the datasheets of the RTL8211F Series); otherwise, it only provides the ‘active low’ waveform.*

In PMEB mode, whether pulse low or active low format is used, it needs to reset the WOL status for the next WOL event (write Page 0xd8a, Register 17, bit[15] = 0 to reset the PMEB pin back to default status).

Table 14. Page 0xd8a, Register 19, bit[2:0]

Reg	Bit	Name	Type	Description	Default Value
19	2:1	pulse_width	RW	Pulse Width of PMEB Pin 00: 84ms 01: 168ms (Default) 10: 336ms 11: 672ms Pulse width variation <5%	01
	0	en_lowpulse	RW	Enable ‘Pulse Low’ waveform format	0

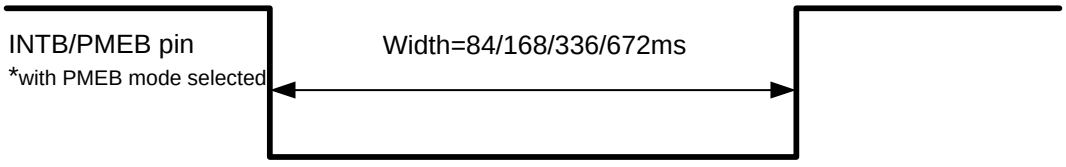


Figure 5. Pulse Low Waveform

6.2. GMII/RGMII Pad Isolation Timing

The RTL8211F series support the pad isolation feature for power saving and isolation between the PHY and MAC in WOL mode. The GMII/RGMII pins will be output low when the pad disable function is enabled.

Table 15. Page 0xd8a, Register 19, bit[15:12]

Reg	Bit	Name	Type	Description	Default Value
19	15	wol_pad_iso_en	RW	GMII/RGMII Pad Isolation (Output Low for WOL)	0
	14	wol_txc_iso_en	RW	TXC Isolation (MII mode) for when bit[15] = 1. TXC will stop outputting.	0
	13	wol_rxc_iso_en	RW	RXC Isolation when bit[15] = 1. RXC will stop outputting.	0
	12	wol_iso_send_lpi_en	RW	During Pad Isolation, the GMII/RGMII pad will continue sending LPI code words in order to make the link partner enter EEE state for power saving.	0

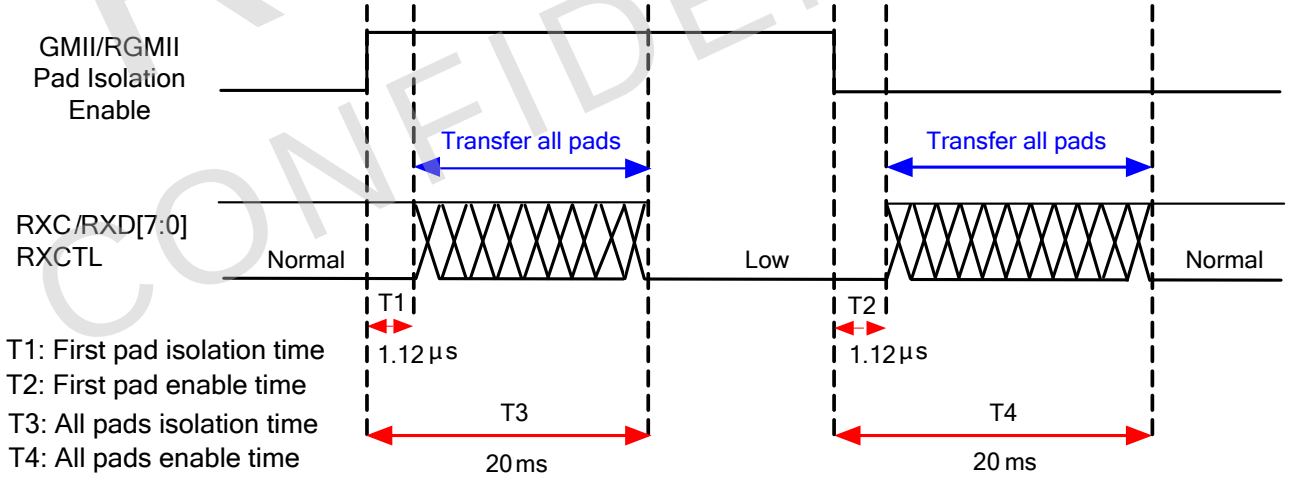


Figure 6. GMII/RGMII Pad Isolation Timing

7. Wake-On-LAN (WOL) Circuit and Timing

7.1. Wake-On-LAN (WOL) Circuit

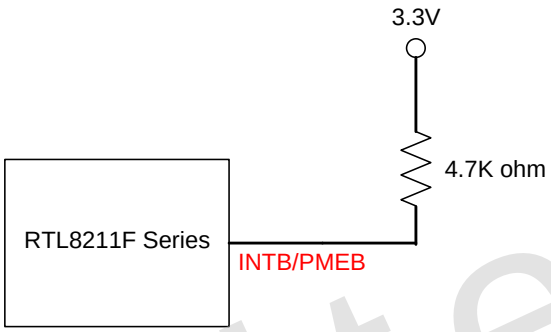


Figure 7. Wake-On-LAN (WOL) Circuit

The RTL8211F series does not support 3.3/2.5/1.8/1.5V GMII/RGMII power off in normal operation mode when using an external power source for the GMII/RGMII power. If using an external power for GMII/RGMII, the power should be maintained when in the WOL state.

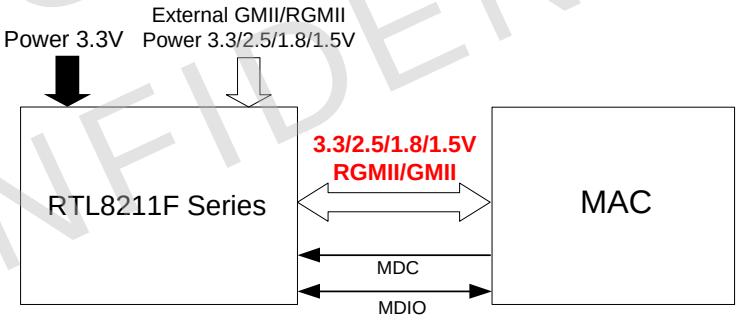
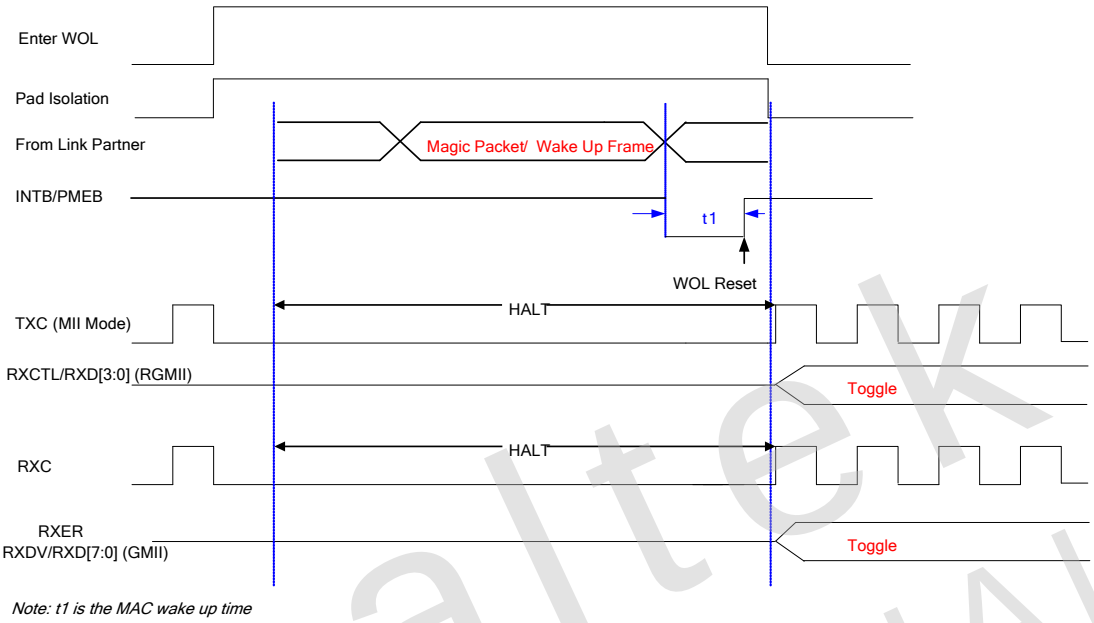


Figure 8. GMII/RGMII WOL Application with External Power Source

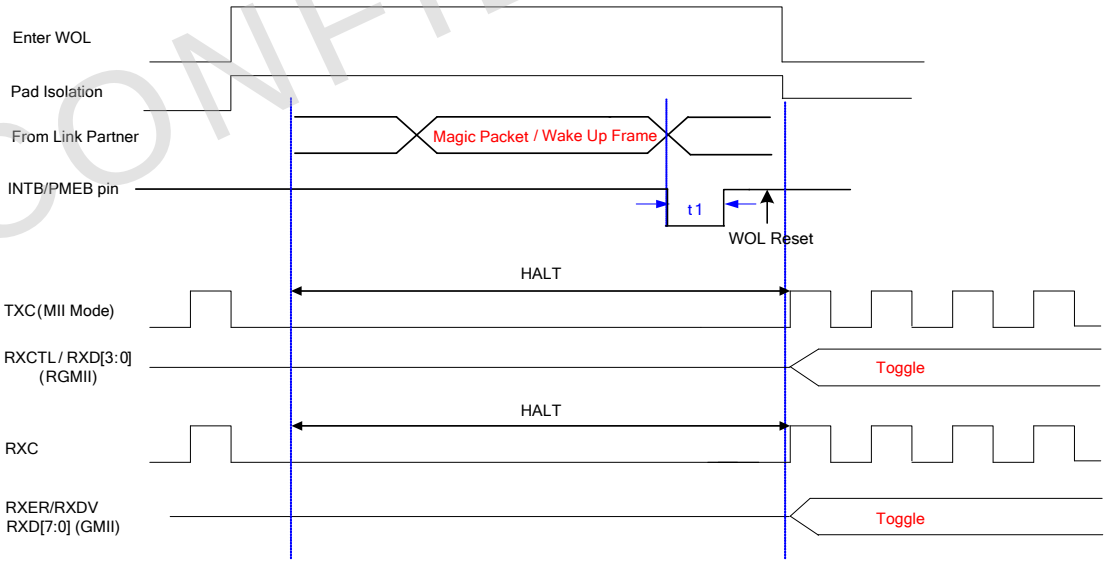
7.2. Wake-On-LAN (WOL) Active Low Timing



Note: t1 is the MAC wake up time

Figure 9. Wake-On-LAN (WOL) Active Low Timing

7.3. Wake-On-LAN Pulse Low Timing (PMEB Mode Only)



Note: Note: t1 width is controlled by Page 0xd8a, Register 19, bit[2:1].

Figure 10. Wake-On-LAN (WOL) Pulse Low Timing

8. Wake-On-LAN (WOL) Pin Types

I: Input

O: Output

L: Low

LI: Latched Input during Power up or Reset

PU Internal Pull up during power on reset

PD: Internal Pull down during power on reset

8.1. RGMII Interface (RTL8211F(I)/RTL8211FD(I))

Table 16. RGMII Pins Type (RTL8211F(I)/RTL8211FD(I))

Name	Type	Normal			Status in Pad Isolation
		1000M	100M	10M	
RXC	O/LI/PD	125M CLK Output	25M CLK Output	2.5M CLK Output	L*
RXD0	O/LI/PU	O	O	O	L
RXD1	O/LI/PD	O	O	O	L
RXD2	O/LI/PD	O	O	O	L
RXD3	O/LI/PU	O	O	O	L
RXCTL	O/LI/PD	O	O	O	L

**Note 1: With wol_rxc_iso_en = 1.*

Note 2: If the user sets wol_pad_iso_en =1and wol_rxc_iso_en = 1, then all of RXC/RXD[3:0]/RXCTL pins type are 'Low'.

8.2. RGMII Interface (RTL8211FS(I)/RTL8211FS(I)-VS)

Table 17. RGMII Pins Type (RTL8211FS(I)/RTL8211FS(I)-VS)

Name	Type	Normal			Status in Pad Isolation
		1000M	100M	10M	
RXC	O/LI/PD	125M CLK Output	25M CLK Output	2.5M CLK Output	L*
RXD0	O/LI/PU	O	O	O	L
RXD1	O/LI/PD	O	O	O	L
RXD2	O/LI/PD	O	O	O	L
RXD3	O/LI/PU	O	O	O	L
RXCTL	O/LI/PD	O	O	O	L

**Note 1: With wol_rxc_iso_en = 1.*

Note 2: If the user sets wol_pad_iso_en =1and wol_rxc_iso_en = 1, then all of RXC/RXD[3:0]/RXCTL pins type are 'Low'.

8.3. GMII Interface (RTL8211FG(I) / RTL8211FG(I)-VS)

Table 18. GMII Pins Type (RTL8211FG(I) / RTL8211FG(I)-VS)

Name	Type	Normal			Status in Pad Disable
		1000M	100M	10M	
RXC	O/LI/PD	125M CLK Output	25M CLK Output	2.5M CLK Output	L*
RXD0	O/LI/PU	O	O	O	L
RXD1	O/LI/PD	O	O	O	L
RXD2	O	O	O	O	L
RXD3	O	O	O	O	L
RXD4	O/LI/PD	O	O	O	L
RXD5	O/LI/PU	O	O	O	L
RXD6	O	O	O	O	L
RXD7	O	O	O	O	L
RXDV	O/LI/PD	O	O	O	L
RXER	O/LI/PU	O	O	O	L
TXC	O	O	25M CLK Output	2.5M CLK Output	L*
COL	O	O	O	O	O
CRS	O/PD	O	O	O	O

**Note 1: With wol_rxc_iso_en = 1 and wol_txc_iso_en = 1.*

Note 2: If the user sets wol_pad_iso_en =1, wol_rxc_iso_en = 1, and wol_rxc_iso_en = 1, then all of RXC/TXC/RXD[7:0]/RXDV/RXER pins type are 'Low'.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211 Fax: +886-3-577-6047
www.realtek.com