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RTL8211D-VB, RTL8211DG-VB, RTL8211DN-VB
RTL8211E-VB, RTL8211E-VL, RTL8211EG-VB

INTEGRATED 10/100/1000M ETHERNET TRANSCEIVER

MII/(R)GMII BEHAVIOR IN EEE APPLICATION NOTE

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2010/04/28	First release.
1.1	2010/08/13	Major revisions to all sections.
1.2	2011/06/23	Separated original combined application note to 10/100M and 10/100/1000M versions. Major revisions to all sections.
1.3	2011/11/07	Revised section 2.1 EEE Function Enable/Disable, page 4. Revised Figure 22 EEE in 1000M PHY Mode RGMII (RX; Stop RXC) (RXC, RXCTL, and RXD are Halted), page 19.

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1. Introduction

IEEE 802.3az Energy Efficient Ethernet (EEE) reduces the power consumption of Ethernet ports in low power idle mode for 100Mbps and 1000Mbps Ethernet. EEE capability requires the use of a MAC as defined in Annex 4A, for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when PHY is in the low power state.

The MII and (R)GMII signal behavior needs to be modified in both the MAC and PHY if EEE capability is supported. This ensures correct communication between the MAC and PHY for entering low power mode in low traffic situations (no packets need to be sent), or exiting low power mode for data transmission.

In general, the interface from the MAC to the PHY is defined as a 'TX interface' and the interface from the PHY to the MAC is defined as an 'RX interface'.

EEE TX Interface

The MAC uses the following combinations as a request to enter, or remain in low power state (TX LPI).

- MII (100Base-T): TX_EN=0, TX_ER=1, and TXD[3:0]=0x1
- GMII (1000Base-T): TX_EN=0, TX_ER=1, and TXD[7:0]=0x1
- RGMII (100Base-T): TXCTL=0 at TXC rising, TXCTL=1 at TXC falling, and TXD[3:0]=0x1
- RGMII (1000Base-T):
  - TXCTL=0 at TXC rising, TXCTL=1 at TXC falling
  - TXD0=1 at TXC rising , TXD0=0 at TXC falling

EEE RX Interface

The PHY uses the following combinations to indicate that it is receiving LPI (link partner's request to enter, or remain in low power state) (RX LPI).

- MII (100Base-T): RX_DV=0, RX_ER=1, and RXD[3:0]=0x1
- GMII (1000Base-T): RX_DV=0, RX_ER=1, and RXD[7:0]=0x1
- RGMII (100Base-T): RXCTL=0 at RXC rising, RXCTL=1 at RXC falling, and RXD[3:0]=0x1
- RGMII (1000Base-T):
  - RXCTL=0 at RXC rising, RXCTL=1 at RXC falling
  - RXD0=1 at RXC rising, RXD0=0 at RXC falling

MII, GMII, and RGMII TX and RX interface behavior in EEE are described in the following two cases (see Table 1, page 3 for all the conditions).

Case 1

Both MAC and PHY have EEE capability (defined as 'EEE in MAC Mode') and the TX/RX interface follows IEEE 802.3az-2010.

a. For EEE capability, the MAC can assert/de-assert TX LPI.

b. For EEE capability, the PHY can assert/de-assert RX LPI.

c. For EEE capability, the PHY can use an asserted CRS (defined as 'EEE CRS') to notify that the MAC is still asserting TX LPI, and use a de-asserted CRS to notify that the MAC is able to send packets as the MAC has de-asserted TX LPI, and the PHY wake timer has expired.

d. For TX interface power consumption, GMII GTX_CLK, RGMII TXD0, TXCTL, and TXC can be stopped when TX LPI is asserted.

e. For RX interface power consumption, MII RX_CLK, GMII GRX_CLK, RGMII RXD0, RXCTL, and RXC can be stopped when RX LPI is asserted if MMD 3.0.10 (Clock stop enable) is equal to 1.

Case 2

Only the PHY has EEE capability (defined as 'EEE in PHY Mode'). The RX interface follows IEEE 802.3az-2010, but the TX interface does not.

a. The MAC does not support EEE and does not have signaling of TX LPI, however, the PHY only solution with PHY buffer will generate TX LPI requests when there is no traffic.

b. For EEE capability, the PHY can assert/de-assert RX LPI.

c. The MAC does not support EEE, and cannot stop TXC.

d. The MAC does not support EEE, and EEE CRS from the PHY is not needed.

e. MII RX_CLK, GMII GRX_CLK, RGMII RXD0, RXCTL, and RXC signals should be stopped when RX LPI is asserted if (and only if) the MAC can accept a stopped RXC.

f. When the MAC cannot support the stopped RXC from PHY, RX LPI signaling in 1000Base-T RGMII would have RXC, RXCTL, and RXD0 toggling at a frequency of 125MHz, resulting in interface IO power consumption of about 40mA. If RXC/RXCTL/RXD0 is halted, RGMII IO power consumption will be as low as 10mA.

g. When the MAC does not have EEE capability and does not support the RXC being stopped, stopping RXCTL and RXD0 via register setting (see section 2.5, page 8) is suggested in order to reduce the interface IO power consumption. After making this setting, the behavior of the RGMII RX interface is the same as the RGMII RX interface operating in normal mode without EEE capability (defined as 'Normal mode like').

Table 1. Conditions for MAC and PHY Interface Behavior in EEE

Interface/Mode	Behavior	EEE in PHY Mode	EEE in MAC Mode
MII TX LPI	Stop TXC	X	X
	EEE CRS	X	✓/X
MII RX LPI	Stop RXC	✓/X	✓
	Normal Mode Like	X	X
GMII TX LPI	Stop TXC	X	✓
	EEE CRS	X	✓/X
GMII RX LPI	Stop RXC	✓/X	✓
	Normal Mode Like	X	X
RGMII TX LPI	Stop TXC (TXC, TXCTL, TXD0)	X	✓
	EEE CRS	X	X
RGMII RX LPI	Stop RXC (RXC, RXCTL, RXD0)	✓/X	✓
	Normal Mode Like	✓	X

Note 1: ✓ means that the TX or RX interface supports EEE behavior in PHY or MAC mode.

Note 2: X means that the TX or RX interface does not support EEE behavior in PHY or MAC mode.

Note 3: ✓/X means that the TX or RX interface may support or not may support EEE behavior in PHY or MAC mode (this is dependent on the requirements or capabilities of the MAC).

2. EEE Related Parameter Settings

2.1. EEE Function Enable/Disable

Enable (default setting):

Write Register#31=0x0000 (select Page 0)

Write Register#0=0x8000 (phy reset)

Wait 20ms for phy reset

Write Register#31=0x0005 (select Page 5)

Write Register#5=0x8b85

Write Register#6=0xE200 (for RTL8211D)

Write Register#6=0x2AE2 (for RTL8211E)

Write Register#31=0x0007 (select Page 7)

Write Register#30=0x0020

Write Register#21=0x0100 (for RTL8211D)

Write Register#21=0x1108 (for RTL8211E)

Write Register#31=0x0000 (select Page 0)

Write Register#13=0x0007 (set address mode and MMD Device=7)

Write Register#14=0x003c (set address value)

Write Register#13=0x4007 (set data mode and MMD Device=7)

Write Register#14=0x0006 (set data)

Disable:

Write Register#31=0x0000 (select Page 0)

Write Register#0=0x8000 (phy reset)

Wait 20ms for phy reset

Write Register#31=0x0005 (select Page 5)

Write Register#5=0x8b85

Write Register#6=0xC200 (for RTL8211D)

Write Register#6=0x0AE2 (for RTL8211E)

Write Register#31=0x0007 (select Page 7)

Write Register#30=0x0020

Write Register#21=0x0000 (for RTL8211D)

Write Register#21=0x1008 (for RTL8211E)

Write Register#31=0x0000 (select Page 0)

Write Register#13=0x0007 (set address mode and MMD Device=7)

Write Register#14=0x003c (set address value)

Write Register#13=0x4007 (set data mode and MMD Device=7)

Write Register#14=0x0000 (set data)

2.2. EEE in MAC/PHY Mode Selection

EEE in MAC Mode:

Write Register#31=0x0000 (select Page 0)

Write Register#0=0x8000 (phy reset)

Wait 20ms for phy reset

Write Register#31=0x0007 (select Page 7)

Write Register#30=0x0020

Write Register#27=0x2f0a (for RTL8211D)

Write Register#27=0xa03a (for RTL8211E)

Write Register#31=0x0000 (select Page 0)

EEE in PHY Mode (default setting):

Write Register#31=0x0000 (select Page 0)

Write Register#0=0x8000 (phy reset)

Wait 20ms for phy reset

Write Register#31=0x0007 (select Page 7)

Write Register#30=0x0020

Write Register#27=0x2f8a (for RTL8211D)

Write Register#27=0xa0ba (for RTL8211E)

Write Register#31=0x0000 (select Page 0)

2.3. EEE CRS Enable/Disable (RTL8211EG Only)

Enable:

Write Register#31=0x0005 (select Page 5)

Write Register#5=0x8b86 (set address)

Write Register#6=0xF201 (enable EEE CRS)

Write Register#31=0x0000 (select Page 0)

Disable (default setting):

Write Register#31=0x0005 (select Page 5)

Write Register#5 =0x8b86 (set address)

Write Register#6=0xE201 (disable EEE CRS)

Write Register#31=0x0000 (select Page 0)

2.4. EEE RXC Stop Enable/Disable

Enable:

Write Register#31=0x0000 (select Page 0)

Write Register#13=0x0003 (set address mode and MMD Device=3)

Write Register#14=0x0000 (set address value)

Write Register#13=0x4003 (set data mode and MMD Device=3)

Write Register#14=0x0400 (set data)

Disable (default setting):

Write Register#31=0x0000 (select Page 0)

Write Register#13=0x0003 (set address mode and MMD Device=3)

Write Register#14=0x0000 (set address value)

Write Register#13=0x4003 (set data mode and MMD Device=3)

Write Register#14=0x0000 (set data)

2.5. EEE RGMII RXCTL and RXD0 Stop Toggling

Write Register#31=0x0007 (select Page 7)

Write Register#30=0x0020

Write Register#22=0x0001

Write Register#26=0x0001

Write Register#31=0x0000 (select Page 0)

3. EEE in MAC Mode MII/GMII

EEE in MAC Mode means both MAC and PHY have EEE capability.

MDIO Command (Select EEE in MAC Mode):

See section 2.2, page 6 for EEE in MAC Mode settings.

3.1. EEE in MAC Mode MII/GMII TX (Without CRS)

MDIO Command (Disable EEE CRS; RTL8211EG only):

See section 2.3, page 7 for Disable EEE CRS settings.

3.1.1. MII (TX Without CRS; TX_CLK Cannot be Stopped)

For EEE capability, the MAC can assert/de-assert TX LPI (see EEE TX Interface, page 1).

MII TX_CLK cannot be stopped as MII TX_CLK is provided by the PHY side.

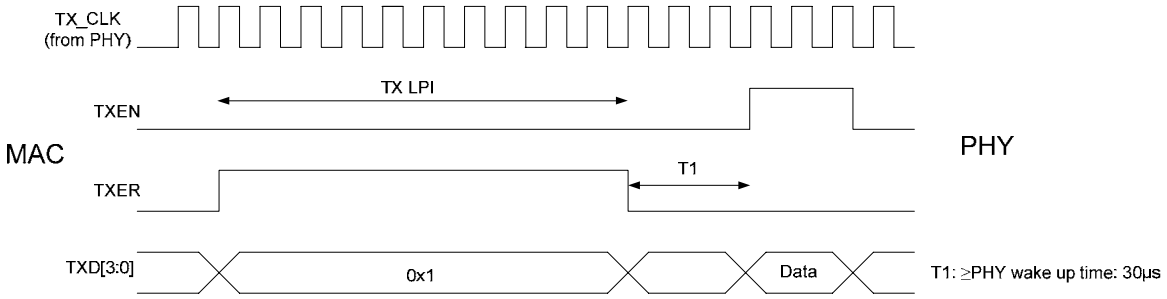

Figure 1. EEE in MAC Mode MII (TX without CRS; TX_CLK Cannot be Stopped)

3.1.2. GMII (TX Without CRS; Stop GTX_CLK)

For EEE capability, the MAC can assert/de-assert TX LPI (see EEE TX Interface, page 1).

For TX power consumption, GMII GTX_CLK can be stopped by the MAC side when TX LPI is asserted.

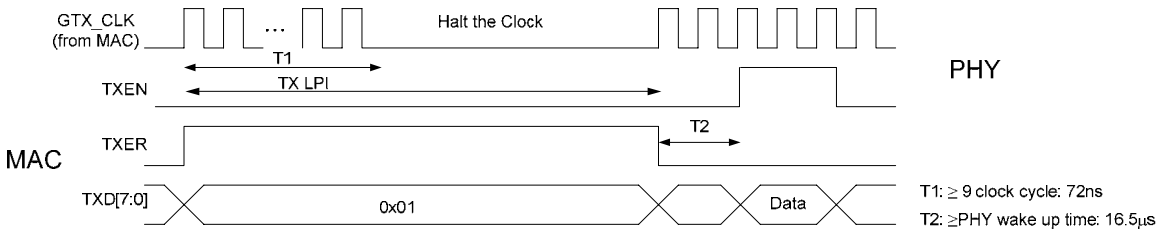

Figure 2. EEE in MAC Mode GMII (TX without CRS; Stop GTX_CLK)

3.2. EEE in MAC Mode MII/GMII TX (With CRS)

MDIO Command (Enable EEE CRS; RTL8211EG only):

See section 2.3, page 7 for Enable EEE CRS settings.

3.2.1. MII (TX with CRS; TX_CLK Cannot be Stopped)

For EEE capability, the MAC can assert/de-assert TX LPI (see EEE TX Interface, page 1) and CRS to notify whether the MAC can transmit packets or not.

MII TX_CLK cannot be stopped as MII TX_CLK is provided by the PHY side.

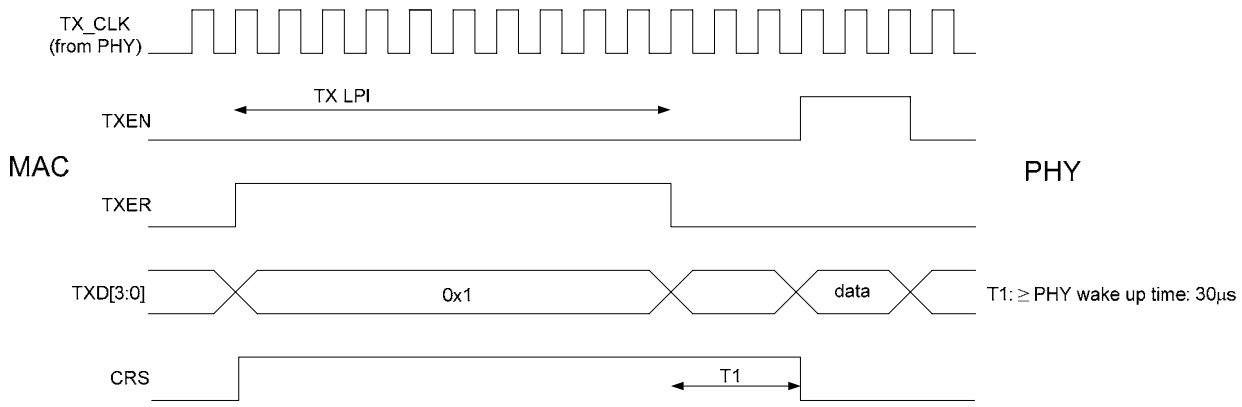

Figure 3. EEE in MAC Mode MII (TX with CRS; TX_CLK Cannot be Stopped)

3.2.2. GMII (TX with CRS; Stop GTX_CLK)

For EEE capability, the MAC can assert/de-assert TX LPI (see EEE TX Interface, page 1) and CRS to notify whether the MAC can transmit packets or not.

For TX power consumption, GMII GTX_CLK can be stopped by the MAC side when TX LPI is asserted.

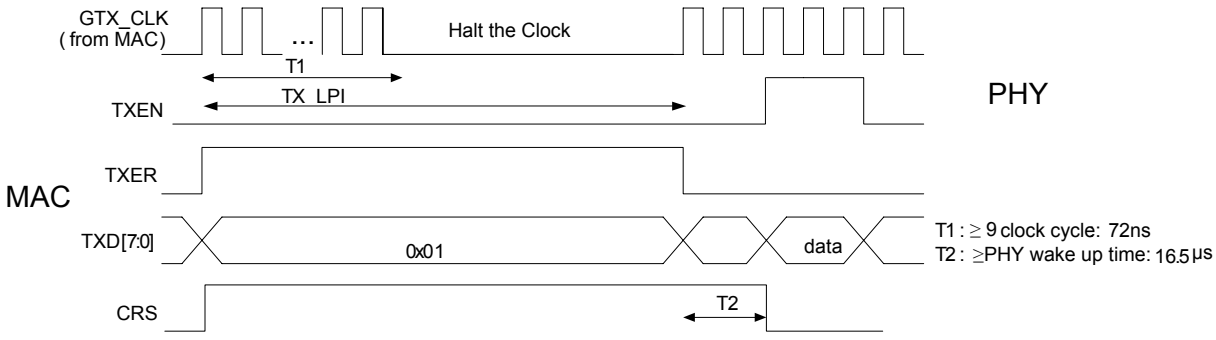

Figure 4. EEE in MAC Mode GMII (TX with CRS; Stop GTX_CLK)

3.3. EEE in MAC Mode MII/GMII RX

MDIO Command (Enable RXC Stop):

Please see section 2.4, page 7 for Enable RXC Stop settings.

3.3.1. MII (RX; Stop RX_CLK)

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

For RX power consumption, MII RX_CLK can be stopped when RX LPI is asserted if MMD 3.0.10 (clock stop enable) is equal to 1.

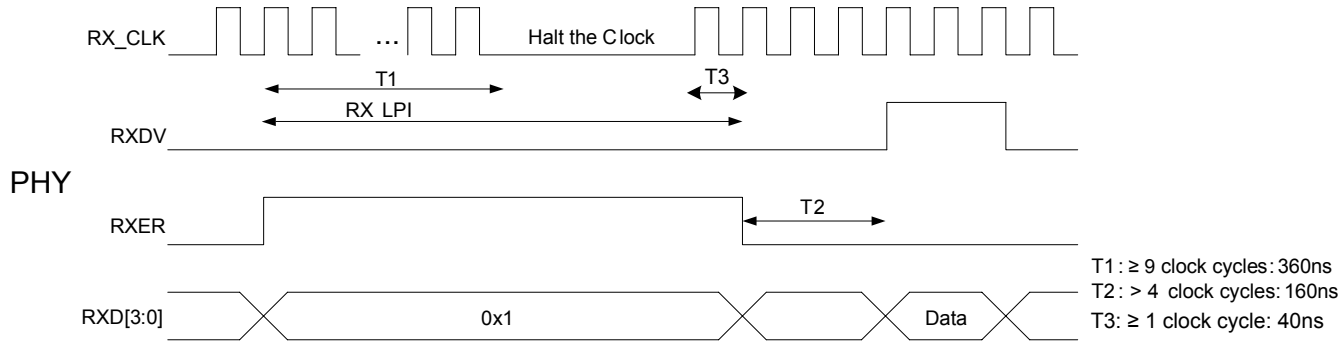

Figure 5. EEE in MAC Mode MII (RX; Stop RX_CLK)

3.3.2. GMII (RX; Stop GRX_CLK)

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

For RX power consumption, GMII GRX_CLK can be stopped when RX LPI is asserted if MMD 3.0.10 (clock stop enable) is equal to 1.

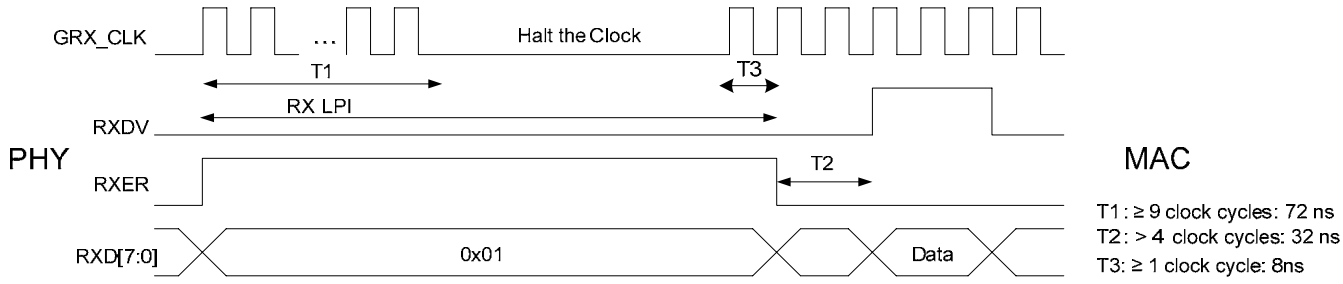

Figure 6. EEE in MAC Mode GMII (RX; Stop GRX_CLK)

4. EEE in PHY Mode MII/GMII

EEE in PHY Mode means only the PHY has EEE capability (the MAC does not support EEE).

MDIO Command (Select EEE in PHY Mode):

See section 2.2, page 6 for EEE in PHY Mode settings.

4.1. EEE in PHY Mode MII/GMII TX

In this mode the MAC does not support EEE and does not have a TX LPI signal. The PHY buffer will generate TX LPI requests when there are no packets to be transmitted.

4.1.1. MII (TX; TX_CLK Cannot be Stopped)

The MAC has no EEE capability and cannot assert/de-assert TX LPI (see EEE TX Interface, page 1).

MII TX_CLK cannot be stopped because MII TX_CLK is provided by the PHY side.

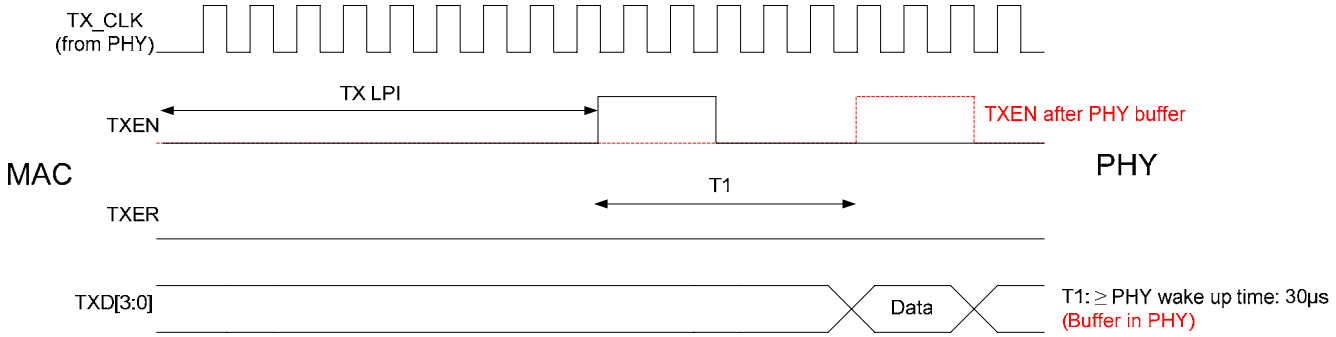

Figure 7. EEE in PHY Mode MII (TX; TX_CLK Cannot be Stopped)

4.1.2. GMII (TX; GTX_CLK Cannot be Stopped)

The MAC has no EEE capability and cannot assert/de-assert TX LPI (see EEE TX Interface, page 1) so the GMII GTX_CLK cannot be stopped by the MAC side.

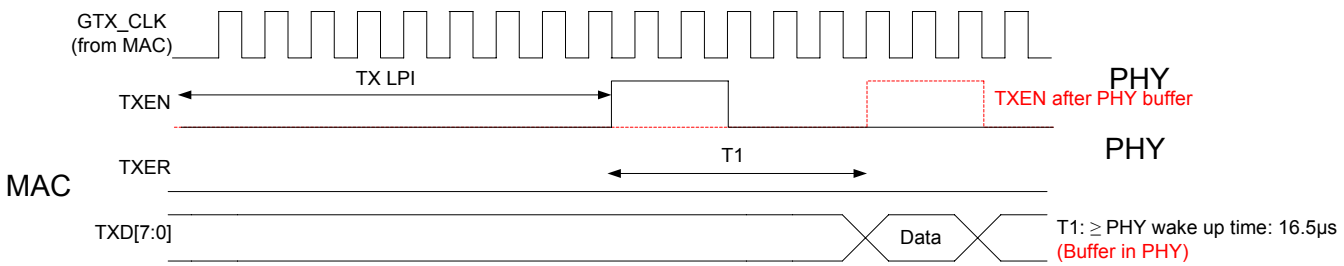

Figure 8. EEE in PHY Mode GMII (TX; GTX_CLK Cannot be Stopped)

4.2. EEE in PHY Mode MII/GMII (RX, RXC Cannot be Stopped)

In this mode, the MAC does not support RXC Stop.

MDIO Command (Disable RXC Stop):

See section 2.4, page 7 for Disable RXC Stop settings.

4.2.1. MII (RX; RX_CLK Cannot be Stopped) (Default Setting)

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

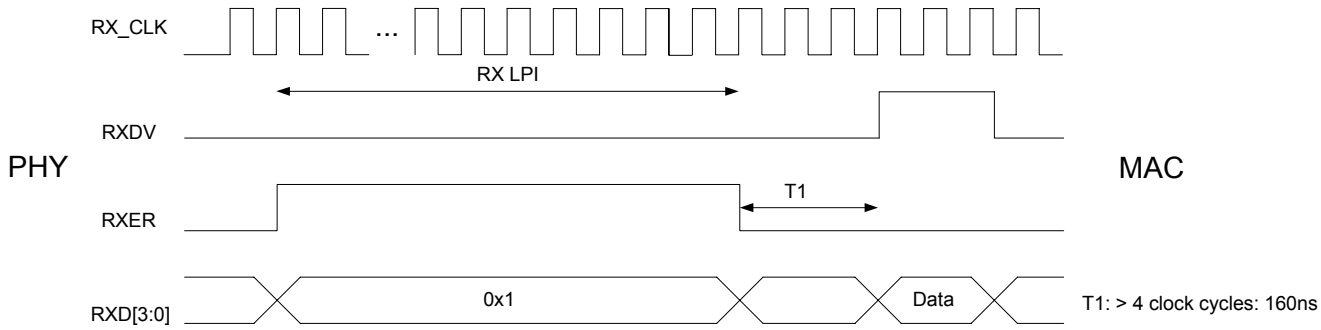

Figure 9. EEE in PHY Mode MII (RX; RX_CLK Cannot be Stopped) (Default Setting)

4.2.2. GMII (RX; GRX_CLK Cannot be Stopped) (Default Setting)

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

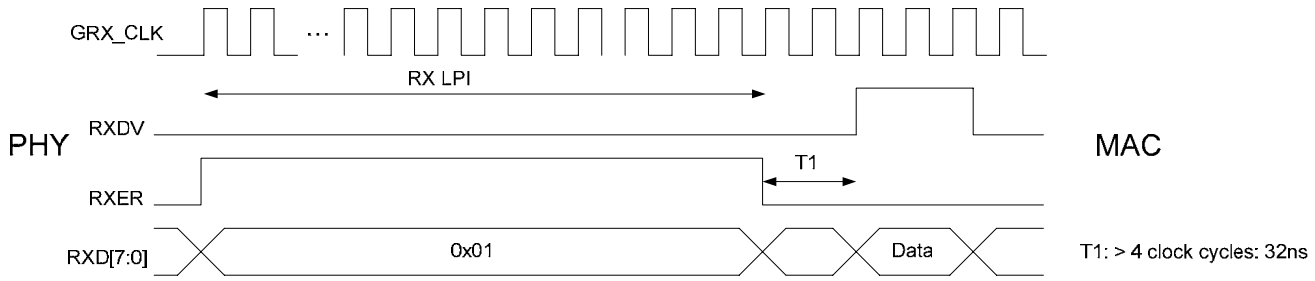

Figure 10. EEE in PHY Mode GMII (RX; GRX_CLK Cannot be Stopped) (Default Setting)

4.3. EEE in PHY Mode MII/GMII (RX, Stop RXC)

In this mode, the MAC supports RXC Stop.

MDIO Command (Enable RXC Stop):

See section 2.4, page 7 for Enable RXC Stop settings.

4.3.1. MII (RX; Stop RX_CLK)

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

For RX power consumption, MII RX_CLK can be stopped when RX LPI is asserted if MMD 3.0.10 (clock stop enable) is equal to 1 and the MAC can accept the stopped MII RX_CLK.

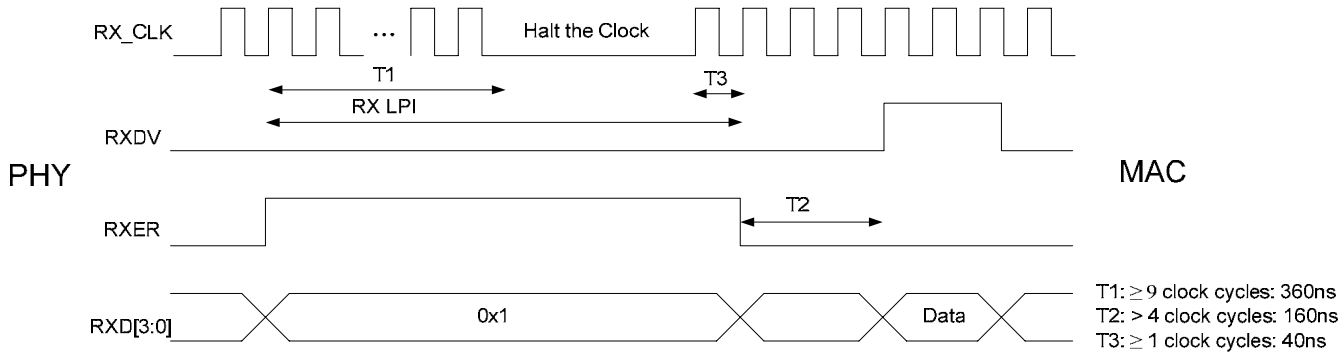

Figure 11. EEE in PHY Mode MII (RX; Stop RX_CLK)

4.3.2. GMII (RX; Stop GRX_CLK)

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

For RX power consumption, GMII RX_CLK can be stopped when RX LPI is asserted if MMD 3.0.10 (clock stop enable) is equal to 1 and the MAC can accept the stopped GMII GRX_CLK.

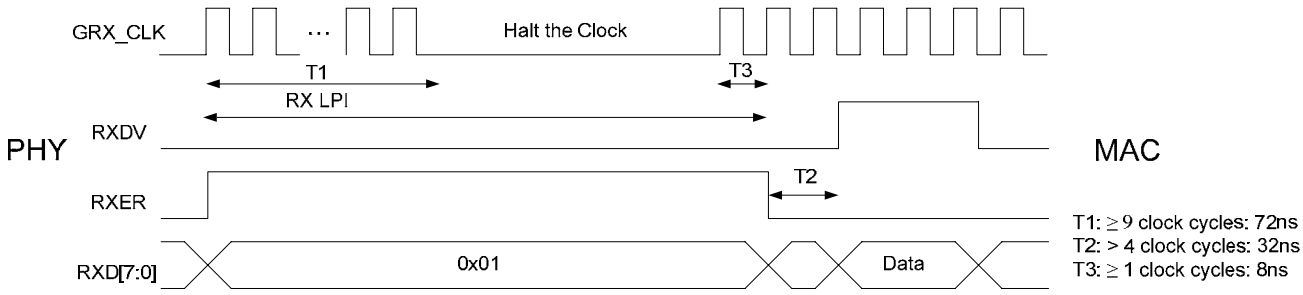

Figure 12. EEE in PHY Mode GMII (RX; Stop GRX_CLK)

5. EEE in MAC Mode RGMII

EEE in MAC Mode means that both MAC and PHY have EEE capability.

MDIO Command (Select EEE in MAC Mode):

See section 2.2, page 6 for EEE in MAC Mode settings.

5.1. EEE in MAC Mode RGMII (TX; Stop TXC)

For EEE capability, the MAC can assert/de-assert TX LPI (see EEE TX Interface, page 1).

For TX power consumption, RGMII TXC, TXCTL, and TXD can be stopped by the MAC side when TX LPI is asserted.

5.1.1. 100M (TX; Stop TXC)

RGMII TX LPI in 100Base-T has TXC and TXCTL toggling, and Stop TXC means both TXC and TXCTL stop toggling.

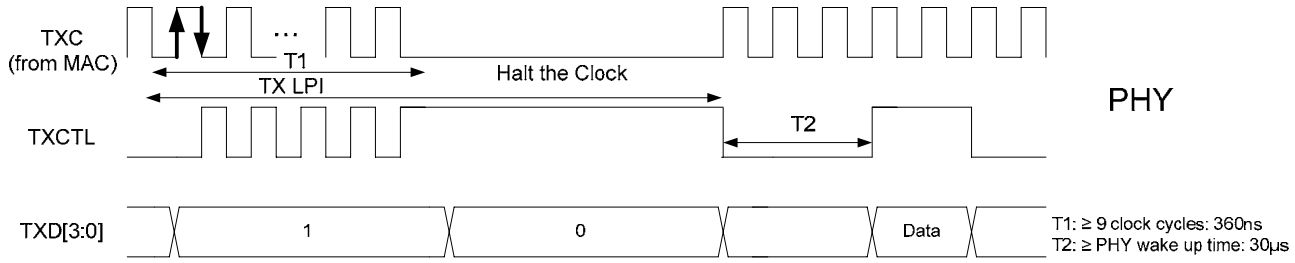

Figure 13. EEE in 100M MAC Mode RGMII (TX; Stop TXC) (TXC/TXCTL/TXD)

5.1.2. 1000M (TX; Stop TXC)

RGMII TX LPI in 1000Base-T has TXC, TXCTL, and TXD toggling. Stop TXC means TXC, TXCTL, and TXD all stop toggling.

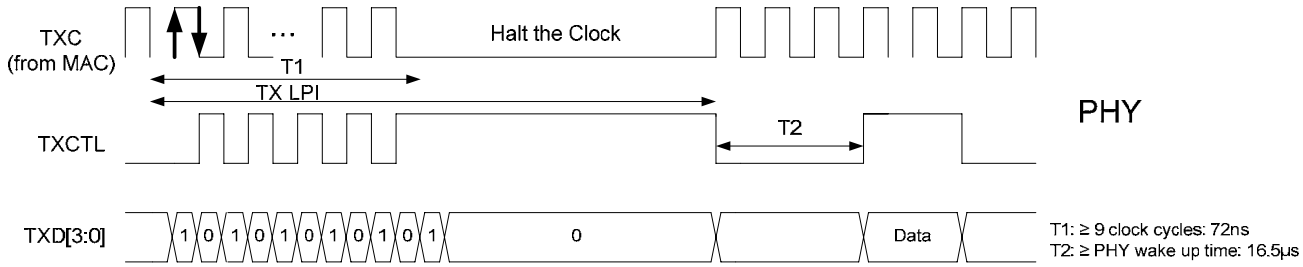

Figure 14. EEE in 1000M MAC Mode RGMII (TX; Stop TXC) (TXC/TXCTL/TXD)

5.2. EEE in MAC Mode RGMII (RX; Stop RXC) (RXC, RXCTL, and RXD are Stopped)

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

For RX power consumption, RGMII RXC, RXCTL, and RXD can be stopped when RX LPI is asserted if MMD 3.0.10 (clock stop enable) is equal to 1.

MDIO Command (Enable RXC Stop):

See section 2.4, page 7 for Enable RXC Stop settings.

5.2.1. 100M (RX; Stop RXC)

RGMII RX LPI in 100Base-T has RXC and RXCTL toggling, and Stop RXC means both RXC and RXCTL stop toggling.

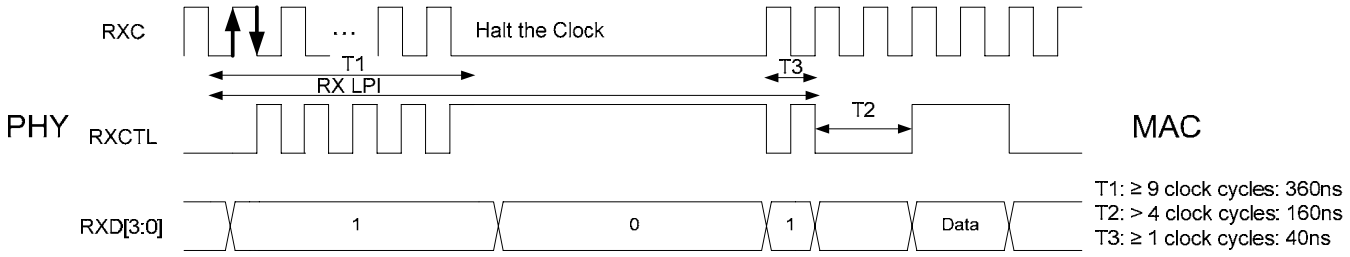

Figure 15. EEE in 100M MAC Mode RGMII (RX; Stop RXC) (RXC, RXCTL, and RXD are Stopped)

5.2.2. 1000M (RX; Stop RXC)

RGMII RX LPI in 1000Base-T has RXC, RXCTL, and RXD toggling. Stop RXC means RXC, RXCTL, and RXD all stop toggling.

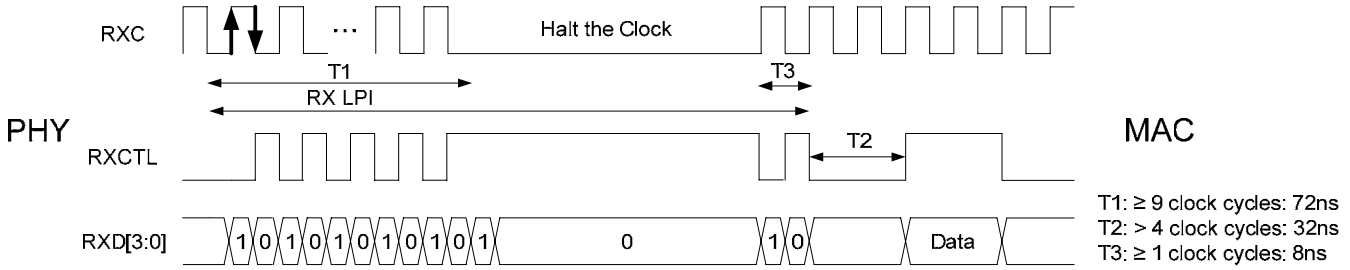

Figure 16. EEE in 1000M MAC Mode RGMII (RX; Stop RXC) (RXC, RXCTL, and RXD are Halted)

6. EEE in PHY Mode RGMII

EEE in PHY Mode means only the PHY has EEE capability (the MAC does not support EEE).

MDIO Command (Select EEE in PHY Mode):

See section 2.2, page 6 for the EEE in PHY Mode settings.

6.1. EEE in PHY Mode RGMII (TX; TXC Cannot be Stopped)

In this mode the MAC does not support EEE and does not have a TX LPI signal, so the RGMII TXC cannot be stopped by the MAC side. The PHY buffer will generate TX LPI requests when there are no packets to be transmitted.

6.1.1. 100M (TX; TXC Cannot be Stopped)

RGMII TX LPI in 100Base-T has only TXC toggling, and TXC cannot be stopped.

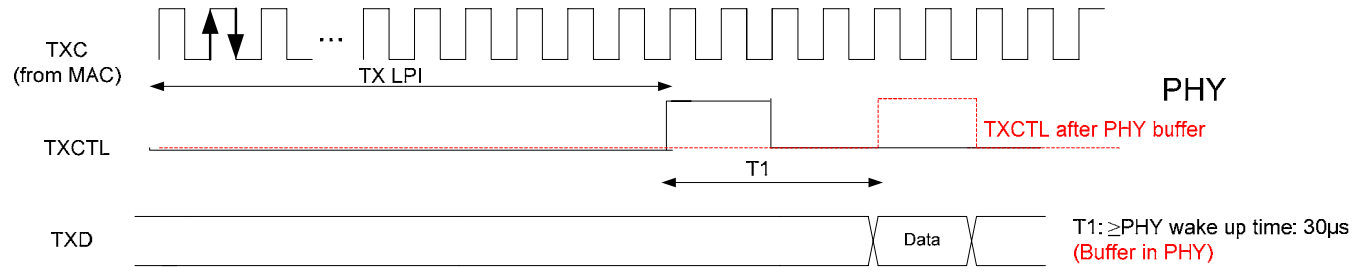

Figure 17. EEE in 100M PHY Mode RGMII (TX; TXC Cannot be Stopped)

6.1.2. 1000M (TX; TXC Cannot be Stopped)

RGMII TX LPI in 1000Base-T has only TXC toggling, and TXC cannot be stopped.

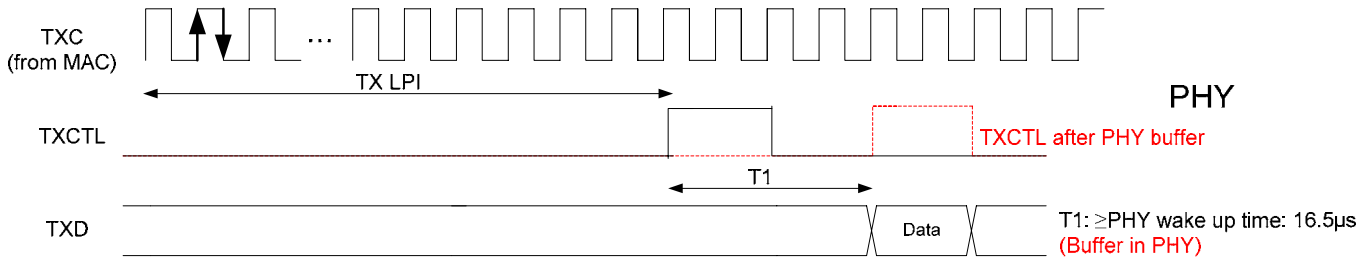

Figure 18. EEE in 1000M PHY Mode RGMII (TX; TXC Cannot be Stopped)

6.2. EEE in PHY Mode RGMII (RX; RXC Cannot be Stopped) (Default Setting)

In this mode the MAC does not support RXC Stop.

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

MDIO Command (Disable RXC Stop):

Please see section 2.4, page 7 for Disable RXC Stop settings.

6.2.1. 100M (RX; RXC Cannot be Stopped)

RGMII RX LPI in 100Base-T has RXC and RXCTL toggling, and RXC cannot be stopped.

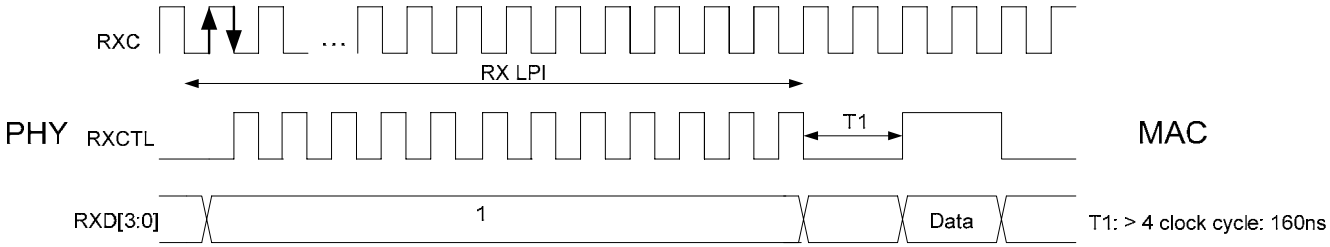

Figure 19. EEE in 100M PHY Mode RGMII (RX; RXC Cannot be Stopped) (Default Setting)

6.2.2. 1000M (RX; RXC Cannot be Stopped)

RGMII RX LPI in 1000Base-T has RXC, RXCTL, and RXD toggling, and RXC cannot be stopped.

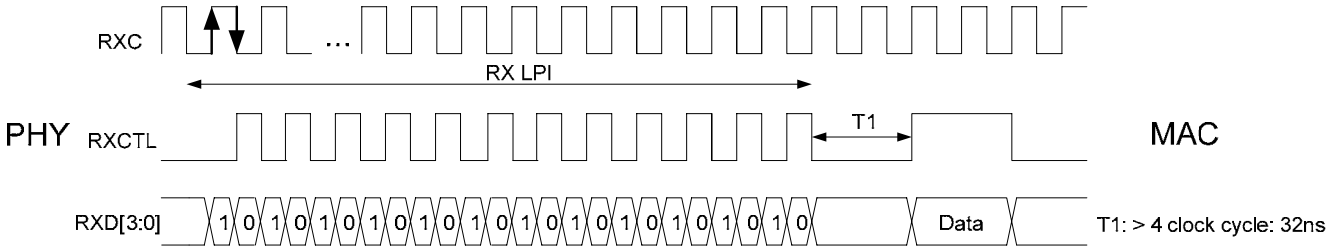

Figure 20. EEE in 1000M PHY Mode RGMII (RX; RXC Cannot be Stopped) (Default Setting)

6.3. EEE in PHY Mode RGMII (RX; Stop RXC) (RXC, RXCTL, and RXD are Stopped)

In this mode, the MAC supports RXC Stop.

For EEE capability, the PHY can assert/de-assert RX LPI (see EEE RX Interface, page 1).

For RX power consumption, RGMII RXC can be stopped when RX LPI is asserted if MMD 3.0.10 (clock stop enable) is equal to 1 and the MAC can accept the stopped RXC.

MDIO Command (Enable RXC Stop):

See section 2.4, page 7 for Enable RXC Stop settings.

6.3.1. 100M (RX; Stop RXC)

RGMII RX LPI in 100Base-T has RXC and RXCTL toggling, and Stop RXC means both RXC and RXCTL stop toggling.

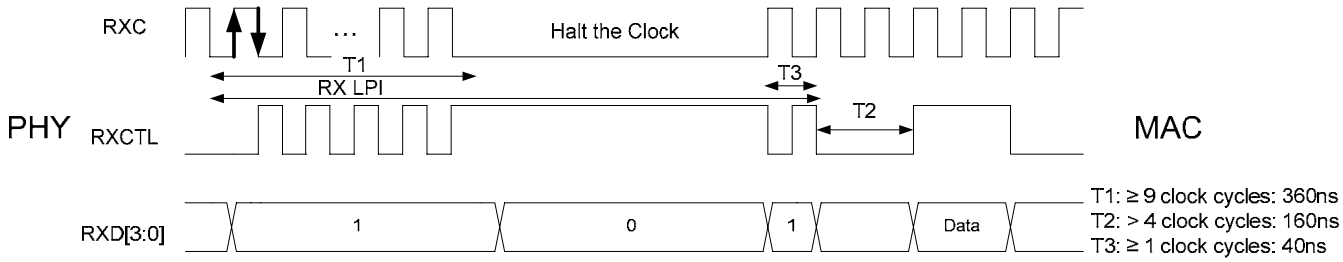

Figure 21. EEE in 100M PHY Mode RGMII (RX; Stop RXC) (RXC, RXCTL, and RXD are Halted)

6.3.2. 1000M (RX; Stop RXC)

RGMII RX LPI in 1000Base-T has RXC, RXCTL, and RXD toggling. Stop RXC means RXC, RXCTL, and RXD all stop toggling.

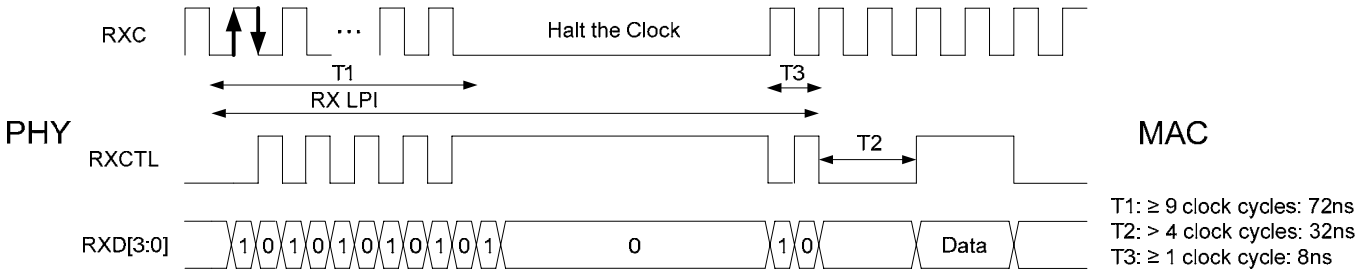

Figure 22. EEE in 1000M PHY Mode RGMII (RX; Stop RXC) (RXC, RXCTL, and RXD are Halted)

6.4. EEE in PHY Mode RGMII (RX; Normal Mode) (RXCTL and RXD Not Toggling)

In this mode, the MAC cannot support the RXC Stop.

The setting of stopping RXCTL and RXD0 will reduce the interface IO power consumption. After this setting, the RGMII RX behavior is the same as the RGMII RX interface operating in normal mode (with no EEE capability). The PHY cannot assert/de-assert RX LPI (see EEE RX Interface, page 1).

MDIO Command (Disable RXCTL/RXD Toggling):

See section 2.5, page 8 for Disable RXCTL and RXD toggling settings.

MDIO Command (Disable RXC Stop):

See section 2.4, page 7 for Disable RXC Stop settings.

6.4.1. 100M (RX; Normal Mode)

RGMII RX LPI in 100Base-T has only RXC toggling, and RXCTL behaves as if operating in normal mode (with no EEE capability).

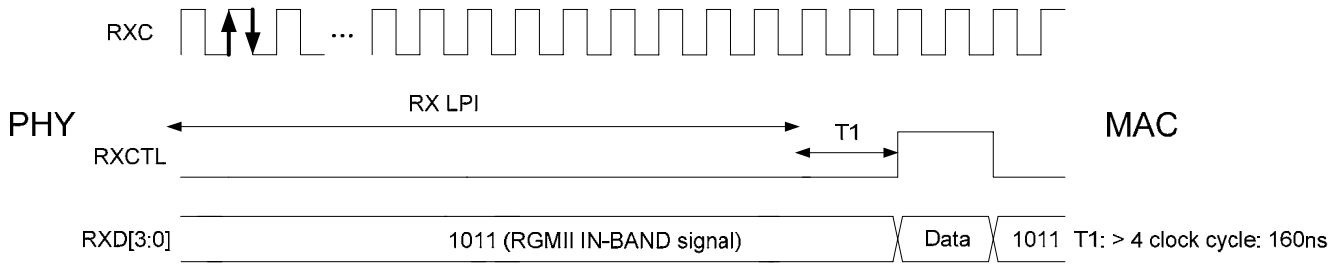

Figure 23. EEE in 100M PHY Mode RGMII (RX; Normal Mode) (RXCTL and RXD Not Toggling)

6.4.2. 1000M (RX; Normal Mode)

RGMII RX LPI in 1000Base-T has only RXC toggling, and RXCTL and RXD behave as if operating in normal mode (with no EEE capability).

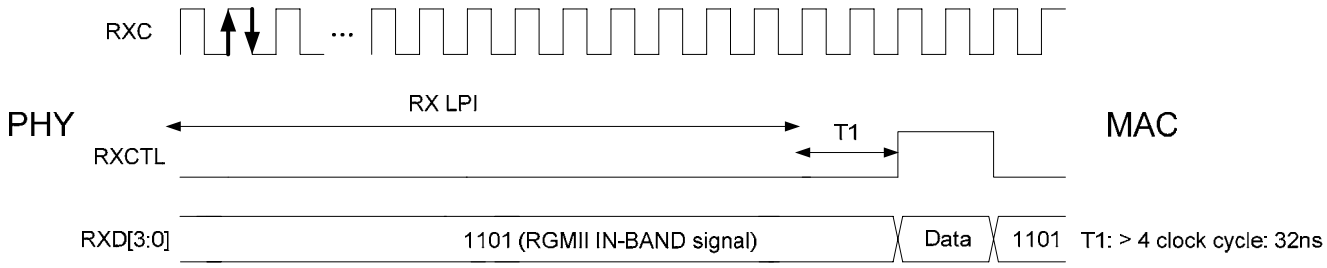

Figure 24. EEE in 1000M PHY Mode RGMII (RX; Normal Mode) (RXCTL and RXD Not Toggling)

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