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RTL8376-GR

16-PORT 10/100/1000 SWITCH CONTROLLER WITH INTEGRATED OCTAL GIGA-PHY

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8376 IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2009/09/28	First release.
1.1	2009/12/17	Revised Table 6 Miscellaneous Pins, page 10 (ATEST-1 and ATEST-2 pins). Revised section 8.1.1 Hardware Reset, page 14. Revised Figure 8 RTL8376+RTL8231 for One Single and One Bi-Color LED, page 24. Revised section 11.5 Reset Characteristics, page 45.
1.2	2010/11/26	Revised Figure 11 8-Bit Address EEPROM Sequential Read, page 26. Revised Figure 12 16-Bit Address EEPROM Sequential Read, page 26. Revised Table 23 Recommended Operating Range, page 37. Revised section 11.3 Thermal Characteristics, page 38. Revised Table 30 EEPROM SMI Host Mode Timing Characteristics, page 42. Revised Table 32 MIIM (MDC/MDIO) Timing Characteristics, page 44.
1.3	2011/06/14	Revised section 12 Mechanical Dimensions, page 46.

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1. General Description

The RTL8376-GR is a 128-pin, low-power consumption, high-performance 16-port 10/100/1000M Ethernet switch, with integrated 8-port Giga-PHY that supports 1000Base-T, 100Base-T, and 10Base-T. The 5~8th port's MACs implement dual RSGMII-Plus interfaces for connecting with an external PHY (e.g., RTL8218) in 16-port switch applications. The RTL8376-GR integrates all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS mixed mode device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8376 features superior memory management technology to efficiently utilize memory space. The RTL8376 integrates an 8K-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the EEPROM Serial Management Interface (SMI), and each of the entries can be configured as a static entry. The entry aging time is between 200 and 400 seconds. Eight Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The RTL8376 supports standard 802.3x flow control frames for full duplex and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8376 supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only.

In order to support flexible traffic classification, the RTL8376 supports 32-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, and rate policing. The rate policing mechanism supports from 64Kbps to 1Gbps (in 64Kbps steps)

To improve real-time or multimedia networking applications, the RTL8376 supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There are 2 leaky buckets for each queue of all ports, one for Average packet rate control and the other for Peak packet rate control. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or mixed.

The RTL8376 provides a 4K-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8376 supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or EEPROM SMI Slave after reset. The RTL8376 also provides a Leaky VLAN function to meet special VLAN application requirements. This function can send unicast frames to other VLANs, or only forwards unicast frames to the originating VLAN. The VLAN tags can be inserted or removed on a per-port basis.

2. Features

- 16-port gigabit non-blocking switch architecture
  - Embedded 8-port 10/100/1000Base-T PHY
  - Integrates 2 pairs of 5GHz high-speed serial links (Reduced Serial Gigabit Media Independent Interface-RSGMII-Plus)
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Supports pre-IEEE 802.3az Energy Efficient Ethernet.
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Integrated SRAM for packet buffer
- Supports packet length 9216 bytes jumbo frame packet forwarding at wire speed
- Supports Realtek Cable Test (RTCT) function
- Supports ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions support dropping, priority adjustment, and traffic rate policing
  - Optional setting of per-port action to take when ACL mismatch
- VLAN
  - 802.1Q VLAN supports for 4096 entries
  - Supports Port-based, Tag-based, and Protocol-based VLAN
  - Supports per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL/SVL
- Supports Quality of Service (QoS)
  - Input Bandwidth Control from 8Kbps to 1Gbps (in 8Kbps steps)
  - Traffic classification based on IEEE 802.1Q priority definition, physical Port, ACL definition, VLAN based priority
  - Scheduling supports Strict Priority (SP) and Weighted Fair Queuing (WFQ)
  - Supports per queue flow control
  - Min-Max Scheduling
- Security Filtering
  - Disable learning for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports Realtek Green Ethernet features
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving
- Each port supports 3 LED outputs via serial MDIO interface
- Supports EEPROM SMI Slave interface to access configuration register
- Supports 2048-byte EEPROM space for configuration
- 25MHz crystal or 3.3V OSC input
- Low Power consumption < 460mW/port
- LQFP 128-pin E-PAD package

3. System Applications

3.1. 16-Port 1000Base-T Switch

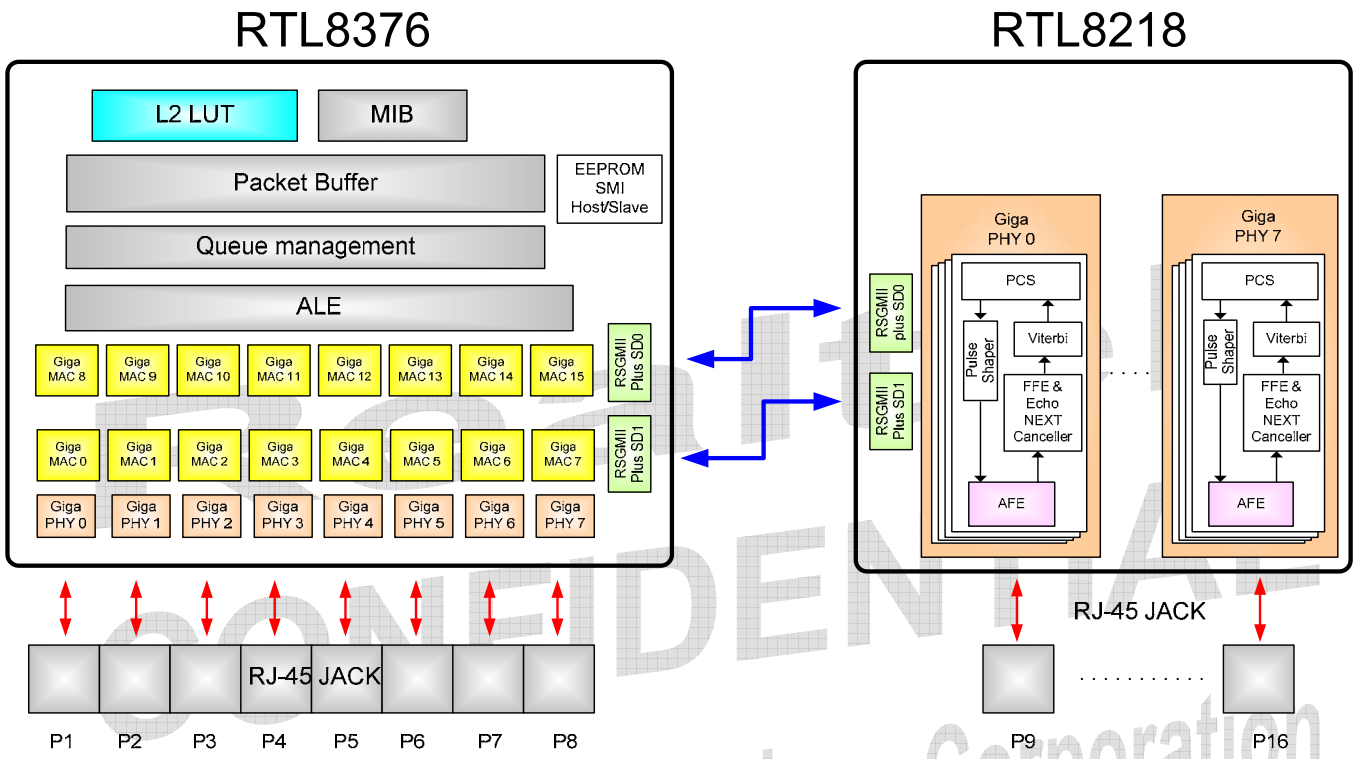


Figure 1. 16-Port 1000Base-T Switch

4. Block Diagram

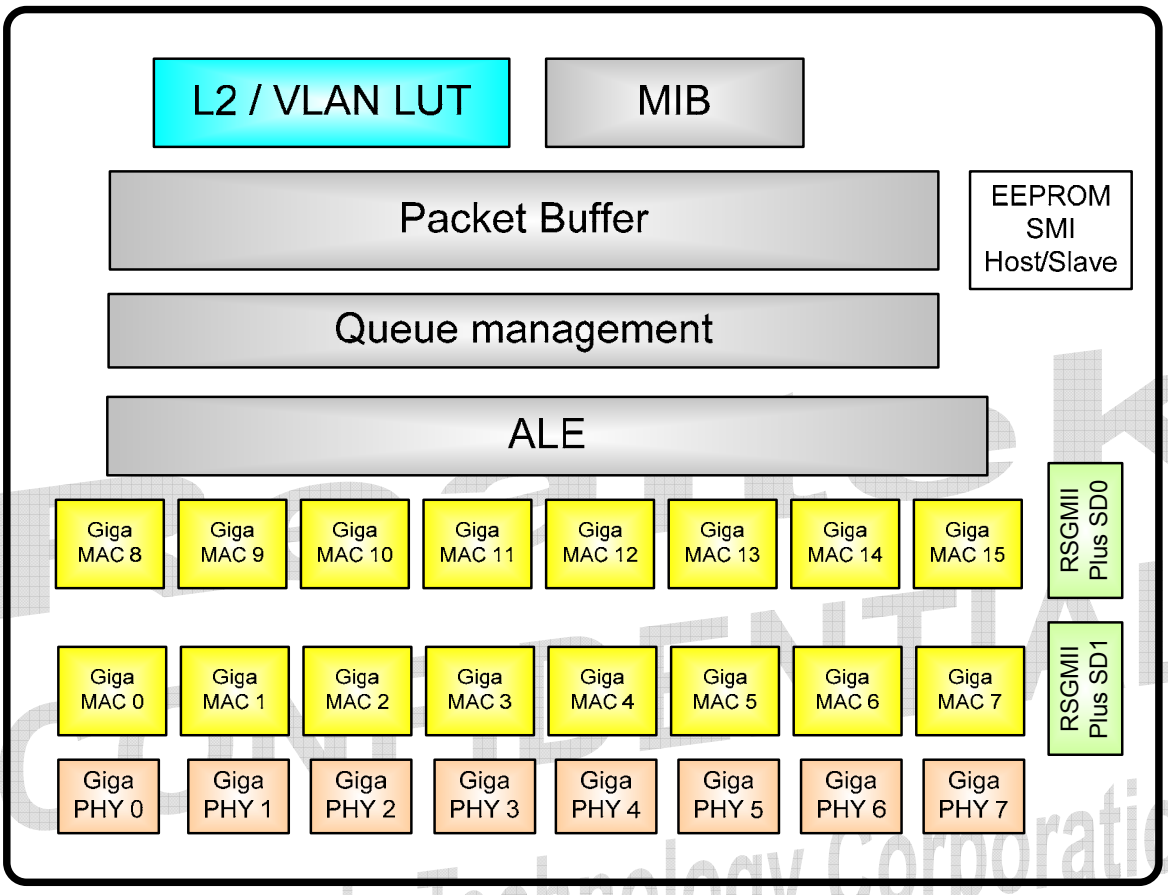


Figure 2. Block Diagram

5. Pin Assignments

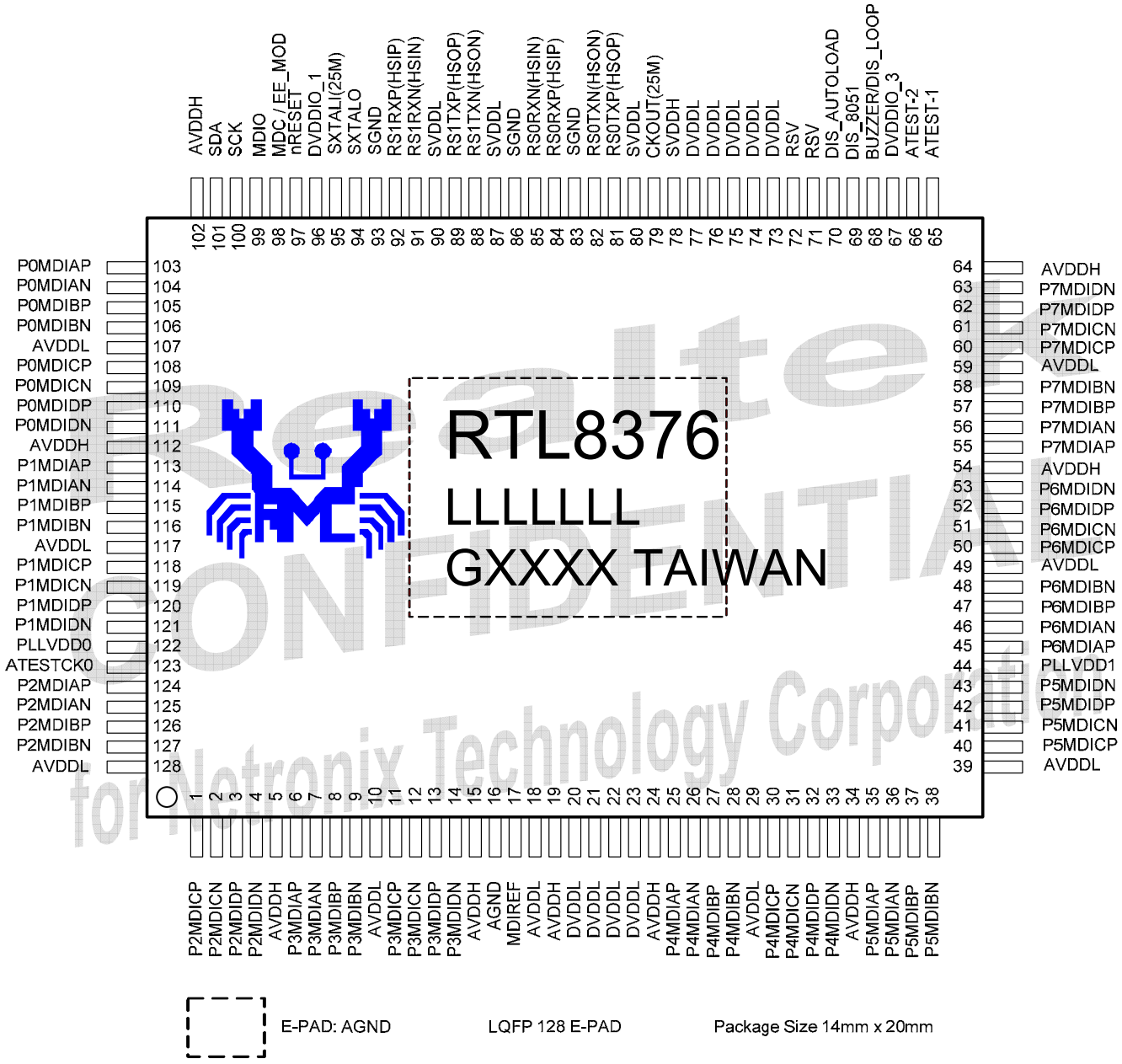


Figure 3. Pin Assignments

5.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 3).

5.2. Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75Kohm)

I_S: Schmitt-Trigger Input Pin

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75Kohm)

Table 1. Pin Assignment Table

Name	Pin No.	Type
P2MDICP	1	AI/O
P2MDICN	2	AI/O
P2MDIDP	3	AI/O
P2MDIDN	4	AI/O
AVDDH	5	AP
P3MDIAP	6	AI/O
P3MDIAN	7	AI/O
P3MDIBP	8	AI/O
P3MDIBN	9	AI/O
AVDDL	10	AP
P3MDICP	11	AI/O
P3MDICN	12	AI/O
P3MDIDP	13	AI/O
P3MDIDN	14	AI/O
AVDDH	15	AP
AGND	16	AG
MDIREF	17	A
AVDDL	18	AP
AVDDH	19	AP
DVDDL	20	P
DVDDL	21	P
DVDDL	22	P

Name	Pin No.	Type
DVDDL	23	P
AVDDH	24	AP
P4MDIAP	25	AI/O
P4MDIAN	26	AI/O
P4MDIBP	27	AI/O
P4MDIBN	28	AI/O
AVDDL	29	AP
P4MDICP	30	AI/O
P4MDICN	31	AI/O
P4MDIDP	32	AI/O
P4MDIDN	33	AI/O
AVDDH	34	AP
P5MDIAP	35	AI/O
P5MDIAN	36	AI/O
P5MDIBP	37	AI/O
P5MDIBN	38	AI/O
AVDDL	39	AP
P5MDICP	40	AI/O
P5MDICN	41	AI/O
P5MDIDP	42	AI/O
P5MDIDN	43	AI/O
PLLVDD1	44	AP

Name	Pin No.	Type
P6MDIAP	45	AO
P6MDIAN	46	AI/O
P6MDIBP	47	AI/O
P6MDIBN	48	AI/O
AVDDL	49	AI/O
P6MDICP	50	AP
P6MDICN	51	AI/O
P6MDIDP	52	AI/O
P6MDIDN	53	AI/O
AVDDH	54	AI/O
P7MDIAP	55	AP
P7MDIAN	56	AI/O
P7MDIBP	57	AI/O
P7MDIBN	58	AI/O
AVDDL	59	AI/O
P7MDICP	60	AP
P7MDICN	61	AI/O
P7MDIDP	62	AI/O
P7MDIDN	63	AI/O
AVDDH	64	AI/O
ATEST-1	65	AO
ATEST-2	66	AI/O
DVDDIO_3	67	P
BUZZER/DIS_LOOP	68	I/O_{PU}
DIS_8051	69	I/O_{PU}
DIS_AUTOLOAD	70	I/O_{PU}
RSV	71	I/O_{PU}
RSV	72	I/O_{PU}
DVDDL	73	P
DVDDL	74	P
DVDDL	75	P
DVDDL	76	P
DVDDL	77	P
SVDDH	78	SP
CKOUT(25M)	79	AO
SVDDL	80	SP
RS0TXP(HSOP)	81	AO
RS0TXN(HSON)	82	AO
SGND	83	AG
RS0RXP(HSIP)	84	AI
RS0RXN(HSIN)	85	AI
SGND	86	SG
SVDDL	87	SP

Name	Pin No.	Type
RS1TXN(HSON)	88	AO
RS1TXP(HSOP)	89	AO
SVDDL	90	SP
RS1RXN(HSIN)	91	AI
RS1RXP(HSIP)	92	AI
SGND	93	SG
SXTALO	94	AO
SXTALI(25M)	95	AI
DVDDIO_1	96	P
nRESET	97	I_S
MDC/EE_MOD	98	I/O_{PU}
MDIO	99	I/O
SCK	100	I/O
SDA	101	I/O
AVDDH	102	AP
P0MDIAP	103	AI/O
P0MDIAN	104	AI/O
P0MDIBP	105	AI/O
P0MDIBN	106	AI/O
AVDDL	107	AP
P0MDICP	108	AI/O
P0MDICN	109	AI/O
P0MDIDP	110	AI/O
P0MDIDN	111	AI/O
AVDDH	112	AP
P1MDIAP	113	AI/O
P1MDIAN	114	AI/O
P1MDIBP	115	AI/O
P1MDIBN	116	AI/O
AVDDL	117	AP
P1MDICP	118	AI/O
P1MDICN	119	AI/O
P1MDIDP	120	AI/O
P1MDIDN	121	AI/O
PLLVDD0	122	AP
ATESTCK0	123	AO
P2MDIAP	124	AI/O
P2MDIAN	125	AI/O
P2MDIBP	126	AI/O
P2MDIBN	127	AI/O
AVDDL	128	P
E-PAD	129	AG/G

6. Pin Descriptions

6.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Description
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	103, 104 105, 106 108, 109 110, 111	AI/O	Port 0 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	113, 114 115, 116 118, 119 120, 121	AI/O	Port 1 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	124, 125 126, 127 1, 2 3, 4	AI/O	Port 2 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	6, 7 8, 9 11, 12 13, 14	AI/O	Port 3 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P4MDIAP/N P4MDIBP/N P4MDICP/N P4MDIDP/N	25, 26 27, 28 30, 31 32, 33	AI/O	Port 4 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P5MDIAP/N P5MDIBP/N P5MDICP/N P5MDIDP/N	35, 36 37, 38 40, 41 42, 43	AI/O	Port 5 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P6MDIAP/N P6MDIBP/N P6MDICP/N P6MDIDP/N	45, 46 47, 48 50, 51 52, 53	AI/O	Port 6 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.

Pin Name	Pin No.	Type	Description
P7MDIAP/N P7MDIBP/N P7MDICP/N P7MDIDP/N	55, 56 57, 58 60, 61 62, 63	AI/O	Port 7 Media Dependent Interface A~D For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.

6.2. RSGMII Interface Pins

Table 3. RSGMII Pins

Pin Name	Pin No.	Type	Description
RS0RXP/N RS1RXP/N	84, 85 92, 91	AO	RSGMII-Plus Differential Input. 5GHz serial interfaces to receive data from an External device that supports the RSGMII-Plus interface.
RS0TXP/N RS1TXP/N	81, 82 89, 88	AO	RSGMII-Plus Differential Output. 5GHz serial interfaces to transfer data from the RTL8376 to an External device that supports the RSGMII-Plus interface.
CKOUT	79	AO	SCKOUT is 25MHz Reference Clock Output for the RSGMII-Plus Interface. SVDDL voltage level signal.

6.3. Configuration Strapping Pins

Table 4. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
BUZZER/DIS_LOOP	68	I/O_{PU}	Realtek Loop Detection Configuration Pull-up: eDisable Loop detection function Pull-down: Enable Loop detection function
DIS_8051	69	I/O_{PU}	Embedded 8051 Configuration Pull-up: Disable embedded 8051 function Pull-down: Enable embedded 8051 function
DIS_AUTOLOAD	70	I/O_{PU}	EEPROM Autoload Configuration Pull Up: Disable EEPROM auto-load function Pull Down: Enable EEPROM auto-load function *Note: When DIS_AUTOLOAD=0 and DIS_8051=1, the EEPROM data will be treated as configuration data at power on or reset initial stage.* *When DIS_AUTOLOAD=0 and DIS_8051=0, the EEPROM data will be loaded to embedded 8051 instruction memory at power on or reset.*
MDC/EE_MOD	98	I/O_{PU}	EEPROM Size Configuration Pull Up: EEPROM 24Cxx Size greater than 16Kbits Pull Down: EEPROM 24Cxx Size less that or equal to 16Kbit, e.g., 24C16.

6.4. Power and GND Pins

Table 5. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO	67, 96	P	Digital I/O High Voltage Power for SMI, LED, nRESET
DVDDL	20, 21, 22, 23, 73, 74, 75, 76, 77	P	Digital Low Voltage Power
SVDDH	78	AP	RSGMII-Plus High Voltage Power
SVDDL	80, 87, 90	AP	RSGMII-Plus Low Voltage Power
AVDDH	5, 15, 19, 24, 34, 54, 64, 102, 112	AP	Analog High Voltage Power
AVDDL	10, 18, 29, 39, 49, 59, 107, 117, 128	AP	Analog Low Voltage Power
PLLVDD0 PLLVDD1	122 44	AG	PLL Low Voltage Power
AGND	16	AG	Analog GND
SGND	83, 86, 93	SG	RSGMII-Plus GND
GND	EPAD	G	Digital/Analog GND

6.5. Miscellaneous Pins

Table 6. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
MDIREF	17	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
ATESTCK0	123	AO	Reserved for Internal Use. Must be left floating.
SXTALI(25M)	95	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz +/- 50ppm tolerance crystal reference or oscillator input.
SXTALO	94	AO	25MHz Crystal Clock Output Pin. 25MHz +/- 50ppm tolerance crystal output.
SCK	100	I_{PU}	EEPROM SMI Clock. EEPROM interface.
SDA	101	I/O_{PU}	EEPROM SMI Data. EEPROM interface.
MDIO	99	I/O_{PU}	MII Management Interface Data Pin.
MDC	98	O	MII Management Interface Clock Pin.
nRESET	97	I_S	System Pin Reset Input. When low active will reset the RTL8376.
BUZZER	68	O	2KHz signal out when looping is detected
ATEST-1	65	AO	Reserved. Must be left floating for normal operation
RSV	71, 72	I/O_{PU}	Reserved.
ATEST-2	66	AI/O	Reserved. Must be pulled up to DVDDIO via a 4.7K ohm resistor for normal operation.

7. Physical Layer Functional Overview

7.1. MDI Interface

The RTL8376 embeds eight Gigabit Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-Tx, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

7.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

7.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

7.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

7.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.8. Auto-Negotiation for UTP

The RTL8376 obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8376 advertises full capabilities (1000full, 100full, 100half, 10full, 10half) together with flow control ability.

7.9. Crossover Detection and Auto Correction

The RTL8376 automatically determines whether or not it needs to crossover between pairs (see Table 7) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8376 automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 7. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

7.10. Polarity Correction

The RTL8376 automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

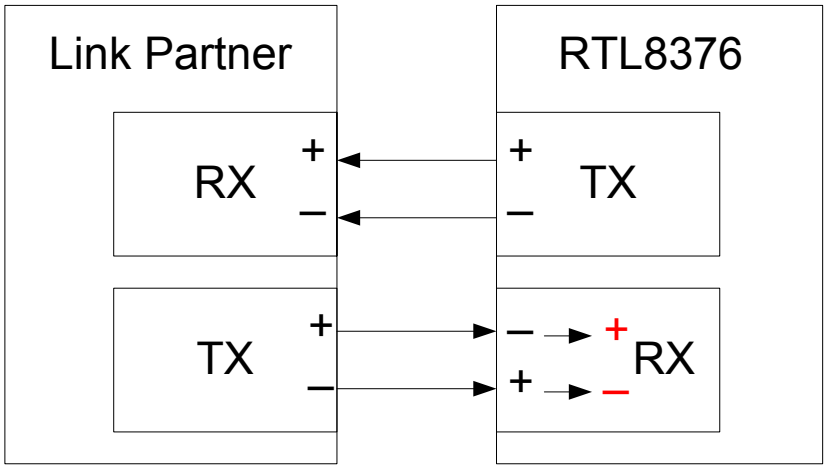


Figure 4. Conceptual Example of Polarity Correction

8. General Function Description

8.1. Reset

8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8376 will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- If EEPROM is detected, autoload the configuration from EEPROM
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU
- 3.3V DVDDH t_{rise} and t_{fall} should be greater than 1ms

8.1.2. Software Reset

The RTL8376 supports two software resets; a chip reset and a soft reset.

8.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

8.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list
2. Restart the auto-negotiation process

8.2. 802.3x Full Duplex Flow Control

The RTL8376 supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on CFG_PHYn_FORCE[6:5] (n: 0~7), CFG_SDS0m_FORCE[6:5] (m: 0-4), CFG_SDS1m_FORCE[6:5] (m: 0~4).

8.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called 'truncated binary exponential backoff'. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

Where:

k = min (n, backoffLimit). The backoffLimit for the RTL8376 is 9 (default).

The half duplex back-off algorithm in the RTL8376 does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

8.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8376 sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. To prevent a partner entering partition status due to over-collisions, the RTL8376 provides an option to receive one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

8.4. Search and Learning

Search

When a packet is received, the RTL8376 uses the destination MAC address and Filtering Identifier (FID) to search the 8K-entry look-up table. The packet will be forwarded to the destination port if the destination MAC address is found in the lookup table. If the destination MAC address is not found, the switch will broadcast the packet.

Learning

The RTL8376 uses the source MAC address and FID of the incoming packet to hash into an 11-bit index. It then compares the source MAC address with the data (MAC address) in this index. If there is a match with one of the entries, the RTL8376 will update the entry with new information. If there is no match and the 8K entries are not all occupied by other MAC addresses, the RTL8376 will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

The RTL8376 supports a 64-entry Content Addressable Memory (CAM) to avoid look-up table hash collisions. When all 8K entries in the look-up table index are occupied, the source MAC address can be learned into the 64-entry CAM. If both the look-up table and the CAM are full, the source MAC address will not be learned in the RTL8376.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8376 is between 200 and 400 seconds (typical is 300 seconds).

8.5. SVL and IVL/SVL

The RTL8376 supports Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured into different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

8.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8376. The maximum packet length may be set to 1522, 1536, 1552, or 16K bytes.

8.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8376 supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered. MAC address 01-80-C2-00-00-03 is always forwarded.

8.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8376 supports 3 types of broadcast storm control mechanism to suppress packet flooding. After the threshold of receiving broadcast/multicast/unknown DA packets is triggered at the enabled port within a reference period, all other broadcast/multicast/unknown DA packets will be dropped.

8.9. MIB Counters

The RTL8376 supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

8.10. Port Mirroring

The RTL8376 supports one set of port mirroring functions for all ports. The TX, RX, or both TX/RX packets of the source port can be monitored from a mirror port.

8.11. VLAN Function

The RTL8376 supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Supports ingress filtering and egress filtering options provide flexible VLAN configuration:

Ingress Filtering

- The Acceptable Frame Type of the Ingress Process can be set to 'Admit All' or 'Admit All Tagged'.
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set.

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains.
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains.

The VLAN tag can be inserted or removed at the output port. The RTL8376 will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames.

8.11.1. Port-Based VLAN

This VLAN function can be configured via an attached serial EEPROM or EEPROM SMI Slave interface. The 4K-entry VLAN Table designed into the RTL8376 provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

8.11.2. IEEE 802.1Q Tag-based VLAN

The RTL8376 supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8376 uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8376 compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8376 performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8376 performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when '802.1Q tag aware VLAN' is enabled is illustrated in Figure 5, page 19.

Two VLAN ingress filtering functions are supported in registers by the RTL8376. One is the 'VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering', which will drop frames if the ingress port is not in the member set.

There are egress filtering could be set. ‘Reserved Multicast Address, leaky VLAN’ are supported by the RTL8376 via register access.

8.11.3. Port and Protocol-Based VLAN

The RTL8376 supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 5. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be ‘Ethernet’ and value to be ‘0x0800’. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

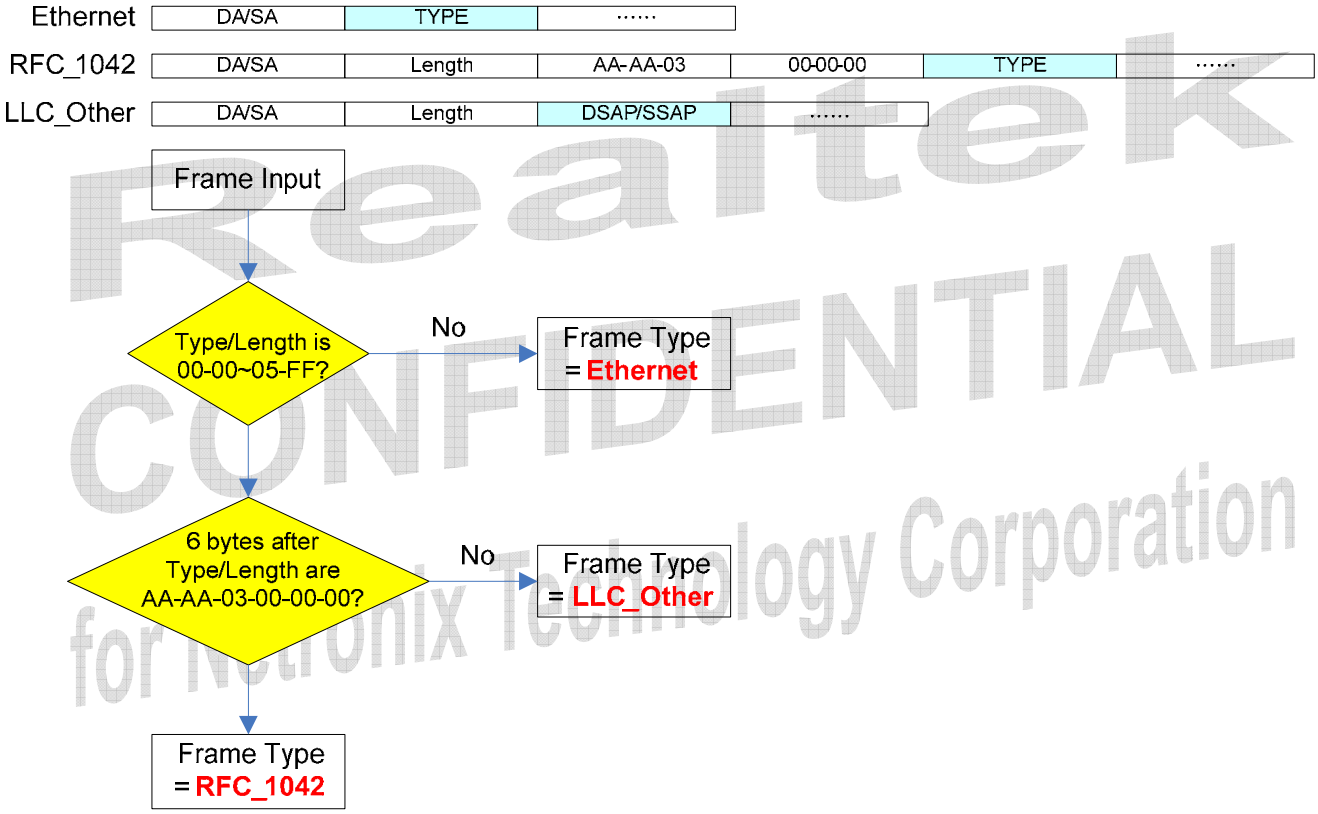


Figure 5. Protocol-Based VLAN Frame Format and Flow Chart

8.11.4. Port VID

The RTL8376 supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL8376 will drop non-tagged packets and packets with an incorrect PVID.

8.12. QoS Function

The RTL8376 supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8376, the packet's priority will be assigned based on the priority selection table.

Leaky buckets for Average Packet Rate. Each queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

8.12.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on flow control status. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

8.12.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8376 can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8376 identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority

8.12.3. Priority Queue Scheduling

The RTL8376 supports MAX-MIN packet scheduling.

Packet scheduling offers three modes:

- Type I leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 6 shows the RTL8376 packet-scheduling diagram.

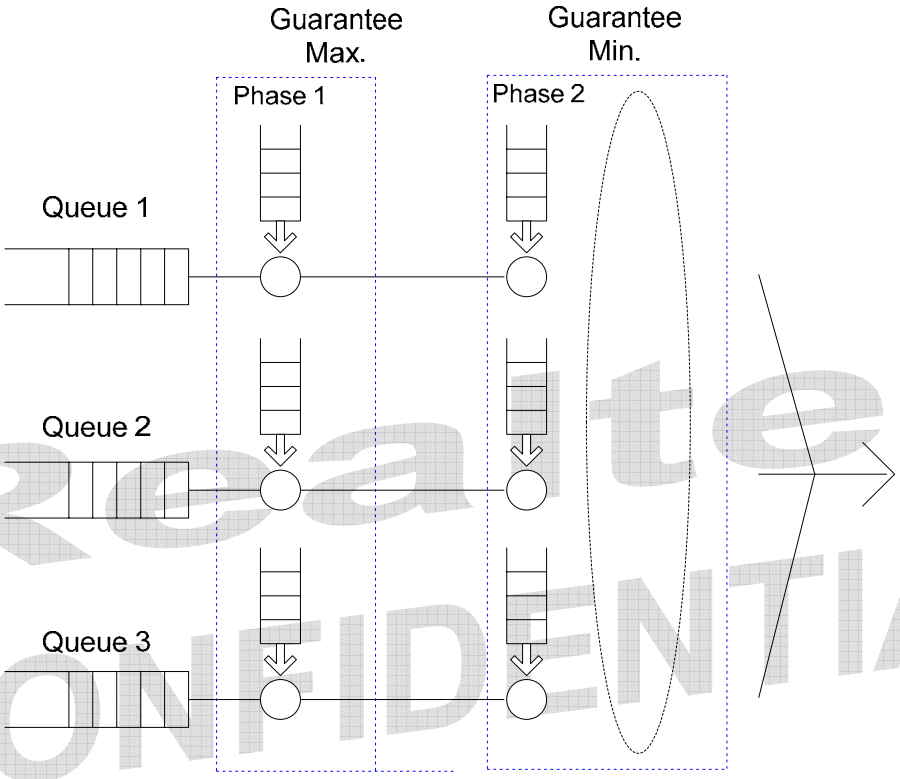


Figure 6. RTL8376 MAX-MIN Scheduling Diagram

8.12.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8376 supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. Each output queue has a 3-bit 802.1p/Q, and a 6-bit IP DSCP value configuration register.

8.12.5. ACL-Based Priority

The RTL8376 supports 64-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule).
- If the action bit is 'Permit', ACL rules will override other rules.

- If the action bit is ‘Mirror’, the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism.
- The priority bit will take effect only if the action bit is ‘CPU’, ‘Permit’, and ‘Mirror’. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism.

8.13. Pre-IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL8376 supports pre-IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T and 100base-TX in full duplex operation, and supports 10Base-Te for 10Base-T in full/half mode.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) Sublayer with 100Base-T and 1000base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T PHY, the RTL8376 supports Energy Efficient Ethernet with the optional function of Low Power Idle.
- For 100Base-TX PHY, the RTL8376 supports Energy Efficient Ethernet with the optional function of Low Power Idle.
- For 10Base-T, IEEE defines a 10Mbps PHY (10Base-Te) with reduced transmit amplitude requirements. 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of Class-D (Cat-5) cable.

The RTL8376 MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

8.14. Realtek Cable Test (RTCT)

The RTL8376 physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open, or impedance mismatch in each differential pair. The RTL8376 also provides LED support to indicate test status and results.

8.15. LED Indicator

The RTL8376 supports MDIO LED mode. Each port has three LED indicator bits. Each bit may have different indicator meanings set by register configuration. Upon reset, the RTL8376 supports chip diagnostics and LED operation test by blinking all LEDs once. This function can be disabled by EEPROM configuration.

There are 3 LED indicator bits for each port:

- LED0 can be configured by LED0_CFG[3:0]
- LED1 can be configured by LED1_CFG[3:0]
- LED2 can be configured by LED2_CFG[3:0] via EEPROM

For MDIO LED Mode, the RTL8376 will send the LED data to an external LED display IC (e.g., RTL8231) via the MDIO interface. The RTL8231 supports 3 single-color LEDs in SCAN mode, and can combine the Pn_LED0 and Pn_LED1 as a Bi-color LED in SCAN LED mode via a pin strapping option. See Figure 7, page 23 for 3 Single-Color LED per port application diagram; Figure 8, page 24 for one single and one Bi-Color LED per port application diagram.

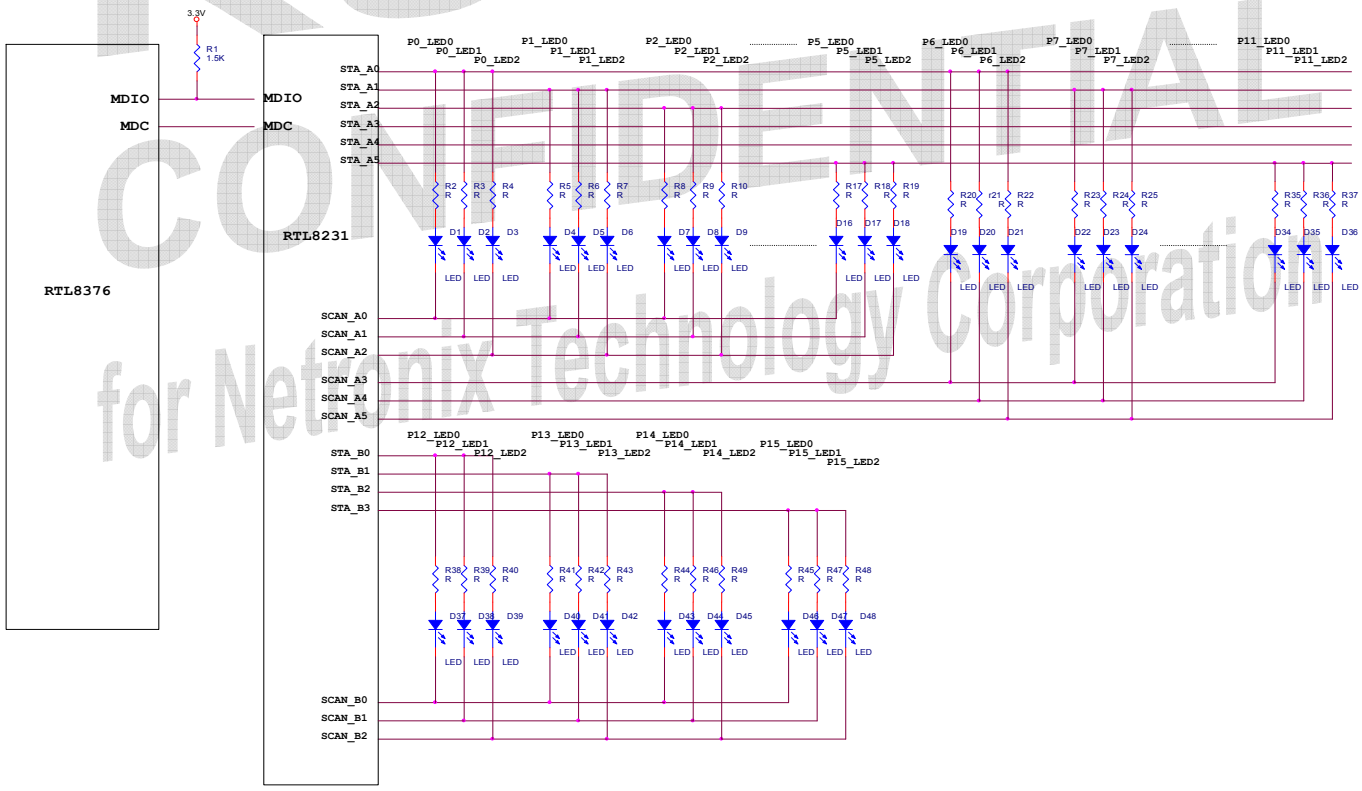


Figure 7. RTL8376+RTL8231 for Single-Color LED

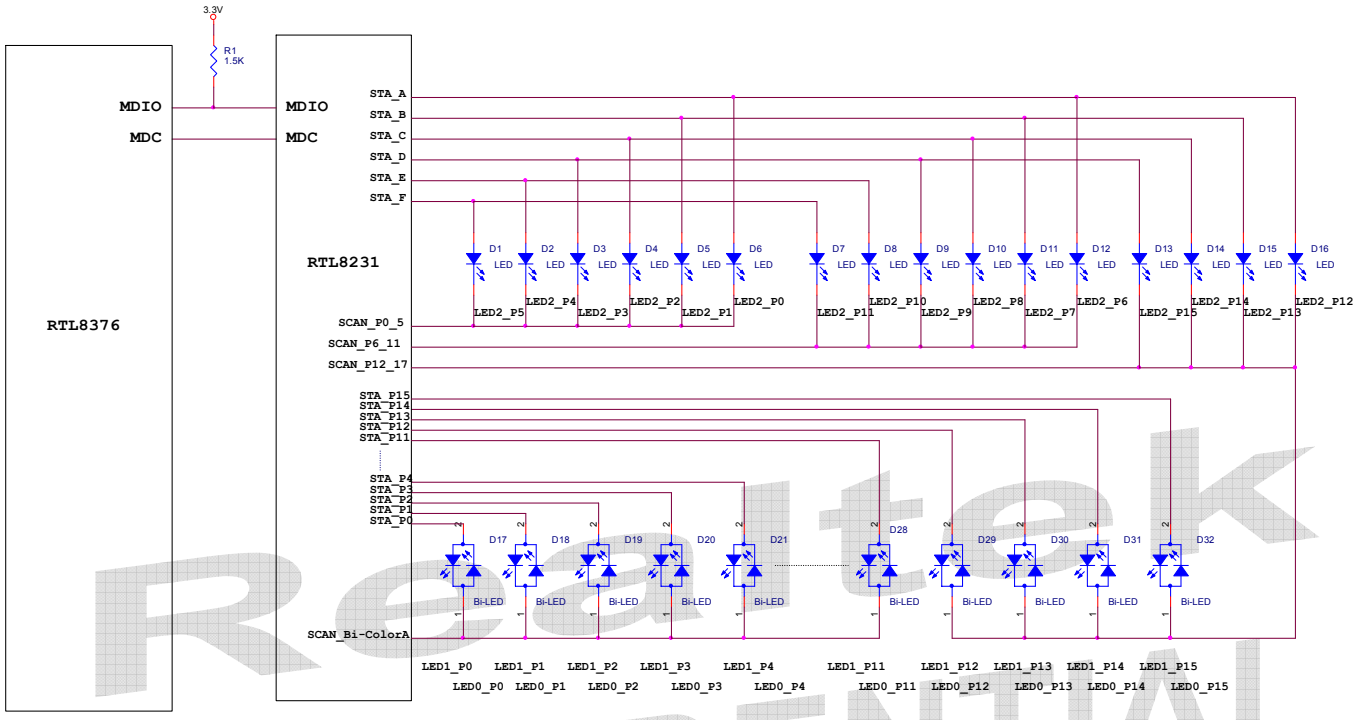


Figure 8. RTL8376+RTL8231 for One Single and One Bi-Color LED

8.16. Green Ethernet

8.16.1. Link-On and Cable Length Power Saving

The RTL8376 provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

8.16.2. Link-Down Power Saving

The RTL8376 implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

9. Interface Descriptions

9.1. EEPROM SMI Host to EEPROM

The EEPROM interface of the RTL8376 uses the serial bus EEPROM Serial Management Interface (SMI) to read the EEPROM (24LCXX), and the RTL8376 provides 8-bit/16-bit address mode selection via a strapping option pin. When the RTL8376 is powered up, it drives SCK and SDA to read the registers (see Figure 9 and Figure 10. Also see Figure 11, page 26 for 8-bit mode, and Figure 12, page 26 for 16-bit mode EEPROM).

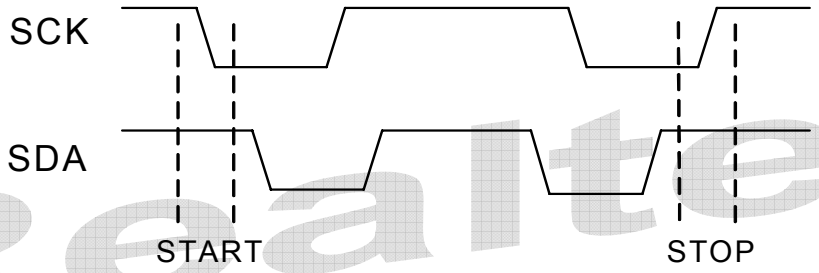


Figure 9. SMI Start and Stop Command

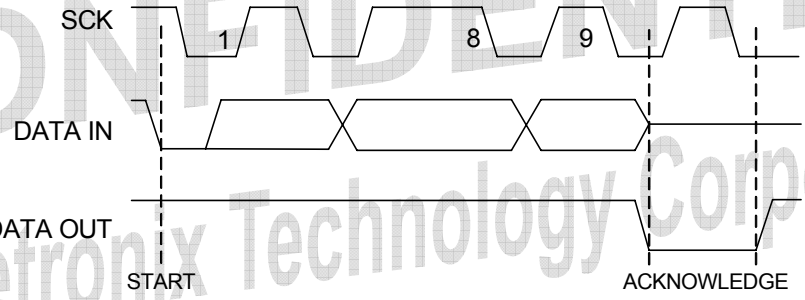


Figure 10. EEPROM SMI Host to EEPROM

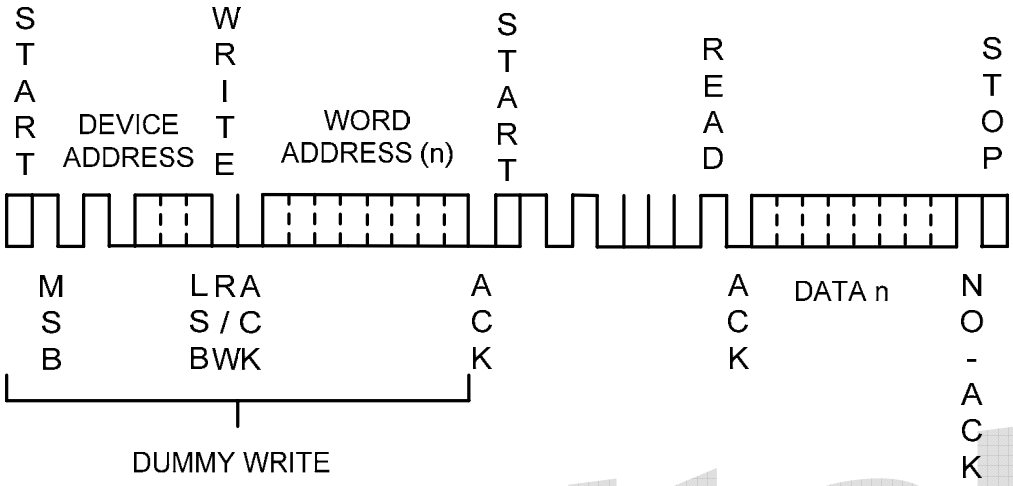


Figure 11. 8-Bit Address EEPROM Sequential Read

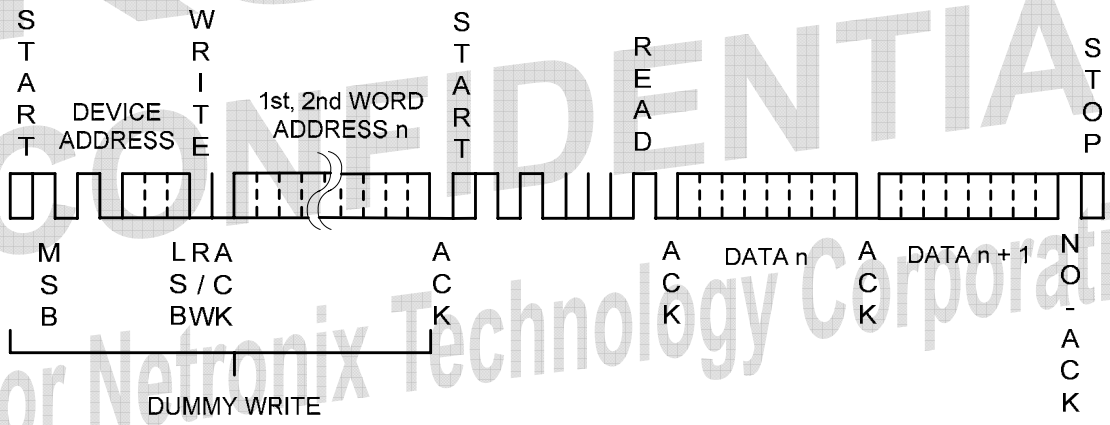


Figure 12. 16-Bit Address EEPROM Sequential Read

9.2. EEPROM SMI Slave for External CPU

When EEPROM auto-load is complete, the RTL8376 registers can be accessed via SCK and SDA via an external CPU. The device address of the RTL8376 is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

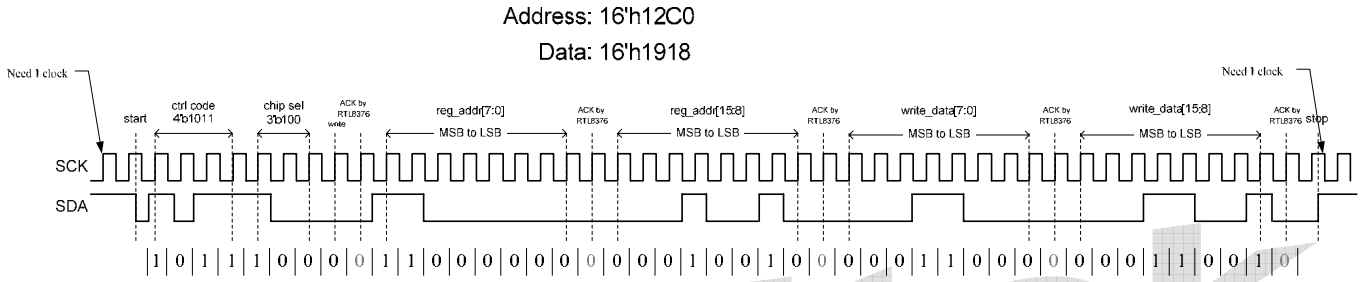


Figure 13. EEPROM SMI Write Command for Slave Mode

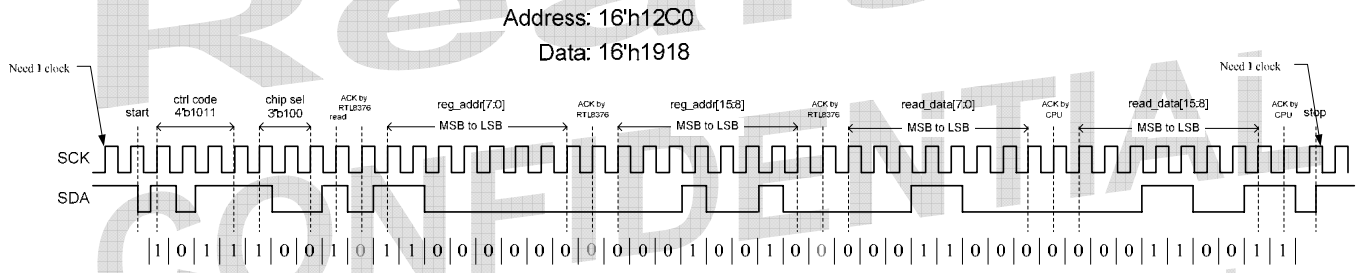


Figure 14. EEPROM SMI Read Command for Slave Mode

9.3. Media Independent Interface Management (MIIM)

The RLT8376 uses an Media Independent Interface Management (MIIM) via MDC and MDIO signals to poll the MII register of the external PHY. The polled PHY addresses are in MIIM frame format.

Table 8. MIIM (MDC/MDIO) Frame Format

	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	Z0	D_{15}…….D_0	Z*
Write	1……..1	01	01	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	10	D_{15}…….D_0	Z*

9.4. Reduced Serial GMII - Plus (RSGMII-Plus) Interface

To reduce PCB complexity and IC pin count, the RTL8376 offers a proprietary interface; the Realtek Reduced Serial Gigabit Media Independent Interface. This innovative 5Gbps serial interface provides an up to 5-inch long MAC to PHY communication path. The RSGMII-Plus can carry the full duplex gigabit Ethernet data streams of two ports simultaneously, and recover clock from the data rather than use a dedicated clock.

The RSGMII-Plus reduces the interconnection between the gigabit Ethernet PHY and MAC to only 5 pins. Figure 15 depicts the RSGMII-Plus interconnection. The MAC side uses a TX+/- pair to transmit 5Gbps data to the PHY side via AC coupling (0.1µF). At the same time, the MAC side uses the RX+/- pair to receive 5Gbps data from the PHY side via AC coupling (0.1µF).

In order to save a crystal circuit on the PHY side, the MAC provides an SVDDH voltage level peak-to-peak 25MHz square wave TXCLK for the PHY as system clock input.

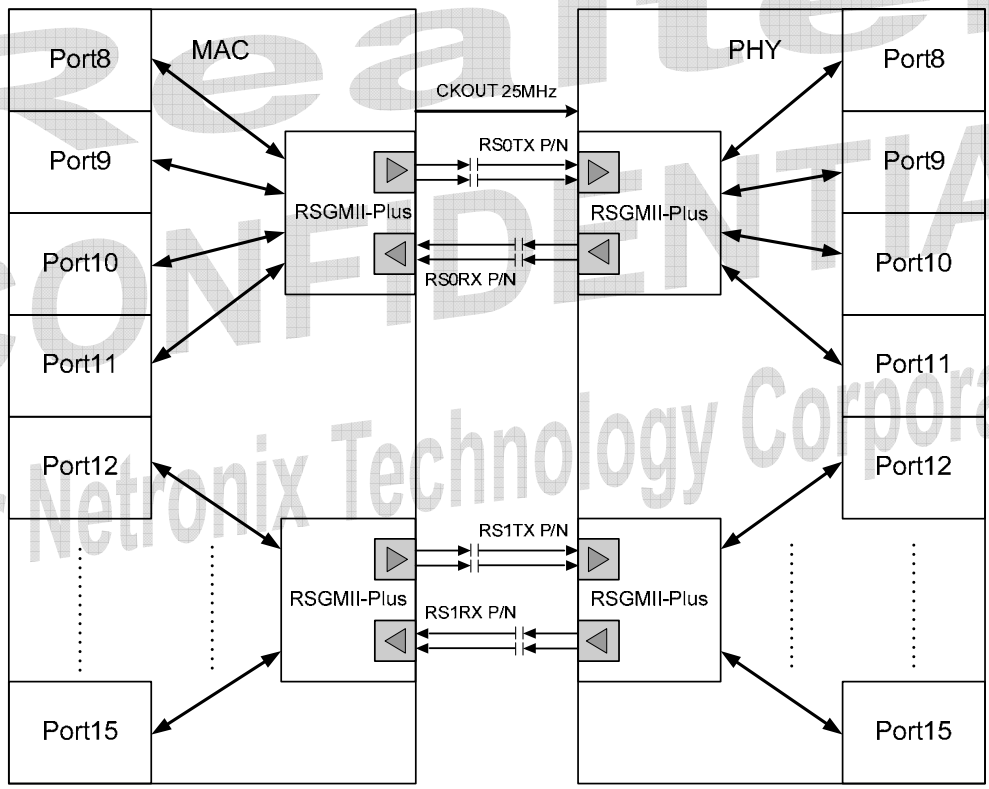


Figure 15. RSGMII-Plus Interconnection Diagram

The RSGMII-Plus interface runs at 5Gbps in 10/100/1000Mbps modes. As a 5Gbps data rate is excessive for interfaces operating at 10/100Mbps, when operating in these conditions the interface elongates each byte of data by 10 times for 100Mbps, and by 100 times for 10Mbps, through a rate adaptation block.

The data paths and all associated control signals are transmitted from each port and recovered at the receiver side via proprietary transmission encode/decode and Serial/De-serial translation. The same method applies to the transmit side.

10. Register Descriptions

In this section the following abbreviations are used:

RO: Read Only
RW: Read/Write
LL: Latch Low until clear
LH: Latch High until clear
SC: Self Clearing

10.1. Page 0: PCS Register (PHY 0~7)

Table 9. Page 0: PCS Register (PHY 0~7)

Name	Page	Register	Register Description	Default
PHY 0~3 Register	0	0	Control Register	0x1140
		1	Status Register	0x7949
		2	PHY Identifier 1	0x001C
		3	PHY Identifier 2	0xC918
		4	Auto-Negotiation Advertisement Register	0x05E1
		5	Auto-Negotiation Link Partner Ability Register	0x0000
		6	Auto-Negotiation Expansion Register	0x0004
		7	Auto-Negotiation Page Transmit Register	0x2001
		8	Auto-Negotiation Link Partner Next Page Register	0x0000
		9	1000Base-T Control Register	0x0E00
		10	1000Base-T Status Register	0x0000
		11	Reserved	0x0000
		12	Reserved	0x0000
		13	Reserved	0x0000
		14	Reserved	0x0000
		15	Extended Status	0x2000
		16~31	ASIC Control Register	-

10.2. Register 0: Control

Table 10. Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1: PHY reset 0: Normal operation This bit is self-clearing.	0
0.14	Loopback (Digital loopback)	RW	1: Enable loopback This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex, 100Base-TX full duplex, or 1000Base-T full duplex.	0
0.13	Speed Selection[0]	RW	[0.6,0.13] Speed Selection[1:0] 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps This bit can be set through SMI (Read/Write).	0
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	1
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from GMII. PHY is still able to respond to MDC/MDIO 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation This bit can be set through SMI (Read/Write).	1
0.7	Collision Test	RO	1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.	0
0.6	Speed Selection[1]	RW	See bit 13	1
0.[5:0]	Reserved	RO	Reserved	000000

10.3. Register 1: Status

Table 11. Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base-T4	RO	0: Not 100Base-T4 capable The RTL8376 does not support 100Base-T4 mode and this bit should always be 0.	0
1.14	100Base-TX-FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base-TX-HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base-T-FD	RO	1: 10Base-T full duplex capable 0: Not 10Base-TX full duplex capable	1
1.11	10Base-T-HD	RO	1: 10Base-T half duplex capable 0: Not 10Base-TX half duplex capable	1
1.10	100Base-T2-FD	RO	0: Not 100Base-T2 full duplex capable The RTL8376 does not support 100Base-T2 mode and this bit should always be 0.	0
1.9	100Base-T2-HD	RO	0: Not 100Base-T2 half duplex capable The RTL8376 does not support 100Base-T2 mode and this bit should always be 0.	0
1.8	Extended Status	RO	1: Extended status information in Register 15 The RTL8376 always supports Extended Status Registers.	1
1.7	Reserved	RO	Reserved	0
1.6	MF Preamble Suppression	RO	The RTL8376 will accept management frames with preamble suppressed	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/LH	1: Remote fault condition detected 0: No remote fault detected This bit will remain set until it is cleared by reading register 1 via the management interface.	0
1.3	Auto-Negotiation Ability	RO	1: Auto-negotiation capable (permanently=1)	1
1.2	Link Status	RO/LL	1: Link is established. If the link fails, this bit will be 0 until after reading this bit again 0: Link has failed since previous read If the link fails, this bit will be set to 0 until bit is read.	0
1.1	Jabber Detect	RO/LH	1: Jabber detected 0: No Jabber detected Jabber is supported only in 10Base-T mode.	0
1.0	Extended Capability	RO	1: Extended register capable (permanently=1)	1

10.4. Register 2: PHY Identifier 1

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number, and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 12. Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th Bits of the Organizationally Unique Identifier (OUI), Respectively	0x001C

10.5. Register 3: PHY Identifier 2

Table 13. Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th Bits of the OUI	110010
3.[9:4]	Model Number	RO	Manufacturer's Model Number (18: Indicates 10/100/1000M 8 port)	011000
3.[3:0]	Revision Number	RO	Manufacturer's Revision Number (00: Indicates S)	0001

10.6. Register 4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device as they will be transmitted to its Link Partner during Auto-negotiation.

Note: Each time the link ability of the RTL8376 is reconfigured, the auto-negotiation process should be executed to allow the configuration to take effect.

Table 14. Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Additional next pages exchange desired 0: No additional next pages exchange desired	0
4.14	Acknowledge	RO	Permanently=0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8376 has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved	0
4.11	Reserved	RW	1: Advertises that the RTL8376 has asymmetric flow control capability 0: No asymmetric flow control capability	1
4.10	Pause	RW	1: Advertises that the RTL8376 has flow control capability 0: No flow control capability	1
4.9	100Base-T4	RO	1: 100Base-T4 capable 0: Not 100Base-T4 capable (Permanently=0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1

Reg.bit	Name	Mode	Description	Default
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

Note 1: The setting of Register 4 has no effect unless auto-negotiation is restarted or the link goes down.
Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted.

10.7. Register 5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after a successful Auto-negotiation.

Table 15. Register 5: Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Reserved	0
5.11	Asymmetric Pause	RO	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability	0
5.10	Pause	RO	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner	0
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00000

10.8. Register 6: Auto-Negotiation Expansion

Table 16. Register 6: Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:5]	Reserved	RO	Ignore on Read	0
6.4	Parallel Detection Fault	RO/LH	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
6.3	Link Partner Next Page Ability	RO	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	0
6.2	Local Next Page Ability	RO	Not Supported Permanently=0	1
6.1	Page Received	RO/LH	1: A New Page has been received 0: A New Page has not been received	0
6.0	Link Partner Auto-Negotiation Ability	RO	If Auto-Negotiation is enabled, this bit means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	0

10.9. Register 7: Auto-Negotiation Page Transmit Register

Table 17. Register 7: Auto-Negotiation Page Transmit Register

Reg.bit	Name	Mode	Description	Default
7.15	Next Page	RW	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
7.14	Reserved	RO	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
7.13	Message Page	RW	1: Message page 0: No Message page ability	1
7.12	Acknowledge 2	RW	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	0
7.11	Toggle	RO	Toggle Bit	0
7.[10:0]	Message/ Unformatted Field	RW	Content of Message/Unformatted Page	1

10.10. Register 8: Auto-Negotiation Link Partner Next Page Register

Table 18. Register 8: Auto-Negotiation Link Partner Next Page Register

Reg.bit	Name	Mode	Description	Default
8.15	Next Page	RO	Received Link Code Word Bit 15	0
8.14	Acknowledge	RO	Received Link Code Word Bit 14	0
8.13	Message Page	RO	Received Link Code Word Bit 13	0
8.12	Acknowledge 2	RO	Received Link Code Word Bit 12	0
8.11	Toggle	RO	Received Link Code Word Bit 11	0
8.[10:0]	Message/Unformatted Field	RO	Received Link Code Word Bit 10:0	0

10.11. Register 9: 1000Base-T Control Register

Table 19. Register 9: 1000Base-T Control Register

Reg.bit	Name	Mode	Description	Default
9.[15:13]	Test Mode	RW	Test Mode Select 000: Normal mode 001: Test mode 1 – Transmit waveform test 010: Test mode 2 – Transmit jitter test in MASTER mode 011: Test mode 3 – Transmit jitter test in SLAVE mode 100: Test mode 4 – Transmitter distortion test 101,110, 111: Reserved	000
9.12	MASTER/SLAVE Manual Configuration Enable	RW	1: Enable MASTER/SLAVE manual configuration 0: Disable MASTER/SLAVE manual configuration	0
9.11	MASTER/SLAVE Configuration Value	RW	1: Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one 0: Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one	1
9.10	Port Type	RW	1: Multi-port device 0: Single-port device	1
9.9	1000Base-T Full Duplex	RW	1: Advertise PHY is 1000Base-T full duplex capable 0: Advertise PHY is not 1000Base-T full duplex capable	1
9.8	1000Base-T Half Duplex	RW	1: Advertise PHY is 1000Base-T half duplex capable 0: Advertise PHY is not 1000Base-T half duplex capable	0
9.[7:0]	Reserved	RW	Reserved	0

10.12. Register 10: 1000Base-T Status Register

Table 20. Register 10: 1000Base-T Status Register

Reg.bit	Name	Mode	Description	Default
10.15	MASTER/SLAVE Configuration Fault	RO/LH/SC	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected	0
10.14	MASTER/SLAVE Configuration Resolution	RO	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	0
10.13	Local Receiver Status	RO	1: Local receiver OK 0: Local receiver not OK	0
10.12	Remote Receiver Status	RO	1: Remote receiver OK 0: Remote receiver not OK	0
10.11	Link Partner 1000Base-T Full Duplex	RO	1: Link partner is capable of 1000Base-T full duplex 0: Link partner is not capable of 1000Base-T full duplex	0
10.10	1000Base-T Half Duplex	RO	1: Link partner is capable of 1000Base-T half duplex 0: Link partner is not capable of 1000Base-T half duplex	0
10.[9:8]	Reserved	RO	Reserved	0
10.[7:0]	Idle Error Count	RO/SC	Idle Error Counter The counter stops automatically when it reaches 0xFF	0

10.13. Register 15: Extended Status

Table 21. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
15.15	1000Base-X Full Duplex	RO	1: 1000Base-X full duplex capable 0: Not 1000Base-X full duplex capable	0
15.14	1000Base-X Half Duplex	RO	1: 1000Base-X half duplex capable 0: Not 1000Base-X half duplex capable	0
15.13	1000Base-T Full Duplex	RO	1: 1000Base-T full duplex capable 0: Not 1000Base-T full duplex capable	1
15.12	1000Base-T Half Duplex	RO	1: 1000Base-T half duplex capable 0: Not 1000Base-T half duplex capable	0
15.[11:0]	Reserved	RO	Reserved	0

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 22. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-10	+125	°C
DVDDIO, AVDDH, SVDDH Supply Referenced to DGND, AGND, and SGND	GND-0.3	+3.63	V
DVDDL, AVDDL, SVDDL, PLLVDD Supply Referenced to GND, AGND, and SGND	GND-0.3	+1.32	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

11.2. Recommended Operating Range

Table 23. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
DVDDIO, AVDDH, SVDDH Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL, SVDDL, SVDDT, PLLVDDL Supply Voltage Range	0.95	1.0	1.05	V

11.3. Thermal Characteristics

11.3.1. Assembly Description

Table 24. Assembly Description

Package	Type	E-Pad LQFP128
	Dimension (L x W)	14x20 (mm^2)
	Thickness	1.4 (mm)
PCB	PCB Dimension (L x W)	162x110 (mm^2)
	PCB Thickness	1.6 (mm)
	Number of Cu Layer-PCB	2 Layer

11.3.2. Material Properties

Table 25. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	1.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.79
PCB		Cu	400
		FR4	0.2
External		Al	180
		EG-150	0.9

11.3.3. Simulation Conditions

Table 26. Simulation Conditions

Input Power	3.10W
Test Board (PCB)	2L (2S) / 4L (2S2P)
Control Condition	Air Flow = 0, 1, 2m/s

11.3.4. Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convection

Table 27. Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convection

	θ_{JA}	θ_{JC}	Ψ_{JT}	Ψ_{JB}
4L PCB	14.5	6.7	1.9	7.3
2L PCB	25.3	8.1	2.3	9.8

11.3.5. Thermal Performance of E-Pad LQFP-128 on PCB under Forced Convection

Table 28. Thermal Performance of E-Pad LQFP-128 on PCB under Forced Convection

	Air Flow (m/s)	0	1	2
4L PCB without HS	θ_{JA}	14.5	12.1	11.3
	Ψ_{JT}	1.9	2.1	2.6
	Ψ_{JB}	7.3	7.1	6.8
2L PCB with External HS	θ_{JA}	25.3	21.8	20.4
	Ψ_{JT}	2.3	2.6	3.1
	Ψ_{JB}	9.8	9.5	9.3

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JB} : Junction to board thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JT}: Junction to top center of package thermal characterization
Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

11.3.6. DC Characteristics

Table 29. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
System Idle (No UTP Port Linked Up)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	87	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	525	-	mA
Total Power Consumption for All Ports	PS	-	812.1	-	mW
1000M Active (Does not include LED Power)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	398	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	1697	-	mA
Total Power Consumption for All Ports	PS	-	3010.4	-	mW
100M Active (Does not include LED Power)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	269	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	697	-	mA
Total Power Consumption for All Ports	PS	-	1584.7	-	mW
10M Active (Does not include LED Power)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}, I_{SVDDH}	-	473	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	546	-	mA
Total Power Consumption for All Ports	PS	-	2106.9	-	mW
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	2.0	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.8	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V

Note: DVDDIO=3.3V, AVDDH=3.3V, SVDDH=3.3V, DVDDL=1.05V, AVDDL=1.05V, SVDDL=1.05V, SVDDT=1.05V.

11.4. AC Characteristics

11.4.1. EEPROM SMI Host Mode Timing Characteristics

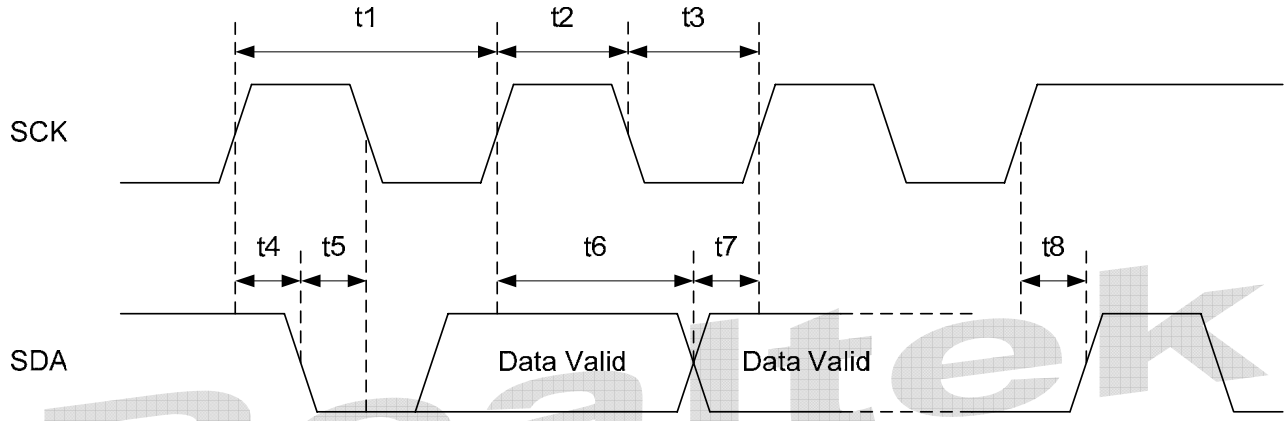


Figure 16. EEPROM SMI Host Mode Timing Characteristics

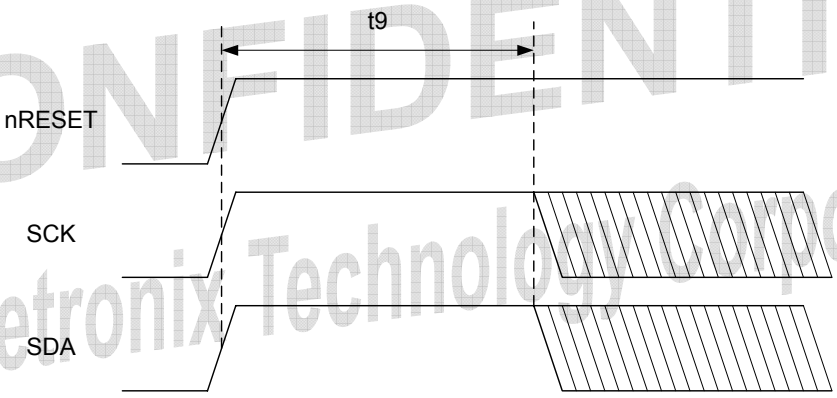


Figure 17. SCK/SDA Power on Timing

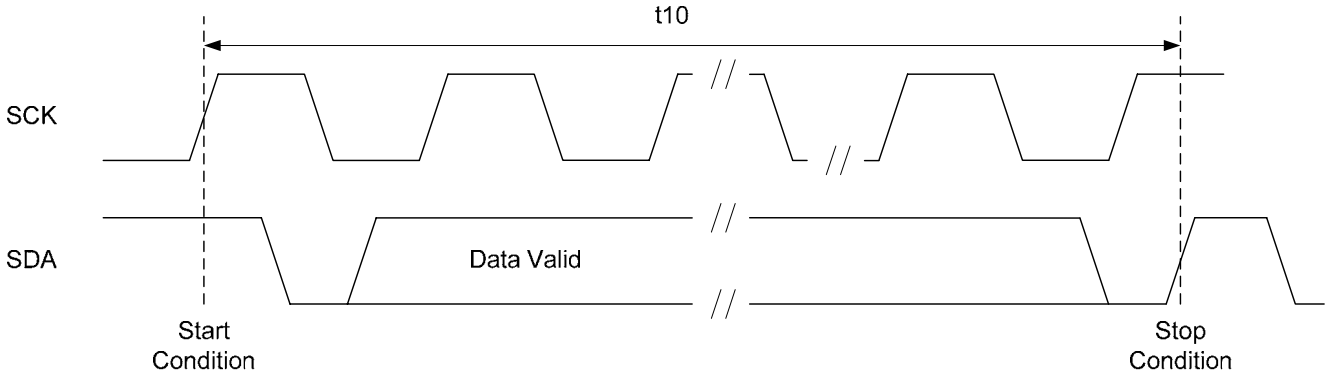


Figure 18. EEPROM Auto-Load Timing

Table 30. EEPROM SMI Host Mode Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
t1	SCK Clock Period	-	5.04	-	µs
t2	SCK High Time	0.6	2.48	-	µs
t3	SCK Low Time	1.2	2.56	-	µs
t4	START Condition Setup Time	0.6	2.52	-	µs
t5	START Condition Hold Time	0.6	2.48	-	µs
t6	Data Hold Time	0	-	-	µs
t7	Data Setup Time	100	-	-	µs
t8	STOP Condition Setup Time	0.6	2.56	-	µs
t9	SCK/SDA Active from Reset Ready	-	92	-	ms
t10	8K-bits EEPROM Auto-Load Time	-	260	-	ms
-	SCK Rise Time (10% to 90%)	-	1.0	-	ns
-	SCK Fall Time (10% to 90%)	-	1.087	-	ns
-	Duty Cycle	-	50	-	%

11.4.2. EEPROM SMI Slave Mode Timing Characteristics

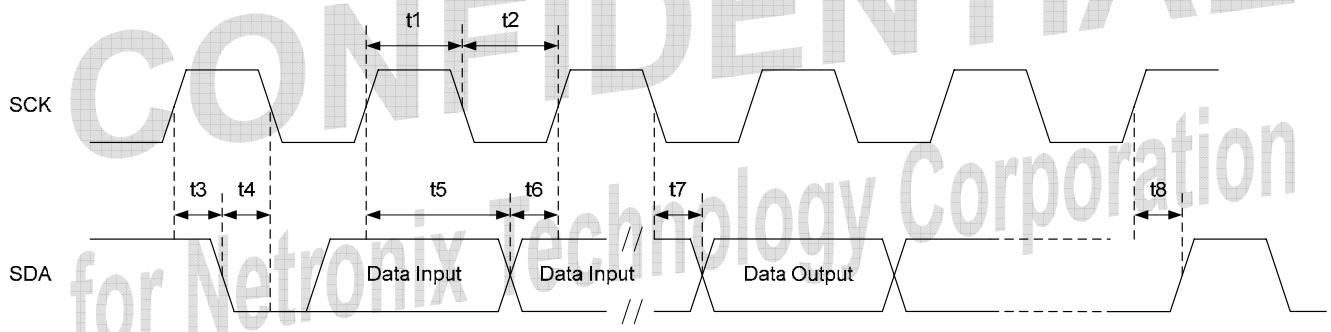


Figure 19. EEPROM SMI Slave Mode Timing Characteristics

Table 31. EEPROM SMI Slave Mode Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
t1	SCK High Time	I	4	-	-	µs
t2	SCK Low Time	I	4	-	-	µs
t3	START Condition Setup Time	I	4	-	-	µs
t4	START Condition Hold Time	I	4	-	-	µs
t5	Data Hold Time	I	5	-	-	µs
t6	Data Setup Time	I	250	-	-	ns
t7	Clock to Data Output Delay	O	-	10	-	ns
t8	STOP Condition Setup Time	I	4	-	-	µs

11.4.3. MIIM (MDC/MDIO) Timing Characteristics

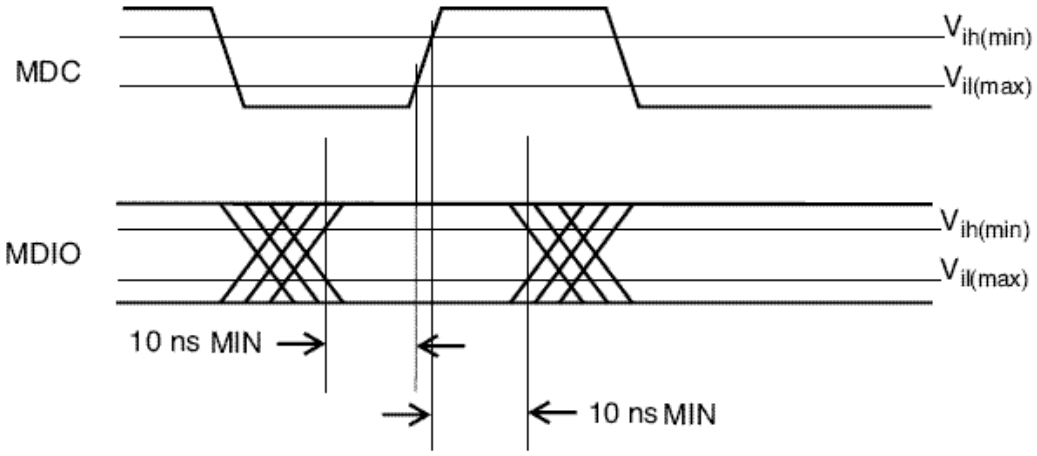


Figure 20. MDIO Sourced by MAC

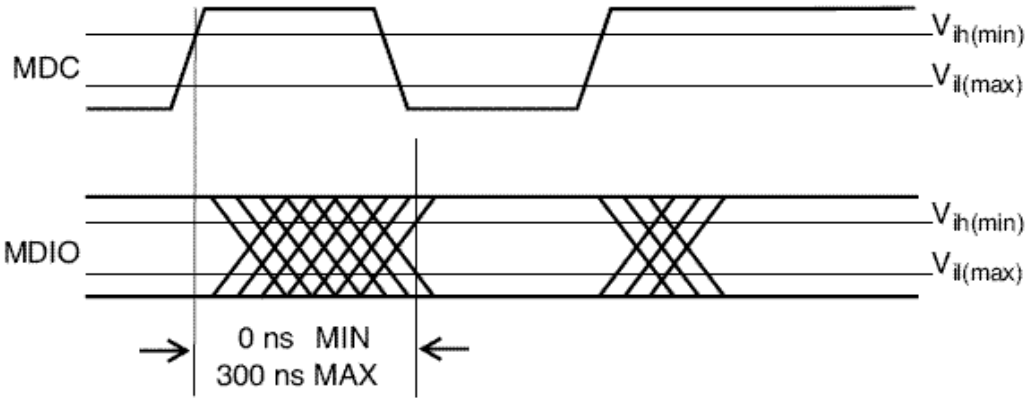


Figure 21. MDIO Sourced by PHY

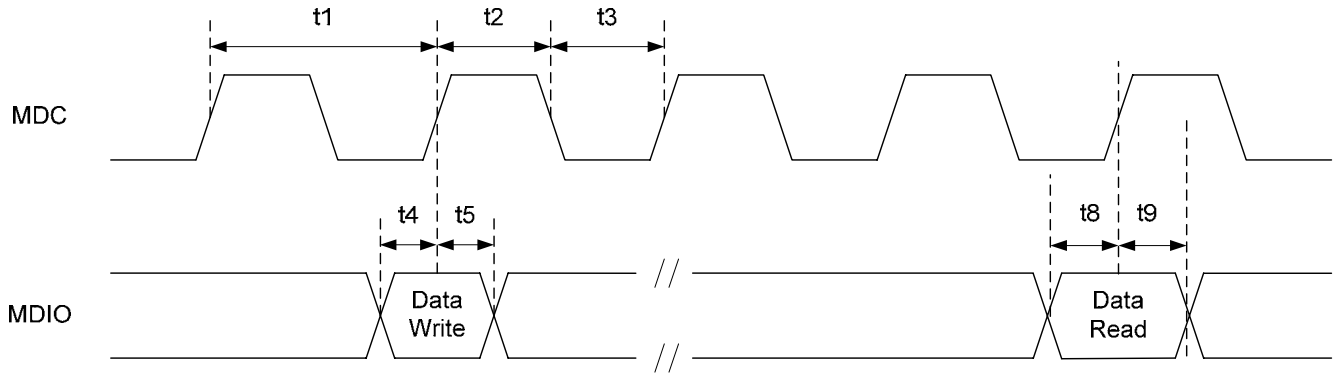


Figure 22. MIIM (MDC/MDIO) Timing Characteristics

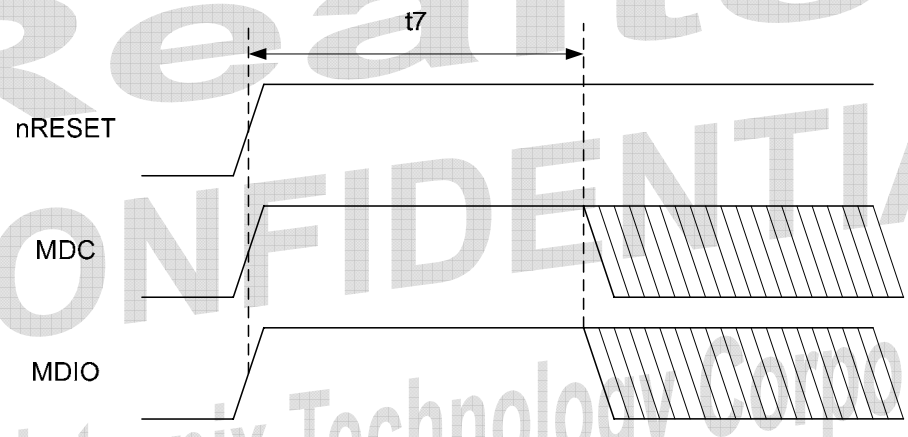


Figure 23. MIIM (MDC/MDIO) Power-On Timing

Table 32. MIIM (MDC/MDIO) Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
t1	MDC Clock Period	O	400	996	-	ns
t2	MDC High Time	O	200	500	-	ns
t3	MDC Low Time	O	200	500	-	ns
t4	MDIO to MDC Rising Setup Time (Write Data)	O	50	324	-	ns
t5	MDIO to MDC Rising Hold Time (Write Data)	O	50	504	-	ns
t7	MDC/MDIO Active from nRESET	O	-	70	-	ms
t8	MDIO to MDC Rising Setup Time (Read Data)	I	14	-	-	ns
t9	MDIO to MDC Rising Hold Time (Read Data)	I	0	-	-	ns
-	MDC Rise Time (10% to 90%)	O	-	1.3	-	ns
-	MDC Fall Time (10% to 90%)	O	-	1.4	-	ns
-	Duty Cycle	O	-	50	-	%

11.5. Reset Characteristics

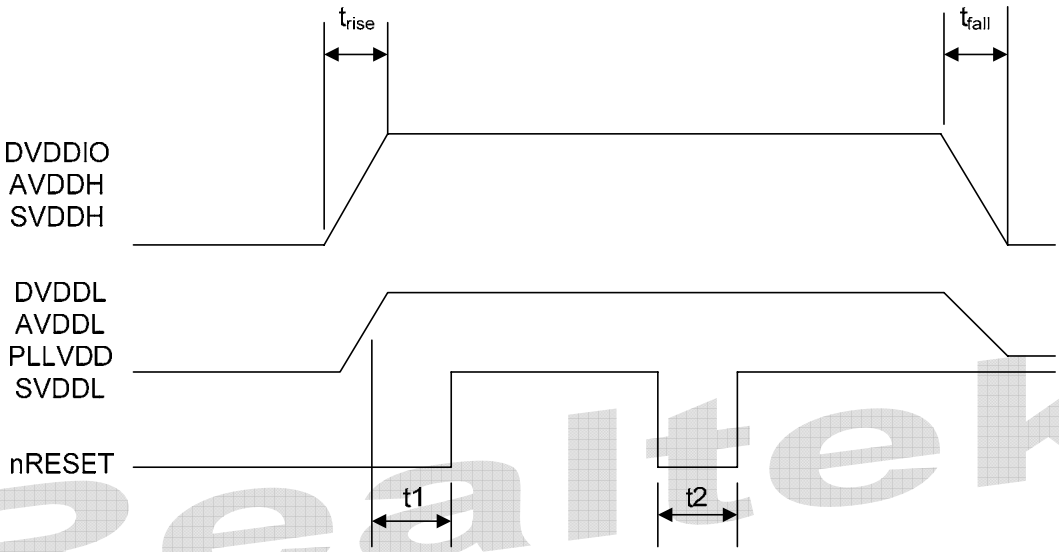
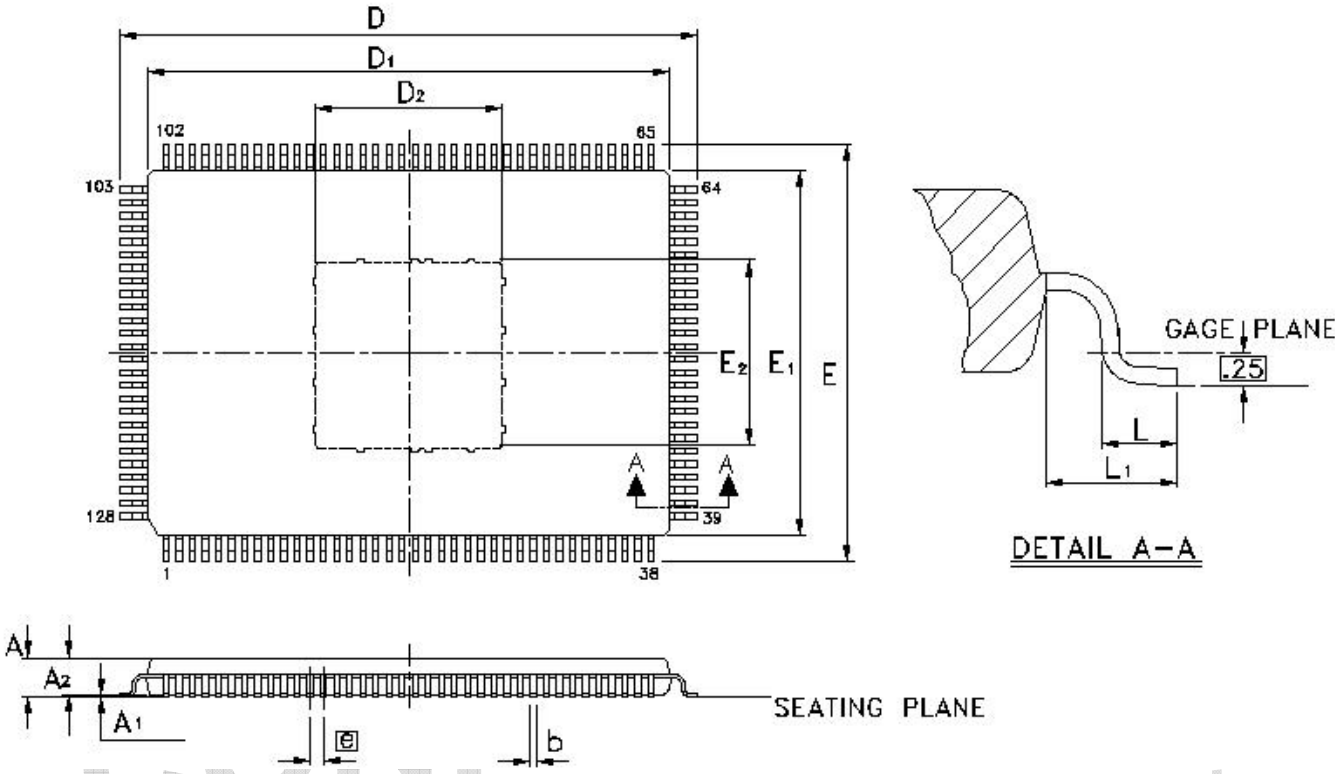


Figure 24. Reset Characteristics

Table 33. Reset Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
t1	Reset Delay	I	10	-	-	ms
t2	Reset Low	I	10	-	-	ms
t_{rise}	Power Rise Slope Time	P	1	-	-	ms
t_{fall}	Power Fall Slope Time	P	1	-	-	ms

12. Mechanical Dimensions



12.1. Mechanical Dimensions Notes (LQFP-128 Pin (14*20mm))

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	0.15	0.002	-	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.2	0.27	0.007	0.009	0.011
D	22.00BSC			0.866BSC		
D_1	20.00BSC			0.787BSC		
D_2/E_2	5.6	-	7.23	0.220	-	0.285
E	16.00BSC			0.630BSC		
E_1	14.00BSC			0.551BSC		
e	0.50BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-26.

13. Ordering Information

Table 34. Ordering Information

Part Number	Package	Status
RTL8376-GR	LQFP 128-Pin E-PAD ‘Green’ Package	

Note: See page 5 for package identification.

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