AQUANTIA®

Product Datasheet
October 2018

AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C
AQrate® Gen 4 Multi-Gigabit Ethernet PHY Transceiver

General Description

The Aquantia® AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C AQrate PHYs are full-reach, low-power, high-performance, multi-gigabit, single-port Gen 4 Ethernet PHY transceivers that are designed with 14nm, multi-gate, FinFET process technology that supports the following network rates: 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX/10BASE-Te.

Aquantia AQrate PHYs are compliant with both the IEEE® 802.3an/bz standard and the NBASE-T™ Alliance PHY Specification to perform all of the physical layer functions required to implement 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX/10BASE-Te transmission over 100+ meters of twisted pair cabling. The AQrate PHY family integrates such key features as Energy Efficient Ethernet (EEE), Precision Time Protocol (PTP)/1588v2, IEEE MAC Security (MACsec), Synchronous Ethernet (Sync-E), support for all PoE standards up to 100W, and support for jumbo packets up to 16KB in all operating modes.

The AQR113-AQR114-AQR115 are pin-compatible, multi-gigabit, single-port PHYs housed in 7 mm x 11 mm, 104-pin, flip-chip BGA (FCBGA) packages, while the AQR113C-AQR114C-AQR115C PHY devices are pin-compatible, multi-gigabit, single-port PHYs housed in compact 7 mm x 7 mm, 64-pin FCBGA packages.

Note: For the remainder of this datasheet, the term *device* or *device family* can be used interchangeably to represent the AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C product line, unless a distinction needs to be made based on the specific package or supported features.

Features	Benefits
• **AQR113/AQR113C**: 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX/10BASE-Te • **AQR114/AQR114C**: 5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX/10BASE-Te • **AQR115/AQR115C**: 2.5GBASE-T/1000BASE-T/100BASE-TX/10BASE-Te	• Pin-compatible low-power, high-performance, multi-gigabit, PHYs enable design flexibility and reuse
• IEEE 802.3an/bz and NBASE-T featuring AQrate technology o 10GBASE-T: 100 meters over Augmented Cat 6 (Cat 6A) and Cat 7, 55 meters over Cat 6, and best effort over Cat 5e o 5GBASE-T, 2.5GBASE-T: over 100 meters of Cat 5e or better cabling	• Ability to support highest data rate possible with a given cable environment while reducing power and latency • 5G and 2.5G operation over legacy infrastructure, while delivering backward compatibility with existing equipment
• Energy-Efficient Ethernet (EEE) • MACsec (IEEE 802.1ae, MAC security standard) o Full support for Advanced Encryption Standard (AES-256) and stand-alone operation • PTP/1588v2 • Synchronous Ethernet (Sync-E), ITU-T standard in cooperation with IEEE	• EEE lowers overall power consumption and lowers equipment operating costs • MACsec provides for secure, encrypted data communications across networks • PTP/1588v2 provides for timing accuracy across the network • Sync-E synchronizes clock signals on the PCB
• Integrated Wake-on-LAN (WoL) Support o Compliant to Microsoft Network Device Class specification • Energy Detect o Places PHY in a low-power state when there is no active link partner	• Integrated packet filtering enables sub-1W support in 100BASE-TX mode • Provides additional power savings when no active link partner is present
• Built-in Thermal Management o On-chip thermal sensor with alarm and warning thresholds	• Enables deployment in thermally constrained environments

Features	Benefits
• 7 mm x 11 mm (AQR113-AQR114-AQR115) o 104-pin FCBGA package o 0.8 mm ball pitch o Low thermal resistance • 7 mm x 7 mm flip-chip (AQR113C-AQR114C-AQR115C) o 64-pin FCBGA package o 0.8 mm ball pitch o Low thermal resistance	• Low cost • Flexible heat-sinking • Compatible with volume PCB manufacturing
• IEEE ® 802.3-2012 compliant auto-negotiation	• Interoperable with existing Ethernet infrastructure
• External SPI FLASH interface with optional FLASH-less operation o At-manufacture FLASH burn capability	• Reduces BOM cost as one or no FLASH devices required • Enables firmware download/upgrade and FLASH image loading during manufacturing
• 50MHz Crystal or LVDS oscillator clock operation o Integrated ultra-low phase noise synthesizer • 50MHz output clock signal • 156.25MHz LVDS oscillator clock operation	• Crystal operation allows for lower BOM cost • Outputs primary and secondary 50MHz and 156.25MHz received reference output for Sync-E
• Advanced Cable Diagnostics o On-chip high-resolution cable analyzer	• Enables the deployment of meaningful cable analysis tools for debugging installation problems
• High-Performance full KR (with autonegotiation)/XFI/USXGMII/5000BASE-R/ 2500BASE-X/SGMII I/F with AC-JTAG/1000BASE-X o Capable of rate adapting all rates into KR/XFI via PAUSE and 100M/1G into 2500BASE-X	• Ensures trouble-free operation over a range of interconnect scenarios (includes parallel detect and downshift capabilities) • Comprehensive interface support o Supports legacy and next generation MACs/switches/processors
• Advance Loopback and Diagnostic Capability o Flexible on-chip BERT o Full 1 second packet counters and CRC-32 checkers	• Enables extensive system test and debug with remote loopback control
• Integrated MDI Filter and Advanced RFI Cancellation o Eliminates external filter components	• Robust Radio Frequency Interference (RFI) performance o Resilient operation when exposed to RFI

Detailed Description

A block diagram of the device family is shown in Figure 1 on page 3. Its port utilizes a common analog front-end for all supported network rates, and a common system interface (configurable as KR or XFI in 10G, 2500BASE-X in 2.5G, and SGMII in 1G or 100M, or all rates via USXGMII/KR). In the transmit direction in 10G, and AQrate modes, data from the system interface is equalized and received. This data is then mapped into a virtual internal XGMII interface where blocks of two XGMII frames (32 bits of data + 4 bits of control) are encoded into a single 65B block, using the 64B/65B encoding scheme specified in Clause 55. In 10G mode, fifty of these 65B blocks are aggregated together, along with a prepended auxiliary bit, and an appended CRC-8 to form the 3259-bit 10GBASE-T transmission frame payload.

This payload is then encoded using a combination of Low-Density Parity-Checking (LDPC) encoding and coset partitioning, with the LDPC encoding adding an additional 325 systematic check bits to produce a 3584-bit 10GBASE-T transmission frame. The coset partitioning effectively divides the frame up into 512 7-bit symbols, where the upper 3 bits are uncoded and describe the coset, while the lower 4 bits are coded and identify an element within the coset. These 8 cosets are then mapped onto a 128-DSQ constellation (a 16 x 16 checkerboard pattern) which is physically encoded as two back-to-back PAM-16 symbols.

These symbols are then coded using the Tomlinson Harashima Precoded (THP) technique, filtered, and sent out over the four twisted pairs in the cable. AQrate 5G transmission is done in a similar fashion, but it uses a fully LDPC encoded 320ns PAM-16 frame containing twenty-five 65B blocks.

The AQrate 2.5G transmission is also similar, but it uses a 640ns frame that contains twenty-five 65B blocks. In the receive direction in 10G, 5G, and 2.5G modes, PAM-16 coded symbols enter the device family from the line interface and pass through the hybrid, which provides transmit/receive isolation. These symbols are then filtered and amplified prior to being sampled by four, high-speed, high-precision Analog-to-Digital (A/D) converters.

The outputs of these A/D converters are then passed through an extensive set of adaptive equalizers which provide both cross-talk and echo cancellation. After timing is recovered, the data from the four channels is aligned and merged together to form the original, but noisy transmission frames.

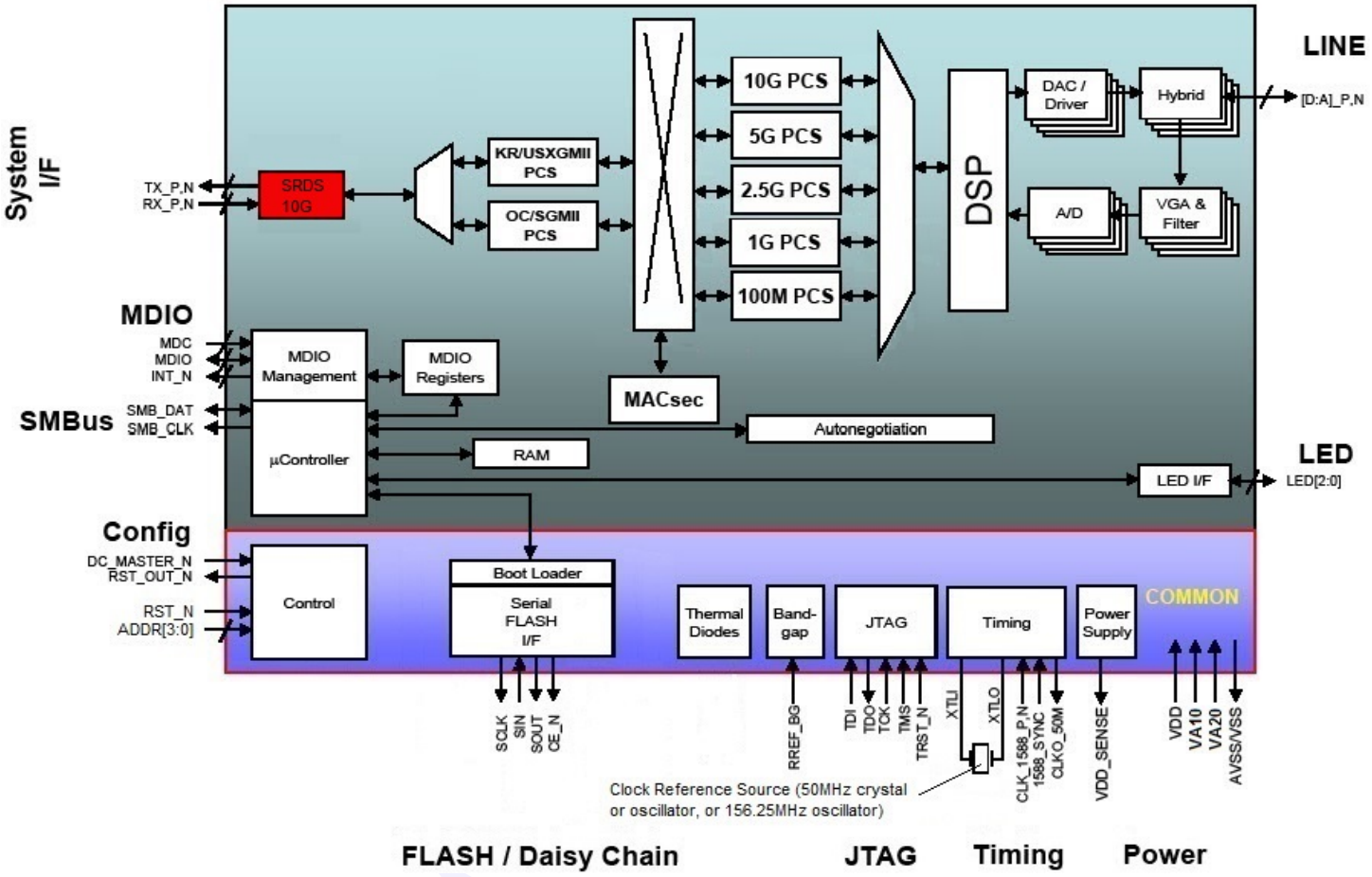

Figure 1 **AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C Block Diagram**

In all three modes, the data is decoded using an LDPC decoder. However, in 10G mode the data is further sliced using knowledge of the coset partitioning and 128-DSQ mapping to produce the original 10GBASE-T transmission frame payload. The CRC-8 over this payload is then checked to ensure integrity of the uncoded bits.

Finally, in all schemes, the auxiliary bit is stripped, 65B blocks remapped into XGMII blocks, and the received Ethernet data transmitted out the MAC interface. When operating in 1G or 100M modes, receive data from the analog front-end is routed to either the 1G or 100M PCS where timing is recovered and equalization performed. In 1G mode, Viterbi decoding is also done.

From here, the data passes across a virtual GMII interface to the system interface which is either SGMII, or USXGMII mode on logical Lane 0. In the transmit direction, if 1G/100M data is received on either the SGMII, or USXGMII interface, it is passed through the 1G or 100M PCS, and is then transmitted by the common analog front-end. Figure 2 shows a typical system-level block diagram of a 10GBASE-T channel built using this device.

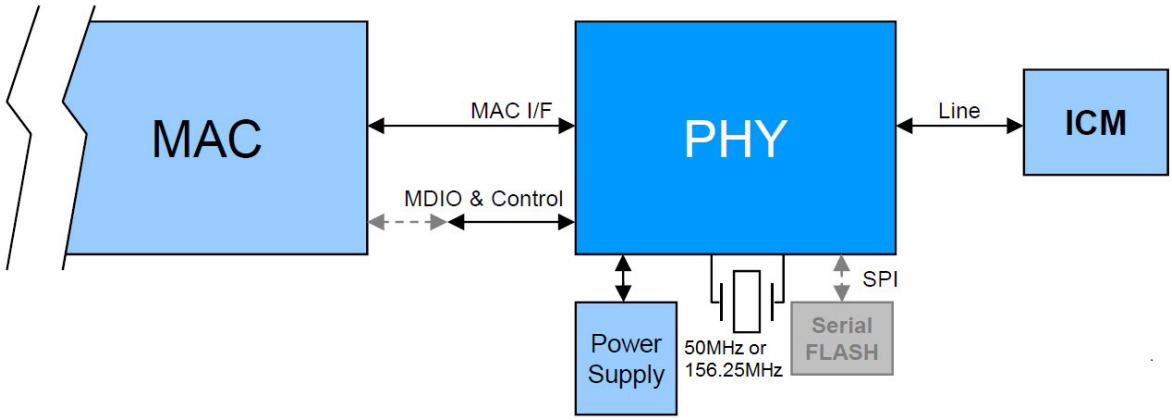

Figure 2 **AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C System Block Interconnect**

On the line side of the device family, a robust interface providing good common-mode rejection and electrical protection against cable discharge is implemented. On the MAC side, the device family provides a robust SerDes interface that supports 10G with configurable pre-emphasis and receive equalization.

For test coverage, this interface also incorporates AC JTAG. Control over the chip is done via an external C-language application program interface (API) that provides an easy-to-use abstraction of the device family, and via an MDIO interface provides the standard Clause 45 register set for control of 10GBASE-T devices.

On-chip, the device family contains a 32-bit microcontroller which manages the state machines and operation of the various elements within the chip. Consequently, there is a great deal of flexibility afforded to the end user because of the presence of this microcontroller, and as such the device family offers a high degree of control and flexibility. The image for the microcontroller is stored either in an optional external SPI FLASH, or loaded at boot time via the MDIO interface (MDIO boot-load).

This interface also provides the user the capability of directly programming the FLASH during manufacturing. In addition to the Ethernet interfaces, the device family provides three 20mA LED outputs for the port that are software configurable to respond to a variety of conditions such as link activity and connection status. Clocking for the device family is provided from a 50MHz external crystal or LVDS differential oscillator or a 156.25MHz LVDS oscillator.

To better assist the system designer in deploying the device family, Aquantia provides a reference design (with part numbers, schematics, and layout) that is optimized for performance, efficiency, and cost. The power for the device family is provided from its analog and digital supply voltages, and it supports an I/O voltage level of either 1.8V or 3.3V.

Package Feature Comparison

This section lists the package feature comparison between the 7 mm x 11mm and the 7 mm x 7 mm packages for the two devices, respectively.

Feature	AQR113-AQR114-AQR115	AQR113C-AQR114C-AQR115C
Device Package Size	7 mm x 11 mm	7 mm x 7 mm
Device Package Type	104-pin FCBGA (8 rows x 13 rows)	64-pin FCBGA (8 rows x 8 rows)
Number of Serial Management Interface Addresses	ADDR[3:0] Up to 16 unique PHY addresses	ADDR[3] Up to 2 unique PHY addresses
PTP/1588v2 Support	Yes	No
Network Rates Supported	• AQR113 (6-speed) • AQR114 (5-speed) • AQR115 (4-speed)	• AQR113C (6-speed) • AQR114C (5-speed) • AQR115C (4-speed)

Table 1: Package Feature Comparison

Package Information

The single-port AQR113-AQR114-AQR115 PHY devices are packaged in a 0.8 mm pitch, 7 mm x 11 mm over-molded, 104-pin FCBGA (8 rows x 13 rows).

The single-port AQR113C-AQR114C-AQR115C PHY devices are packaged in a 0.8 mm pitch, 7 mm x 7 mm over-molded, 64-pin FCBGA (8 rows x 8 rows).

Both the 7 mm x 11 mm and 7 mm x 7 mm packages are marked as shown in Figure 3, and these packages are described in Table on page 6

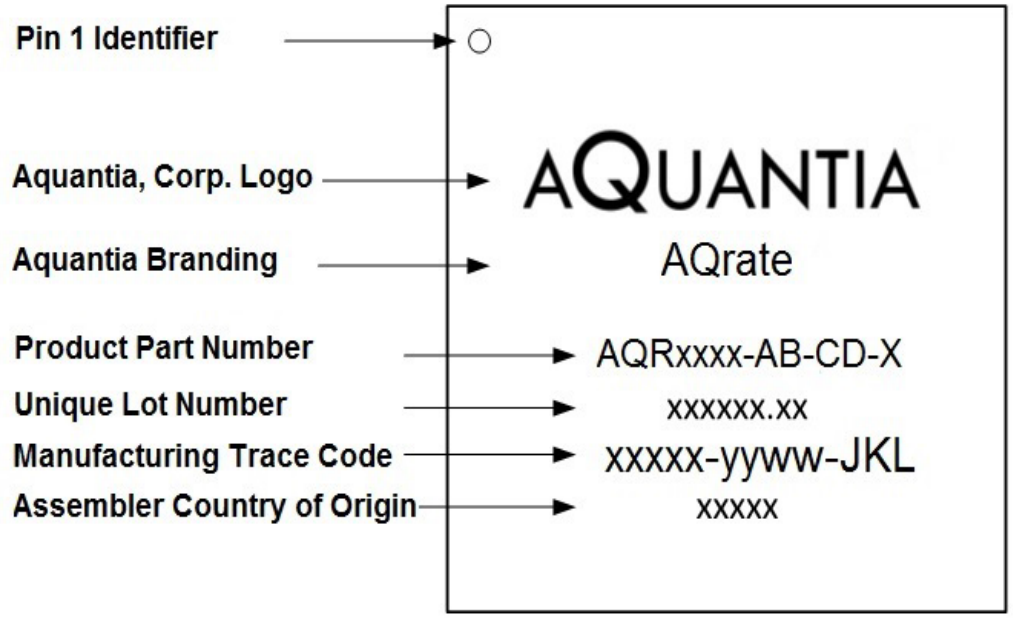

Figure 3 **Part Marking**

Part of Code	Description	Available Options
AQRxxxx	Product Name	Please refer to the master part number specification for specifics
XX	Product Revision Level	Identifies the base and metal layer revision levels
YY	Temperature Grade	C = Commercial
X	Optional Customer-Specific Indicator	Field reserved as an "add mark" field for customer-specific versions of Aquantia products

Table 2: Part Marking Description

Release Notes

Refer to the *Aquantia AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C Release Notes* to determine the latest product revision level device being supported, a full list of known issues, and any errata for both package versions of the AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C family of devices.

Ordering Information

Device	Description	Ordering Part Number
7 mm x 11 mm Package		
AQR113	6-Speed Commercial Temperature Grade, RoHS 6/6	AQR113-XX-C
AQR114	5-Speed Commercial Temperature Grade, RoHS 6/6	AQR114-XX-C
AQR115	4-Speed Commercial Temperature Grade, RoHS 6/6	AQR115-XX-C
7 mm x 7 mm Package		
AQR113C	6-Speed Commercial Temperature Grade, RoHS 6/6	AQR113C-XX-C
AQR114C	5-Speed Commercial Temperature Grade, RoHS 6/6	AQR114C-XX-C
AQR115C	4-Speed Commercial Temperature Grade, RoHS 6/6	AQR115C-XX-C

Note: The "XX" designation in the ordering part number signifies the revision of the device. Please contact your local Aquantia sales representative or FAE for information on the latest device revision.

Contact Information

For more product-related information, use of the following methods to contact your Aquantia Account Manager or Support:

INTERNET: Home: **http://www.aquantia.com**

E-MAIL: **sales@aquantia.com**, **info@aquantia.com**

ADDRESS: Aquantia Corp., 91 East Tasman Drive, Suite 100, San Jose, CA 95134

PHONE/FAX: **408-228-8300**, FAX **408-597-8499**

Revision History

Revision	Date	Chapter/Section	Description
1.0	March 2018	--	Initial release
1.0.1	June 2018	Introduction Chapter 2	Revised company address Revised Table 2.5, Serial FLASH Signals
1.0.2	June 2018	Chapter 2	Revised Table 2.18 and Table 2.19 Revised package drawing for 7 mm x 11 mm device
1.0.3	June 2018	Chapter 2	Revised pin-signal tables
1.0.4	July 2018	Introduction	Revised supported speeds
1.0.5	August 2018	Chapter 5	Revised thermal specifications
1.0.6	September 2018	Chapter 5	Added standard reflow profile for lead-free packages material
1.0.7	October 2018	Introduction	Revised part marking figure per corporate policy to remove trademarks

Trademarks and Copyrights

Strictly Confidential

AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C Revision 1.0.7 - October 2018

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Overview 1

1.1 Introduction

The AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C is a single-port, low-power, high-performance, full-reach, multi-gigabit Gen 4 PHY device family fabricated using 14nm, multi-gate, FinFET process technology. This chapter provides an overview of the device family and its operating modes.

This device family is designed to perform as a cost-competitive, stand-alone, 10G-100Mbps solution for a wide variety of NIC, switch, and LAN-on-Motherboard (LoM) applications that require multi-gigabit capability. The AQR113 and AQR113C devices support the following network rates:

- 10GBASE-T
- 5GBASE-T
- 2.5GBASE-T
- 1000BASE-T
- 100BASE-TX
- 10BASE-Te

The AQR114-AQR114C are 5-speed devices that support 5GBASE-T and all lower listed network rates. The AQR115-AQR115C are 4-speed devices that support 2.5GBASE-T and all lower listed network rates.

Note: For the remainder of this datasheet, the term *device* or *device family* can be used interchangeably to represent the following device family: AQR113, AQR114, AQR115, AQR113C, AQR114C, and AQR115C, unless a distinction needs to be made based on a specific package or supported features.

1.2 General Deployment

This section briefly touches on the hardware implementation. For more detailed hardware design information, please see the *Aquantia Hardware Design Guide* (see “Hardware Design Guide”, Aquantia Corporation" on page 107).

1.2.1 Mechanical

The AQR113-AQR114-AQR115 devices are packaged in a 7 mm x 11 mm, flip-chip 104-pin BGA (8 rows x 13 rows), and the AQR113C-AQR114C-AQR115C devices are packaged in a 7 mm x 7 mm, flip-chip 64-pin BGA (8 rows x 8 rows).

The die is rated to operate up to 108°C junction temperature, so engineering an appropriate thermal solution for the target system is designed so that it is a straight-forward task. For specific thermal values, see Thermal" on page 97.

1.2.2 Power Supplies

The device family utilizes four power supplies:

- A 0.7V digital supply (VDD)
- Two analog supplies: 1.0V and 2.0V (VA10 and VA20, respectively)
- An I/O supply (VDD_IO) with two voltage options (1.8V or 3.3V)

All supplies should come up within 100ms from the first rail rising to the last rail reaching its 70% voltage level. The proper power-up sequence requires the VDD and 1.0V rails reach nominal voltage levels in any order first, followed by the other power rails in any order (this same order *must* be followed for the power-down sequence).

For the I/O supply, the device family offers a configurable VDD_IO that supports either 1.8V or 3.3V, and this will set the logic thresholds for the I/O at 70%/30% of its voltage.

Note: AVSS, VSS, and VSS_SRDS *must* be tied to the same ground plane.

1.2.3 Reset

The device family supports on-chip power-on reset generation, and it is also capable of supplying this reset to the rest of the system via a RST_OUT_N pin.

1.2.4 Clocks

The device family supports using several clocking options: a 50MHz crystal, a 50MHz LVDS oscillator, or a 156.25MHz LVDS oscillator to synthesize all of the required clocks. Supported clocking includes:

- PHY can perform operations using a single, 50MHz external crystal with an absolute accuracy of ±50pmm; only one crystal clock is required per common block.
- PHY can perform differential operations using a single, 50MHz LVDS oscillator with an absolute accuracy of ±50pmm, and the PHY provides 100Ω internal termination for this clock input (only one 50MHz LVDS oscillator is needed for the single version of the PHY).

- PHY can perform differential operations using a single, 156MHz LVDS oscillator with an absolute accuracy of ±50pmm, and the PHY provides 100Ω internal termination for this clock input (only one oscillator is needed for the single-port version of the PHY).

Note: The supported output for synchronous Ethernet (Sync-E) operations in the device family is either 156.25MHz or 50MHz depending on the input clock source.

1.2.5 FLASH

The device family is capable of operating with a 512KByte (4Mbit) or larger SPI serial FLASH for autonomous operation, or of being boot-loaded via the MDIO interface. In both cases, the image stored in FLASH and the MDIO boot-load image are identical. If autonomous operation is not a requirement, and the target system is capable of providing the boot-load image, the FLASH can be eliminated.

The FLASH I/O operating voltage level *must* be the same as the PHY's VDD_IO voltage level. If boot-loading is desired, it is possible to gang-load multiple parts via a broadcast MDIO address in the device family.

1.2.6 Power-On Default Values

The device family supports 10GBASE-T mode and other modes covered by IEEE 802.3an/bz, and includes a fixed set of hardware default values that exist in the chip for all its configurable registers. In addition, its firmware is capable of storing in its boot image (or in a separate image to keep the base firmware constant across multiple platforms) any change to these defaults effectively allows the user to configure the chip to come out of reset in the desired operating state.

1.2.7 SerDes and MDI Configuration

To offer routing flexibility on the SerDes interface, the device family is capable of performing polarity inversions[†]. On the line side, in addition to fully supporting MDI/MDI-X and automatic polarity correction, this device family also supports lane swapping of the ABCD pairs that enables easy board routing with different magnetics pin-outs.

1.3 SerDes

The device family is designed for use in conjunction with a multi-speed MAC chip. Table 1.1, details the supported system interface (I/F) idle options, and Table 1.2 on page 20, lists the SerDes operating modes supported by the device family's system interface (I/F).

[†] Note that polarity inversion is also referred to as "Lane Invert" in the register map.

System I/F Idle Mode	Notes
Off	SerDes turns on at selected operating mode for rate
XFI + USXGMII	
KR + USXGMII	

Table 1.1 **System I/F Idle Options**

This PHY device family includes a single SerDes lane per port that supports 10G, and it supports the following SerDes modes listed in Table 1.2.

System Interface SerDes Operating Modes						
Rates	**USXGMII**	**XFI**	**5000BASE-R**	**2500BASE-X**	**SGMII**	**1000BASE-X**
10G	✓	✓				
5G	✓	✓	✓			
2.5G	✓	✓	✓	✓		
1G	✓	✓	✓	✓	✓	✓
100Mbps	✓	✓	✓	✓	✓	

Table 1.2 **System Interface SerDes Operating Modes**

Note: In Table 1.2, the green check marks indicate native rate support and the orange check marks indicate port-based frame rate-adaptation via one of the native SerDes modes.

1.4 Power-On

The device family is designed to perform the following operations at boot:

- Power-up calibration of internal VCOs and variable power supplies (if variable supply operation is enabled)
- Provision stored default values†
- Calibration of the analog front-end

† AQR113-AQR114-AQR115/AQR113C-AQR114C-AQR115C can store in its firmware image a list of registers with default values that can be overwritten with user-specified values on power-up. To perform this, use the web-based Aquantia Firmware Provisioning Tool, which allows the PHY to be personalized for certain modes of operation.

- Autonegotiation†
- Perform training (as required)
- Verify error-free operation
- Enter steady state

1.5 Cable and Board Diagnostics

The device family implements a powerful cable diagnostic algorithm that accurately measures all of the TDR and TDT‡ sequences within the group of four channels. This algorithm transmits a pseudo-noise sequence with an amplitude of less than 300mV for a brief period of time, and from this, it converges the 10GBASE-T equalizers on all of the other channels. From the results of this measurement, the length of each pair, the top impairment along the pair, and the impedance of the cable are flagged.

These measurements are reported using cable propagation characteristics of 4.83ns/m and these are presented in the Global MMD register map (for details, see “References” on page 107). For board diagnostics, the device family detects opens and shorts on MDI pins or faulty transformers, and these results are stored in the MDIO register.

Note: The device family is an AQrate PHY and compliant with both the IEEE 802.3an/bz standard and the NBASE-T Alliance PHY specifications. In addition, this device family also supports cable diagnostics that meet the latest set of industry-standard switch and port specifications.

1.6 Debug and Diagnostics Tools

The device family supports a full suite of network and system loopbacks at all supported rates, and these loopbacks are shown in Figure 1.1 on page 22.

In addition to the loopbacks, the device family supports CRC-32 packet checking on both the receive and transmit traffic at all supported rates, and it also maintains 1-second interval packet counters for both errored and good packets.

Finally, the device family is able to generate all of the IEEE test mode patterns, as well as CRPAT generation, and checking in both the line and system directions. It also supports (via the API) the ability to generate an eye diagram for each of the receive lanes.

† AQrate supports an automatic downshift capability (as specified in Table 6.9.62 on page 409) for configuring autonegotiation settings.

‡ The cross-channel impulse responses.

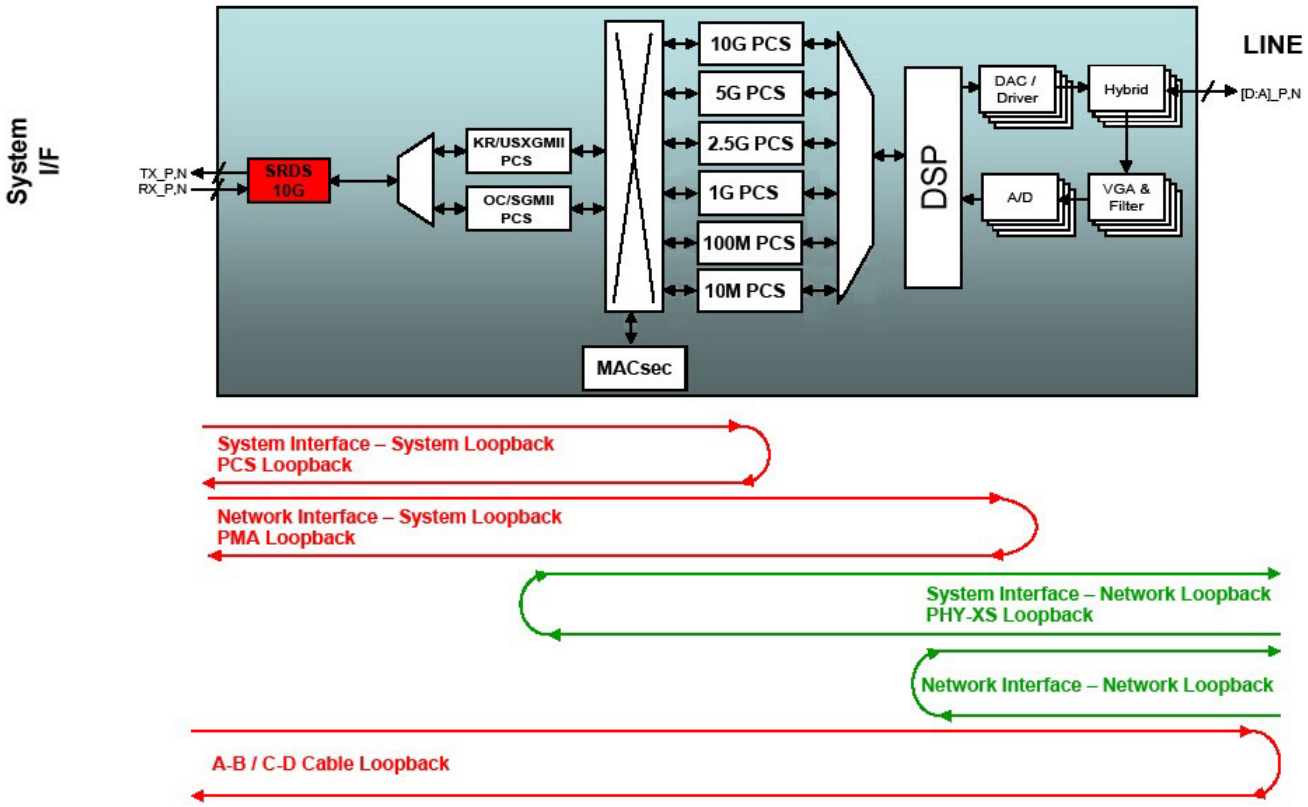


Figure 1.1 **Loopbacks**

On the KR interface, the device family supports x^9, x^{31}, square wave, pseudo-noise generation and checking, as well as CRPAT generation and checking. Figure 1.1 illustrates the supported loopbacks in the device family:

- System interface/system loopback PCS loopback
- Network interface/system loopback PMA loopback
- System interface/network loopback PHY-XS loopback
- Network interface/network loopback
- A-B/C-D cable loopback

1.7 API and Programming Tools

Associated with the device family are the following software tools:

- A set of ANSI C register structures for each MMD that provide bit level and word level access to all of the device family registers.
  For documentation about these structures, refer to the API document (“API”, Aquantia Corporation" on page 107).
- An ANSI C API that provides a set of structures and associated Set/Get functions to implement all normal PHY operations. This API is written with register name abstraction so that the registers are visible, and it is documented using Doxygen, which allows users to view the code and click on a variable to get the datasheet definition.

  This API also contains functions on how to burn new FLASH images, as well as perform other MDIO boot-load operations. For documentation about these and other operations, refer to the API document (“API”, Aquantia Corporation" on page 107).

1.8 MACsec

The device family supports integrated MACsec at all network rates, and it also supports the following modes of operation:

- **Autonomous Operation**: In this mode, the device family does all of the gap insertion and other tasks required to add the MACsec headers and integrity check values (ICVs). This is done via two integrated MACs and 64KB of buffering in each direction. These MACs monitor the buffer fill-depths, and also generate port-based PAUSE frames in either direction, as required. In addition, it responds to port-based PAUSE frames (802.1Qbb class-based PAUSE frames) that are passed through.
- **Cut-through Operation**: In this mode, the device family expects to receive packets from the system pre-gapped, and all the device family does is insert the MACsec headers and ICVs.
- **Bypass Operation**: In this mode, the MACsec block is completely bypassed, in scenarios where MACsec in the PHY is not necessary.

1.8.1 General Features

The MACsec supports the following general features:

1) AES-256, AES-128, and clear operation with simultaneous mixed usage, where the encryption and decryption are decided on a per-packet basis based on an access control list (ACL) that looks either at the MACsec header or fields in the packet header (explicit or implicit secure channel identification).

2) 16 secure channels (SCs), with two security associations (SAs) per SC with automatic roll-over between SAs on a programmable packet number (PN) value.

3) Full support of the 802.1AE MIB (for details, see “Media Access Control (MAC) Security”, IEEE STD-802.AE-2006, IEEE Standards Office, The Institute of Electrical and Electronics Engineers, Inc., 3 Park Avenue, New York, NY 10016-5997, USA, April 17, 2003).

4) Per packet Galois counter mode (GCM) authentication on the ICV (16 or 32 byte).

5) Strict and out-of-order replay checking with a per SC programmable 32-bit (for example, from 0 to 2^{31}-1 packets) replay window for the out-of-order mode.

6) A programmable confidentiality offset per SA of between 0 and 127 bytes offset.

7) A MIB containing the following additional statistics counters:

Per SA	Name	Description
	Ingress Control Packets	The number of ingress control packets received
X	Ingress Untagged Hit Packets	The number of ingress untagged packets received that passed the implicit SCI lookup
	Ingress Untagged Miss Packets	The number of ingress untagged packets received that had no implicit SCI lookup
X	Ingress Hit Packets Dropped	The number of ingress packets that passed the SCI lookup, but were tagged for Drop
	Ingress Tagged Packets	The number of ingress packets with a MACsec header
	Ingress Tagged Packets Bad Tag	The number of ingress packets with an invalid SecTag or packet number (PN).
	Ingress Tagged Packets SCI Miss	The number of ingress tagged packets with a missing SCI or an SCI that was not in the table.
X	Ingress Tagged Packets Non-Operational SA	The number of ingress packets with an identified, but non-operational SA.
X	Ingress Packets Authentication Fail	The number of ingress packets that fail authentication

Table 1.3 **Additional Ingress MACsec Statistics**

Per SA	Name	Description
X	Ingress Packets Replay Fail	The number of ingress packets that fail the replay check
X	Ingress Packets Late	The number of ingress packets that fail the replay check because they are late
X	Ingress Packets OK	The number of ingress packets that pass all checks
	Ingress Reserved Counter 0	
	Ingress Reserved Counter 1	
	Ingress Reserved Counter 2	
	Ingress Reserved Counter 3	

Table 1.3 **Additional Ingress MACsec Statistics** (continued)

Per SA	Name	Description
	Egress Control Packets	The number of egress control packets transmitted
	Egress Packets Unknown SA	The number of egress packets transmitted with an unknown SA (Table Miss and Untagged)
	Egress Untagged Packets	The number of egress packets transmitted without a MACsec header
X	Egress Protected Packets	The number of egress packets transmitted with a valid ICV (authenticated + encrypted)

Table 1.4 **Additional Egress MACsec Statistics**

1.8.2 Ingress Lookup

On ingress, the MACsec block can perform the following tasks:

1) Remove the MACsec header.

2) Strip zero-padded bytes for runt packets.

3) Corrupt the FCS for any failed packets.

4) Run a consistency check against another ACL.

5) Count control packets.

6) Enforce maximum MTU sizes via either truncation or FCS corruption.

7) Generate an interrupt on security failure.

8) Look up the implicit SCI based on the following fields:

   a) MAC DA - 48 bits

   b) MAC SA - 48 bits

   c) Payload Ether-Type - 16 bits

   d) QTAG_VLD and STAG_VLD (Ingress Consistency Check only)

   e) TCI/AN - 8 bits (Note that TCI needs preprocessing as per Clause 9.1.2)

   f) SCI - 64 bits

   g) VLAN - 12 bits (Ingress Consistency Check only)

   h) Any four programmable bytes within the first 64 bytes of the packet

   i) Origin (loopback versus front panel) - ingress table only

   j) Valid bit

9) Lookup the implicit SCI based on the following fields:

   a) The MACsec block for the device family supports the ability to calculate the following categories: EtherType, VLAN, and the User-Priority of a packet by using a 32-bit mapping table provided with each entry in the SCI lookup. There is one mapping table per port and the mapping table contains the following fields:

Bit	Name	Function
31	PARSE_QTAG	Enables parsing 802.1Q VLAN tags
30	PARSE_STAG	Enables parsing 802.1Q MST tags
29	PARSE_QINQ	Enables Q-in-Q parsing
28	QTAG_UP_EN	Enables the use of the 802.1Q priority

Table 1.5 **"Per SCI" 32-Bit Mapping**

Bit	Name	Function
27	STAG_UP_EN	Enables the use of the 802.1S priority
26:24	DEF_UP	Represents default user-priority
23:0	MAP_TBL	Represents priority mapping for 802.1Q priority tags

Table 1.5 **"Per SCI" 32-Bit Mapping** (continued)

Note: The EtherType, VLAN, and User-Priority packet categories are determined using the mapping table fields (listed in Table 1.5):

b) EtherType and VLAN resolution is determined, as shown in Figure 1.3 on page 28.

Note: 802.1S and 802.1Q EtherTypes are provisionable per port.

c) User priority is resolved, as shown in Figure 1.2.

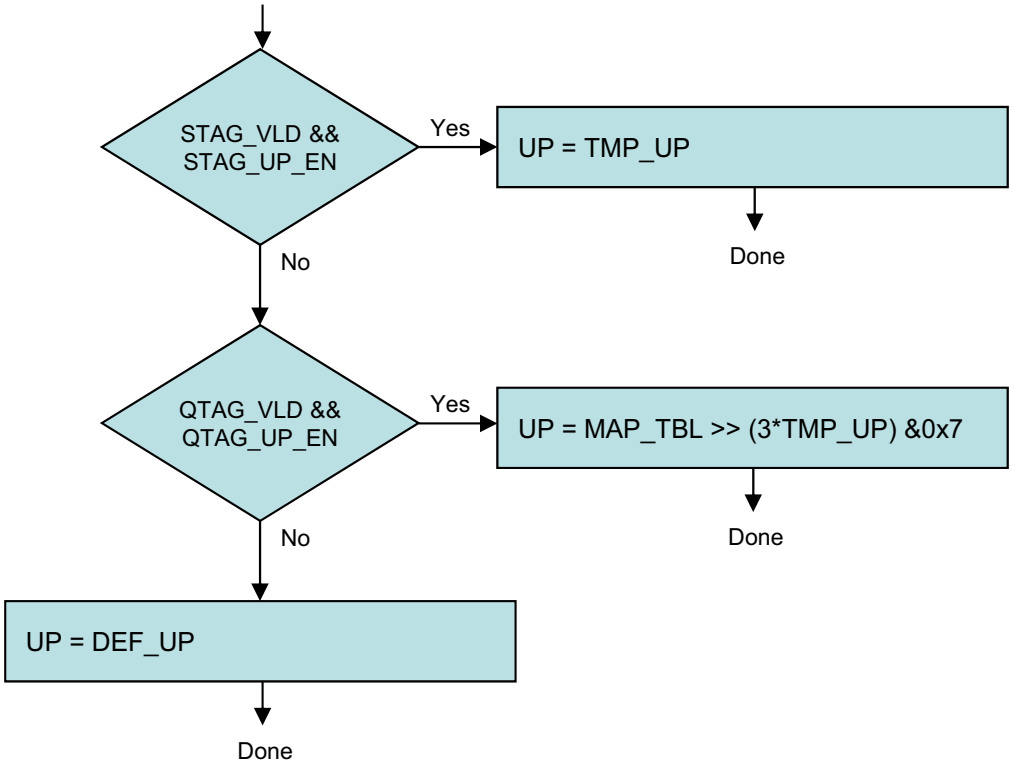


Figure 1.2 **User Priority Resolution**

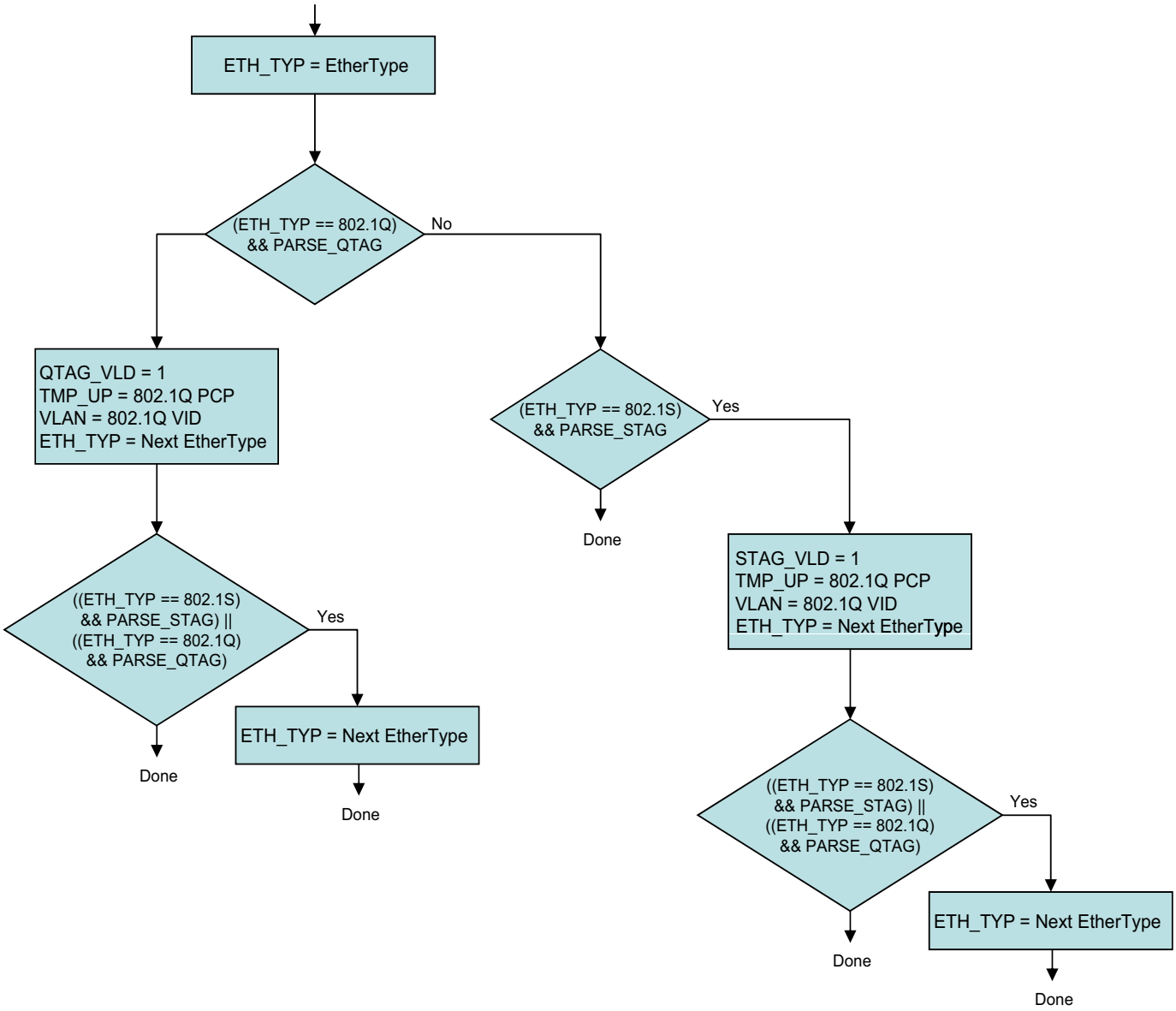


Figure 1.3 **EtherType and VLAN Parsing Algorithm**

*10)*Support a provisioned definition of the 802.1Q and 802.1S EtherType tags.

11) Support the following actions from the SCI lookup:

a) Decrypt/Authenticate (provisioned per SA)

b) Drop

c) Bypass

d) Re-direct (capture to debug)

12) Support globally changing the action for the lookup on a table basis (for allowing rapid debug).

1.8.3 MACsec Ingress Post-Processing

After decryption and during post-processing, the MACsec block can perform the following tasks:

1) Remove or leave the MACsec header.

2) Over-write the PN field of the MACsec header with provisionable data when operating in MACsec header non-removal mode.

3) Strip zero-padding bytes from the packet according to the MACsec header short-length (SL) field.

4) Grow short packets that are not SL stripped back to 64-bytes (for example, the MACsec packet is ≥ 64 bytes, but after removal of the MACsec, the packet is sub-64 bytes).

5) Support the corruption of the FCS on packets which fail any enabled security check in both the ingress and egress directions.

6) Support a 32-entry per-port consistency check after decryption based on:

a) SAI_HIT

b) SAI[3:0]

c) VLAN[11:0]

d) VLAN_VLD

e) ETYPE_VLD (EtherType > Programmable maximum length)

f) Payload EtherType[15:0]

g) Each of these fields shall be maskable and have a single action bit indicating whether to drop the packet or not.

h) The port shall also support a 33rd entry that indicates what to do with a miss.

7) Generate an interrupt on security failure.

1.8.4 Egress Processing

On egress, the MACsec block can perform the following tasks:

1) Support the same lookup and mapping mechanism as is used in the ingress direction.

2) Support the ability to perform lookup with and without the presence of a MACsec header.

3) Zero pad short packets and mark the SL field in the MACsec header accordingly.

4) Fill in the remainder of the MACsec header, given provided TCI and SL fields. This means that the MACsec EtherType (88_E5), AN, PN, and optional SCI are filled in by the PHY.

5) Support the following actions from the SCI lookup:

a) Encrypt/Authenticate (provisioned per SA)

b) Drop

c) Bypass

d) Re-direct (loopback or capture to debug)

6) Count control packets.

7) Enforce maximum MTU sizes via either truncation or FCS corruption.

8) Support globally changing the action for the lookup on a table basis (for allowing rapid debug).

9) Generate an interrupt on security failure.

1.8.5 MACs

The MACs in the MACsec block can perform the following tasks:

1) Support ingress and egress MIBs with per-EtherType 40-bit counters and RMONs (packet drop and packet pass-through).

2) Support an in store-and-forward mode that is a port-based PAUSE flow-control in both directions, with programmable thresholds and hysteresis.

3) Ignore 802.1Qbb class-based PAUSE frames and pass them through the PHY.

4) Support programmable ingress and egress inter-packet gap (IPG) of between 4 and 63 bytes†.

5) Support processor access to the MAC buffers for debug.

6) Support the ability to recognize control packets via the following criteria:

   a) MAC_DA[47:4] = 01_80_C2_00_00_0

   b) MAC_DA[47:4] = 01_00_0C_CC_CC_CC

   c) 8 per port programmable MAC_DA addresses

   d) 8 per port programmable EtherType matches

   e) 1 per port programmable MAC_DA with Do Not Care mask

   f) 2 sets of per port programmable MAC_DA and EtherType combinations

   Note: These are provisionable on a port-by-port basis.

7) Support sending and receiving up to 512 byte packets in both the ingress and egress directions.

   Both the ingress and egress ports shall each support a programmable MAC address, and the ability to disable operation of these ports.

† With each packet having a fixed 7-byte preamble and 1-byte start-of frame delimiter (SFD).

8) Support a non-destructive L2 system loopback, with a programmable MAC address and an enable. This loopback FIFO *must* be 512 bytes in size and support head and tail drop (provisionable). This FIFO *must* be capable of being stopped at any time (on a packet-by-packet granularity) and the packet(s) within read out.

   The depth of this FIFO needs to be programmable. Packets larger than the programmable size can be dropped or truncated (programmable). Packets that are dropped due to overflow *must* be counted on a per SA basis using an 8-bit counter (as saturating, and clear-on-read).

   These looped-back packets *must* be accounted for in a similar set of counters to the ingress MAC, as they are not accounted for there (for example, the loopback after ingress MAC).

9) Enforcing a per priority, programmable maximum MTU size with an option for either truncation or FCS corruption.

10) Support the following statistics on ingress and egress (as shown in Table 1.6):

Egress	Ingress	Per Priority	Name	Description
X	**X**		Total Packets	The total number of packets (good + bad)
X	**X**	**X**	Total Packets (per priority)	The total number of packets (good + bad) (per priority)
X	**X**		Dropped Packets	Packets dropped for any reason
X	**X**	**X**	Dropped Packets (per priority)	Packets dropped for any reason (per priority)
X	**X**		Bytes	Total frame octets
X	**X**	**X**	Bytes (per priority)	Total frame octets (per priority)
X	**X**		Broadcast Packets	Total broadcast packets with a good FCS
X	**X**		Multicast Packets	Total multicast packets with a good FCS
X	**X**		Fragments	Frames < 64 bytes with a bad FCS
X	**X**		Jabbers	Frames > MTU_{MAX} with a bad FCS

Table 1.6 **MAC Statistics**

Egress	Ingress	Per Priority	Name	Description
	X		CRC Align Errors	Frames with a bad FCS that are neither fragments nor jabbers in-the-clear
X			Bad Packets	Frames with a bad FCS
X			Good Packets	Frames with a good FCS
	X		Undersize Packets	Frames with a good FCS less than 64 bytes
X	X		64 Byte Packets	The total number of packets (good + bad) of 64 byte length
X	X		65 To 127 Byte Packets	The total number of packets (good + bad) between 65 and 127 byte length
X	X		128 To 255 Byte Packets	The total number of packets (good + bad) between 128 and 255 byte length
X	X		256 To 511 Byte Packets	The total number of packets (good + bad) between 256 and 511 byte length
X	X		512 To 1023 Byte Packets	The total number of packets (good + bad) between 512 and 1023 byte length
X	X		1024 To 1518 Byte Packets	The total number of packets (good + bad) between 1024 and 1518 byte length
X	X		1519 To 1522 Byte Packets	The total number of packets (good + bad) between 1519 and 1522 byte length
X	X		1523 To 1548 Byte Packets	The total number of packets (good + bad) between 1523 and 1548 byte length
X	X		1549 To 2000 Byte Packets	The total number of packets (good + bad) between 1549 and 2000 byte length
X	X		2001 To 2500 Byte Packets	The total number of packets (good + bad) between 2001 and 2500 byte length

Table 1.6 **MAC Statistics** (continued)

Egress	Ingress	Per Priority	Name	Description
X	X		2501 To MTU Byte Packets	The total number of packets (good + bad) between 2501 and MTU byte length in-the-clear
X	X		1549 To MTU Byte Packets	The total number of packets (good + bad) between 1549 and MTU byte length in-the-clear
X	X	X	Oversize Packets (per priority)	The total number of packets of length greater than MTU bytes and a good FCS in-the-clear
X	X		MAC Control Packets	MAC Control Frames with EtherType 88_08 in-the-clear or secured (option for both)
	X		Errored Packets	Packets with Code or Symbol Errors

Table 1.6 **MAC Statistics** (continued)

*11)*Count MAC control packets that are either secured, unsecured, or both.

1.9 Energy Efficient Ethernet

The device family provides support for EEE on both the system interfaces and line interfaces:

- Supported system interfaces include SGMII and XFI/KR/USX.
- Supported on the line side: 10GBASE-T, 5GBASE-T, 2.5GBASE-T, and 1000BASE-T.

Note: It is also capable of running in both a normal operating mode, where the system controls entering and exiting from the EEE state, and also in autonomous operations on the line, where the PHY controls the entering and exiting EEE operation via a provisionable “no-traffic” timer.

If no traffic is seen within a certain period of time, the line side of the PHY goes into Low Power Idle (LPI) a *sleep* mode if it is connected to any of the supported rates. This operating mode requires that the MACsec buffers and MACs be in operation.

MACsec buffers are required in internal mode to buffer the packet while the line is being restored to operational mode. The system side operates in normal non-EEE mode while the line side operates in EEE mode.

1.10 Precision Time Protocol (PTP)

The device family provides support for PTP and related protocols. Specifically, it supports the following protocols (running both over MACsec or in the clear):

- 1588 Version 1 (1-step and 2-step)
- 1588 Version 2 (1-step and 2-step)
- NTP Version 3
- NTP Version 4
- SNTP Version 4

To support these protocols, the device family provides the following counters:

- A 48-bit seconds counter.
- A 32-bit nanoseconds counter. Note that since 10^9 = 0x3B9ACA00, only 30 bits of this counter actually count.
- A 32-bit fractional nanoseconds counter (LSbit = 2^{-32}ns).

A programmable increment that is sufficient for adding the correct amount of nanoseconds and fractional nanoseconds to the counter for each reference clock cycle.

For example, if you are running on a 200MHz clock, then the increment should nominally be 5ns per cycle; hence, only 3 nanosecond bits and 32 fractional nanosecond bits are required.

Note: All of the PTP counters can be adjusted on-the-fly (setting, adding, and subtracting).

For the ingress, timestamping accuracy in the device family is rounded to 16 fractional nanosecond bits (48 + 32 + 16 = 96 bits). This timestamp is appended to the packet (or placed in the packet preamble when operating in USXGMII mode) and the packet's header and FCS are altered accordingly.

The packet can then be passed to the system interface, or placed in a 512-byte FIFO that can be accessed from the MDIO registers space. A similar FIFO in the egress direction supports the ability to send sync packets into the data stream. Note that the MACsec buffers and associated MACS *must* be operating for this to work.

To support asymmetry between the TX and RX paths, the device family supports a correction register to offset the timestamps by the required amount. The device family also supports the following PTP features:

- Running the PTP clocks from the received line clock.
- Running the PTP clocks from an external (up to) 100MHz LVDS clock input.
- Transparent clock mode.

Hardware Interfaces† 2

2.1 Package Pin-Signal Differences

This section lists key pin-signal functional differences between the 7 mm x 11 mm and the 7 mm x 7 mm packages as shown in Table 2.1.

7 mm x 7 mm Package	7 mm x 11 mm Package	Description
MDIO Address Pin-Signals		
Note: The 7 mm x 7 mm package supports *only* one external MDIO address pin (ADDR3).	ADDR0	Only the 7 mm x 11 mm package supports ADDR0-ADDR3 (the 7 mm x 7 mm package only supports one address pin). See Table 2.2 on page 38, for details.
	ADDR1	
	ADDR2	
	ADDR3	
External PTP Reference Clock Pin-Signals		
Note: This package does not support an external PTP reference clock.	CLK_1588_N	Only the 7 mm x 11 mm package supports an external PTP reference clock. See Table 2.13 on page 61, for details.
	CLK_1588_P	
Clock Frequency Select Pin-Signal		
Note: This package does not support a clock frequency select pin.	CLK50M_SELECT_N	Only the 7 mm x 11 mm package supports a clock frequency select input used for selecting either 50MHz or 156.25MHz. See Table 2.13 on page 61, for details.
Daisy-Chain Pin-Signals		
Note: This package does not support a daisy-chain configuration.	DC_MASTER_N	Only the 7 mm x 11 mm package supports a daisy-chain configuration. See Table 2.6 on page 50, for details.
	RX_DC_RST_N	
	TX_DC_CLK	
	TX_DC_DATA	
	TX_DC_SOF	

Table 2.1 **Key Pin-Signal Package Differences**

† Table Conventions: any signal name that ends with "*" or pin name that ends with "_N" are active low.

2.2 Management Interface

Table 2.2 on page 38 shows the management interface signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Interrupt*	INT_N	L8	G2	OD	Open-drain interrupt signal of the device family. On reset, this is set high. There should be external pull-up resistor to this signal, and the pull-up voltage cannot exceed the VDD_IO voltage.
MDIO Address	ADDR0, ADDR1, ADDR2 ADDR3	F8 M7 K8 M5	-- -- -- H5	I	Logic inputs for setting the MDIO PHY address of the device family. **Note:** The 7 mm x 7 mm package supports *only* one external MDIO address pin.
MDIO Clock	MDC	J8	E1	I	MDIO clock input for PHY 0 of the device family. This input has a digital edge lock-out to prevent clock glitches due to reflections.
MDIO Data	MDIO	H8	D2	I/O	MDIO data line for the device family with Schmitt-triggered logic levels. On reset, it is set to high-impedance. There should be an external pull-up resistor on the PCB.
Reset Out*	RST_OUT_N	K3	H7	OD	Open-drain reset output from the device family. This may be used to drive the power-up reset signal for a board, as it outputs the on-chip power-up reset signal from the device family. There should be external pull-up resistor to this signal, and the pull-up voltage cannot exceed the VDD_IO voltage.

Table 2.2 **Management Interface Signals**

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Reset*	RST_N	F3	H2	I	Hard reset input for the device family with Schmitt-triggered logic levels.
VDD IO Select	VDD_IO_1P8_ SELECT_N	H3	F1	I	When pulled low, this signal enables the I/O to operate from a VDD_IO at 1.8V. When pulled high, the I/O are set to operate at 3.3V.

Table 2.2 **Management Interface Signals** (continued)

Management interface on the device family is done via a two-wire interface with a unidirectional MDC clock and a bidirectional MDIO data. The MDIO interface on the device family is a robust implementation of this standard.

It is designed to operate up to 10.5MHz† and is capable of withstanding voltages up to double the operating voltage (being the theoretical worst-case maximum reflection on an unterminated bus). It utilizes a Schmitt-trigger in conjunction with a debounce state machine to debounce the signals, and is capable of hot-insertion.

The data line is capable of pulling low a 280Ω load tied to 1.8V, and it may be configured to support either open-drain, or push-pull operation in "Global General Provisioning 2: Address 1E.C441" (push-pull is the default operating mode).To provide flexibility to the implementation, the device family uses a programmable I/O voltage.

Note: The logic thresholds for the I/O are set at 70% and 30% of VDD_IO for V_{IH}/V_{OH} and V_{IL}/V_{OL} respectively.

The VDD_IO voltage level affects MDC, MDIO, INT_N, and RST_N. When the VDD_IO is set for 1.8V operation, the pin MDIO_1P8_SELECT_N has to be pulled to ground, and when set for operation at 3.3V the pin MDIO_1P8_SELECT_N has to be pulled to VDD_IO. The management interface allows for communication between the Station Management (STA) and a physical layer device (PHY).

The STA is the external host controller that is the master of the management interface bus. Consequently, it always sources the MDC clock. When the MDIO is sourced by the STA, the PHY samples the MDIO at the rising edge of MDC.

† This is a function of whether the output is set to push-pull or open-drain mode, and on the capacitance of the bus.

When the MDIO is sourced by the PHY during read operations, the STA samples the MDIO at the rising edge. Table 2.3 shows the management interface frame format (802.3-2005 45.3), and the fields are described as follows:

Frame	PRE	ST	OP	PHYAD	MMDAD	TA	Data	IDLE
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read increment address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

Table 2.3 **MDIO Frame Format**

2.2.1 IDLE (Idle Condition)

The idle condition on the management interface is a high-impedance state. All tri-state drivers are disabled and the pull-up resistor(s) on the MDIO bus will pull the MDIO line to a one (1).

2.2.2 PRE (Preamble)

2.2.2.1 Normal Operation

At the start of each transaction, the station management entity sends a sequence of 32 contiguous ones (1s) on the MDIO data line, along with the 32 corresponding cycles on the MDC. This provides the MMD with a pattern it can use to establish synchronization. Each MMD observes a sequence of 32 contiguous “1” bits on MDIO with 32 corresponding cycles on the MDC before responding to any transaction.

2.2.2.2 Preamble Suppression

Optionally, the MDIO interface can disable preamble detection by setting the "MDIO Preamble Detection Disable" bit. This bit is in "Global General Provisioning 2: Address 1E.C441". In this mode of operation, one or more of the preamble bits are required, which are then followed by the 0x0 start of the frame ST bits.

2.2.3 ST (Start Of Frame)

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 are ignored by the MMDs within the device family.

2.2.4 OP (Operation Code)

The operation code field indicates the type of transaction that is being performed by the frame:

a) A <00> pattern indicates that the frame payload contains the address of the register to access.

b) A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame.

c) A <11> pattern indicates that the frame is read operation.

d) A <10> pattern indicates that the frame is a post-read increment address operation.

2.2.5 PHYAD (PHY Address)

The PHY address is four bits, which allows for up to 16 unique PHY addresses, and up to 16 PHYs on an MDIO bus. Note that the address of the PHY is determined from the four bits that comprise the ADDR[3:0] pins (ADDR0, ADDR1, ADDR2, and ADDR3).

The first PHY address bit to be transmitted and received is the Most Significant Bit (MSB) of the address. The station management entity *must* have apriori knowledge of the appropriate PHY address for each PHY to which it is attached, regardless if it is connected to a single PHY or to multiple PHYs.

Note: The AQR113-AQR114-AQR115 device can support up to 16 unique PHY addresses, while the AQR113C-AQR114C-AQR115C device can only support two unique PHY addresses.

2.2.6 MMDAD (MMD Address)

The MMD address is four bits, which allows for up to 16 unique MMDs per PHY. The first MMD address bit transmitted and received is the MSB of the address. In addition, the device family supports a broadcast mode when the PHYAD is 0x00.

Note: Only the write and load address opcodes are supported in broadcast mode. Read and post-read increment opcodes are ignored in broadcast mode.

This mode of operation can be enabled via the "MDIO Broadcast Mode Enable"bits ("Global General Provisioning 2: Address 1E.C441").

2.2.7 TA (Turnaround)

The turnaround time is a 2-bit time spacing between the MMD address field and the data field of a management frame to avoid contention during a read transaction.

For a read or post-read increment address transaction, both STA and the MMD remain in a high-impedance state for the first bit time of the turnaround. MMD then drives a zero bit during the second bit time of the turnaround of a read or post-read increment address transaction.

During a write or address transaction, the STA transmits a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround, and this behavior is shown in Figure 2.1 on page 42.

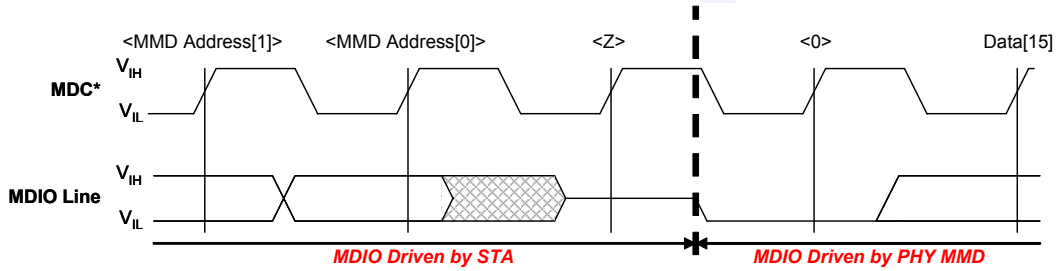


Figure 2.1 **MDIO Bus Turn-Around During Read Operations**

2.2.8 ADDRESS/DATA

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register.

For a read or post-read increment address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

For counters that are greater than 16-bits, the Least Significant Word (LSW) *must* be read first, then the MSW *must* be read immediately afterwards. When the LSW is read, the counter is cleared and the MSW is stored in a shadow register. Reading the MSW actually reads the shadow register.

Optionally the host may read the MSW first, then the LSW immediately afterwards by setting the "MDIO Read MSW First Enable" bit in "Global General Provisioning 2: Address 1E.C441".

2.2.9 Interrupt

The device family supports an open-drain interrupt pin per PHY.

2.2.10 Reset

The device family supports an active-low reset input. In addition to this, the device family is capable of generating a RST_OUT_N signal from its internal power-on reset generation circuitry that can be used by the external board circuitry. The operation of the reset machinery is as follows:

1) Release from the Reset state begins when the RST_N input is high†, and all of the core power supplies are above their required thresholds. These thresholds are listed in Table 2.4.

Supply	Parameter	Min	Max	Units
VA20	Power-on reset threshold for VA20 DC supply	1.70	1.80	V
VA10	Power-on reset threshold for VA10 DC supply	0.93	0.99	V
VDD	Power-on reset threshold for VDD DC supply	0.56	0.60	V

Table 2.4 **Power-On Reset Thresholds for Core Supply Voltages**

Note: Typically, power-on reset thresholds are 20% below the nominal value for analog DC power supplies. For example, for VA20 >1.68V nominal threshold value, and for VA10 > 0.96V nominal threshold value.

2) Once all of the conditions for release from Reset are true, a 20ms timer engages, the purpose of which is to allow the supplies to settle prior to allowing the PHY to boot.

3) After the 20ms timer has completed, hardware state machines designed to guarantee PLL and band-gap stability engage.

4) After the PLLs and band-gap are locked and functioning properly, the processor and digital circuitry are released from reset.

† Note that there are no timing requirements on issuance of reset relative to the clock.

5) The PHY image is then loaded through MDIO boot-load and the processor boots.

6) After the processor boots, any provisioned register values are set, and the PHY enters the provisioned operating state.

7) Once this is complete, the processor raises the MMD reset bits and sets the Reset Completed alarm, indicating it has completed reset and is ready for operation.

2.2.11 Configuration

The device family contains a number of static configuration pins that are used to set the power-up operation of the devices, and these signals currently include:

1) MDIO Address (ADDR[3:0])

2.3 Serial Flash

Table 2.5 shows the serial FLASH signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

The device family is capable of two modes of boot operation: MDIO boot-load and Daisy Chain master. When it is functioning in the Daisy Chain master mode, the device family has an attached SPI FLASH, and the PHY's firmware image is loaded from that FLASH.

Integrity checking of the loaded image is performed in hardware via the CRC that is embedded in the image. If there is an error, a reload is automatically requested. When functioning in MDIO boot-load mode, no FLASH device is required.

Instead, for this mode, the firmware image is loaded via the MDIO interface, and integrity checking of the loaded image is performed via a hardware CRC function on the memory interface. Before using MDIO boot-load, boot-load functions from the API should be carefully studied, or used verbatim.

2.3.1 SPI FLASH Interface

The SPI interface is responsible for connecting the device family to the external FLASH memory device. The microcontroller that resides on the device accesses the boot code and its corresponding default register values from the FLASH memory after power-on reset.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
SPI Chip Enable*	CE_N	F2	C6	O	This is a dual purpose pin. When PHY is in Master Mode, this pin acts as FLSH_CE_N (the SPI CE* signal from the device to the serial FLASH). On reset, this is set high. When PHY is in SLAVE Mode, pin acts as "TX_DC_RST_N" (daisy-chain transmit reset). This signal travels away from FLASH.
SPI Serial Clock	SCLK	E1	C8	O	This is a dual purpose pin. When PHY is in Master Mode, this pin acts as FLSH_SCK (the SPI clock from the device to the serial FLASH). On reset, this is set low. When PHY is in Slave Mode, this pin acts as "RX_DC_SOF" (daisy chain receive start of frame). This signal travels toward the FLASH.
SPI Serial Input Data	SIN	D1	F7	I	This is a dual purpose pin. When PHY is in Master Mode, this pin acts as FLSH_SI (the SPI input data from the serial FLASH to the device). When PHY is in Slave Mode, pin acts as "RX_DC_DATA" (daisy chain receive serial data). This signal travels toward the flash.

Table 2.5 **Serial FLASH Signals**

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
SPI Serial Output Data	SOUT	F1	C7	O	This is a dual purpose pin. When PHY is in Master Mode, this pin acts as FLSH_SO (the SPI output data from the device to the serial FLASH). On reset, this is set low. When PHY is in Slave Mode, this pin acts as "RX_DC_CLK" (daisy chain receive serial clock). This signal travels toward the flash.

Table 2.5 **Serial FLASH Signals** (continued)

This FLASH memory is also accessible via the MDIO interface for any firmware updates and manufacturing burn is done via the API, or via the registers in the Global MMD. The SPI interface is a four-wire, unidirectional, serial bus as shown in Figure 2.2, and is composed of the following:

1) A serial clock output: “SCLK”

2) A serial data output: “SOUT”

3) A chip-select: “CE*” (with all the signals being unidirectional)

4) A serial data input: “SIN”

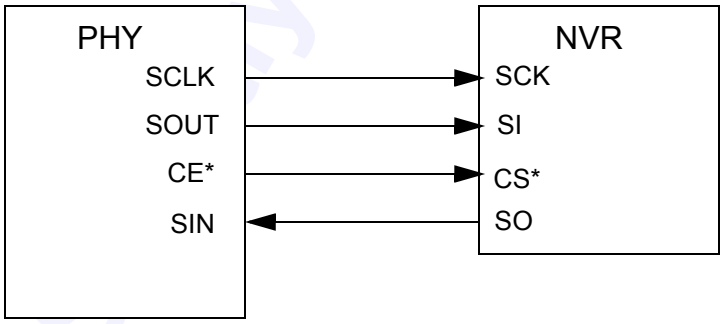


Figure 2.2 **SPI Interface Block Diagram**

The device family is set up to function as a Mode 0 (0,0) SPI device, which means that the clock defaults to zero when not bursting. Data on this interface, for both SIN and SOUT, is always sourced on the falling edge of SCLK, and sampled on the rising edge of SCLK.

Figure 2.3, Figure 2.4, and Figure 2.5 on page 47 show the typical read, burst read, and write operations for the device family. In all of these scenarios, use the API or the NVR interface in the Global MMD to access the FLASH.

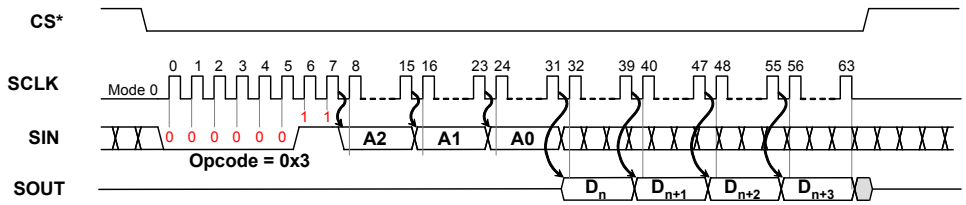


Figure 2.3 **SPI Read**

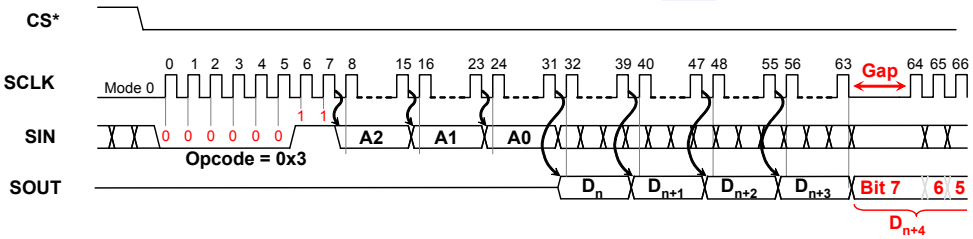


Figure 2.4 **SPI Burst Read**

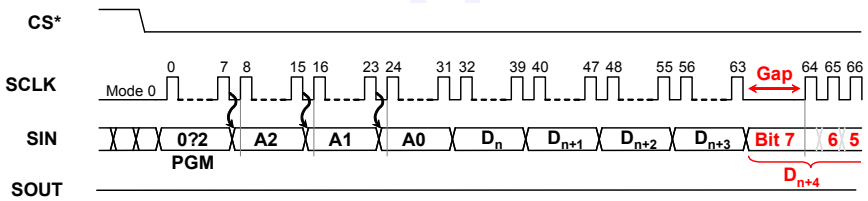


Figure 2.5 **SPI Burst Write**

The NVR interface in the device family is designed to be able to output any arbitrary opcode, followed by a programmable zero to three address bytes, which is followed by a programmable zero to four data bytes. This allows any variation of opcodes to be output to the attached FLASH device. This interface also supports a burst read and write mode, which keeps the CS* line pulled low to enable back-to-back reads and writes.

To support this, the NVR interface supports two 16-bit address registers and two 16-bit data registers. These registers allow up to 4 data bytes in a burst over the SPI interface. To extend this to even longer bursts, the device family halts the clock after the last bit in the data burst allowing the host processor to load another block of data *to/from* the NVR interface.

This is shown in Figure 2.4 on page 47 and Figure 2.5 on page 47, and this allows the data burst to be extended by as many bytes as necessary, without outstripping the MDIO's I/O capabilities.

Note that typical NVRs require that writing be performed on a block basis, and thus, the addresses usually wrap within the block being programmed. As such, it is desirable from a speed and efficiency perspective to attempt to write entire blocks, versus pieces of blocks. In order to assure that no polling is required on NVR interface, it is recommended that the NVR clock speed be set to at least[†]:

$$f_{\mathrm{SCLK}} > \frac{64}{63} \cdot f_{\mathrm{MDIO}}$$

Note: The desired FLASH memory should be chosen to be at least 512K bytes in size.

2.3.2 Boot-Load

Regardless if the PHY is a daisy-chain master, new images can be boot-loaded into the PHY's IRAM and DRAM via the MDIO interface. In addition, if a boot-load operation is desired as the product's standard operating mode, the FLASH can be depopulated, and the image always loaded on power-up. For more information on this mode of operation, refer to the API documentation (see "API", Aquantia Corporation on page 107).

2.4 Firmware

The device family contains a 32-bit microcontroller, and this microcontroller is designed to have its IRAM and DRAM loaded in any of the following ways: on power-up/reset from the attached FLASH, via the daisy-chain loading described in Section , or to have its boot image loaded by the host processor via the MDIO interface. Programming of the FLASH on the daisy-chain master device is done via the appropriate function in the API.

2.4.1 Provisionable Default

Another feature of the device family is its ability to change and store the default values of any field marked as "PD". A delta list of all defaults that are different from the hardware defaults are stored in the image, and during power-up, the PHY's microprocessor overwrites the hardware defaults with these new values.

[†] This is derived from the fact that the longest burst instruction on the SPI is 64 bits, at one bit per clock, whereas to write a register on the MDIO takes 64 clocks, and the data is not written until the last bit - hence the 63.

Provisioning new default values is done using the Aquantia Default Provisioning tool, and PHYs are identified by hop count, allowing each PHY to be uniquely provisioned.

2.4.2 Gang-Load

To save time on MDIO boot-loading operations, the device family supports a gang-load feature, whereby if there are multiple device family chips on a single MDIO bus, they may be simultaneously loaded with boot images.

This is done by temporarily setting all of the device's MDIO addresses to be the same, loading the boot image, and then toggling the MDIO Address Reset bit in the Global register MMD. This can also be handled using the API (for specific details, refer to the API documentation). One additional option is to enable MDIO broadcast on address 0.

2.5 Daisy Chain

Table 2.7 shows the Daisy Chain signals for the 7 mm x 11 mm package.

Note: The 7 mm x 7 mm package does not support daisy chain configuration.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Daisy-Chain Clock Output	TX_DC_CLK	E4	**Note:** This package does not support a daisy-chain configuration.	O	This is the daisy chain transmit serial clock and this signal travels away from FLASH.
Daisy-Chain Data Output	TX_DC_DATA	E6	**Note:** This package does not support a daisy-chain configuration.	O	This is the daisy chain transmit serial data and this signal travels away from FLASH.
Daisy-Chain Master*	DC_MASTER_N	G7	**Note:** This package does not support a daisy-chain configuration.	I	This is the daisy-chain mode control: 0=Daisy Chain Master 1=Daisy Chain Slave
Daisy-Chain Reset* Input	RX_DC_RST_N	E5	**Note:** This package does not support a daisy-chain configuration.	I	This is the daisy chain receive reset and this signal travels towards FLASH.
Daisy-Chain Start-of-Frame Output	TX_DC_SOF	D6	**Note:** This package does not support a daisy-chain configuration.	O	This is the daisy chain transmit start of frame and this signal travels away from FLASH.

Table 2.6 **Daisy Chain Signals**

2.6 SerDes

Table 2.7 shows the SerDes signals for both the 7 mm x 11 mm and 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Pin Number(s)		Type	Description
		7 mm x 11 mm	7 mm x 7 mm		
Lane 0 RX	RX_P RX_N	N2 N3	G1 H1	I	PHY 0 Physical Lane 0 differential RX of the device family SerDes interface. This lane can operate in KR, 2500BASE-X, and SGMII mode.
Lane 0 TX	TX_P TX_N	N6 N5	H8 G8	O	PHY 0 Physical Lane 0 differential TX of the device family SerDes interface. This lane can operate in KR, 2500BASE-X, and SGMII mode.

Table 2.7 **SerDes Signals**

The device family SerDes interface is both robust and flexible, and it provides the numerous loopback and diagnostic capabilities that can act to ease the system interface-PHY board design and bring-up, as well as AC JTAG. The interface is capable of providing arbitrary lane swapping and inversion.

In the transmit direction, there is a programmable 3 tap equalizer (1 precursor tap and 1 postcursor tap), as well as the ability to program the TX drive strength, and TX termination.

In the receive direction, there is programmable gain and programmable boost. The device family SerDes interface also contains diagnostic pattern generation and checking functionality as listed in the subsequent sections.

A key feature that the device family SerDes interface provides is its eye-diagram mode, which allows the device user to create an eye-diagram. To make use of this functionality, the appropriate API functions *must* first be called.

The parameters associated with the SerDes interface have provisionable default values; this means that the device family SerDes interface can be tailored to power-up with the optimal settings for any given application.

Test	Description	Generate	Check	Invert
x^9 PRBS	$x^9 + x^5 + 1$	X	X	X
x^{31} PRBS	$x^{31} + x^{28} + 1$	X	X	X
Square Wave	Clause 49.2.12	X	X	X
Pseudo-Noise		X	X	X
CRPAT	IEEE 802.3 Annex48A.4	X	X	X

Table 2.8 **KR Diagnostic Pattern Capabilities**

Test	Description	Generate	Check	Invert
CRPAT	IEEE 802.3 Annex48A.4	X	X	X

Table 2.9 **SGMII Diagnostic Pattern Capabilities**

2.7 SerDes System Interface (I/F) Start-Up

In start-up on the system interface side, the following are the different operating scenarios for the SerDes I/F:

a) 10G mode (KR/XFI)

b) 2500BASE-X mode

c) 1000BASE-X mode

d) XSGMII mode†

e) All-off mode

These different modes affect *only* the system interface, and function independently of whether the MDI or KR-look-aside interface is selected.

2.7.1 10G Mode

1) The 10G mode is the hardware default, and it is the one in which the device family comes up in as a pre-configured mode (KR/XFI), and transmits Local Faults/Idles, and remains in this state until a connection to a link partner is established.

† XSGMII is an extension of the Cisco SGMII protocol, which informs the system interface what the PHY has autonegotiated as a rate. The XSGMII extension as proposed by Aquantia uses this same mechanism, but also informs if there is a 10G connection. After receiving acknowledgment of a 10G connection, the PHY switches to the pre-configured 10G mode. For more details see XSGMII on page 56.

2) Once a connection to a link partner has been established, the device family stays in the pre-configured 10G mode, 1000BASE-X mode, or the 100M SGMII mode depending upon the autonegotiated line rate.

3) Once the SerDes interface has synchronized, traffic flows.

4) If the link fails and the system interface was in the 10G mode, the device family generates a Local Fault message towards the system interface, effectively restarting it. If the link had transitioned to 1G operation, the SerDes is restarted in 10G mode generating Local Faults/Idles.

5) Autonegotiation restarts after the link break timer expires.

2.7.2 2500BASE-X Mode

1) In this mode, the device family comes up in 2500BASE-X mode and transmits Idles, and remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the device family does one of the following: stays in 2500BASE-X mode, switches to the pre-configured 10G mode, or switches to the 1G or 100M SGMII mode, depending on what is the autonegotiated line rate.

3) Once the SerDes I/F has synchronized, traffic flows.

4) If the link fails and the system interface was in the pre-configured 10G mode (KR/XFI), the device family generates a Local Fault message towards the system interface, and effectively restarts in 2500BASE-X mode, generating Idles.

   Otherwise, the link remains in 2500BASE-X mode and continues generating Idles.

5) Autonegotiation restarts after the link break timer expires.

2.7.3 1000BASE-X Mode

1) In this mode, the device family comes up in 1000BASE-X mode and transmits Idles, and remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the device family does one of the following: stays in 1000BASE-X mode, switches to the pre-configured 10G mode, or switches to the 100M SGMII mode, depending upon what is the autonegotiated line rate.

3) Once the SerDes interface has synchronized, traffic flows.

4) If the link fails and the system interface was in the pre-configured 10G mode (KR/XFI), the device family generates a Local Fault message towards the system interface, and effectively restarts in 1000BASE-X mode, generating Idles. Otherwise, the link just stays in 1000BASE-X mode generating Idles.

5) Autonegotiation restarts after the link break timer expires.

2.7.4 XSGMII Mode

1) In this mode, the device family comes up in XSGMII mode. After sending and receiving an ACK on an XSGMII link-down autonegotiation message (for more information, see Table 2.10 on page 57), the SerDes transmits Idles, and it remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the device family sends an XSGMII Link Up autonegotiation message with the appropriate rate† (see Table 2.10 on page 57), and receives an ACK.

3) Upon receiving an acknowledge from the system interface, the device family does one of the following: switches to the 100M SGMII mode, stays in 1G SGMII mode (essentially 1000BASE-X), or switches to the pre-configured 10G mode (KR/XFI/USXGMII), depending on what was the autonegotiated line rate (10G, 1G, or 100M).

4) Once the SerDes interface has synchronized, traffic flows.

5) If the link fails, and the device family was in the pre-configured 10G mode, the device generates a Local Fault message towards the system interface, and then transitions back to XSGMII mode.

   At this point, it then sends and receives an ACK on an XSGMII link-down autonegotiation message, and then resumes transmitting Idles.

   If the link fails and the device was in 1G SGMII mode, it first sends and receives an ACK on an XSGMII link-down autonegotiation message, and then it resumes transmitting Idles, without any interruption to SerDes operations.

† The SGMII autonegotiation machinery was derived from 1000BASE-X and involves exchanging 16-bit control words via /C and /I ordered sets. It was adopted for SGMII to solve the issue of how a copper SFP module would inform the system interface what rate it had autonegotiated on the line, without having an MDIO interface (SFP-only support).

However, if the system interface was in the 100M SGMII mode, then the SerDes transitions back to XSGMII mode, at which point it sends and receives an ACK on an XSGMII link-down autonegotiation message, and then resumes transmitting Idles.

6) Autonegotiation restarts after the link break timer expires.

2.7.5 USXGMII Mode

1) In this mode, the device family comes up in USXGMII mode. After it sends and receives an ACK on an USXGMII link-down autonegotiation message (for more information, see Table 2.11 on page 58), the SerDes transmits Idles, and remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the device family sends an USXGMII Link Up autonegotiation message with the appropriate rate† (see Table 2.11 on page 58), and receives an ACK.

3) Upon receiving the acknowledge from the system interface, the device family switches to the desired rate, depending on what was the autonegotiated line rate (100M, 1G, 2.5G, 5G, or 10G).

4) Once the SerDes interface has synchronized, traffic flows.

5) If the link fails, the device family generates a Local Fault message towards the system interface, and then transitions back to USXGMII Idle mode, where it sends and receives an ACK on an USXGMII link-down autonegotiation message, and then resumes transmitting Idles.

6) Autonegotiation restarts after the link break timer expires.

2.7.6 All-Off Mode

1) In this mode, the device family comes up with the system interface off, and it remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the device family does one of the following: turns on the pre-configured 10G mode (XFI/KR), 2500BASE-X, 1000BASE-X, or the 100M SGMII mode, depending on what was the autonegotiated line rate.

† The SGMII autonegotiation machinery was derived from 1000BASE-X and involves exchanging 16-bit control words via /C and /I ordered sets. It was adopted for SGMII to solve the issue of how a copper SFP module would inform the system interface what rate it had autonegotiated on the line, without having an MDIO interface (SFP-only support).

3) Once the SerDes interface has synchronized, traffic flows.

4) If the link fails and it was in the pre-configured 10G mode, the device family generates a Local Fault message towards the system interface, and then shuts off. Otherwise, the system interface just shuts off.

5) Autonegotiation restarts after the link break timer expires.

2.7.7 Interrupts

In all of these modes, the processor has the ability to generate an interrupt upon completing autonegotiation.

2.7.8 XSGMII

XSGMII is an extension of the SGMII interface and provides the signaling and control for moving to a 10G connection mode, in addition to the supported SGMII rates of 1G and 100M.

XSGMII builds upon the existing specification for SGMII, and the existing 10GE specifications defined in 802.3-2005 (for details, see “Serial-GMII Specification Version 1.8“, Document ENG-46158, Cisco Systems, April 27, 2005 on page 107).

The creation of XSGMII requires a minimal change to existing SGMII specification; namely, there is the addition of a 10G connect rate, as described in the following sequence:

1) System interface and PHY connect and synchronize the SGMII 1.25 Gb/s 8B/10B SerDes link.

2) PHY uses Clause 28 autonegotiation over the MDI to establish a connection with the remote PHY, which is constrained by the abilities the local system interface communicated during step 1, above.

3) PHY uses SGMII (Clause 37) autonegotiation to inform the system interface which rate it is selecting.

4) If a 10G connection is established, after receiving an acknowledgment from the system interface, the PHY switches over to 10G operation and traffic begins to flow once the 10GBASE-T training sequence has been completed.

5) If a 100M or 1G connection is established, after receiving an acknowledgment from the system interface, the PHY stays in SGMII mode, and traffic begins to flow once the link has been established.

The sequence steps just described require that the modifications to Table 1 of the SGMII specification as shown in Table 2.10, with the key modification being indicated in red.

Bit Number	tx_config_Reg[15:0] sent from PHY to System Interface	tx_config_Reg[15:0] sent from System Interface to PHY
15	Link: 1 = link up Link: 0 = link down	0: Reserved for future use
14	Reserved for Auto-Negotiation acknowledge as specified in 802.3z	1
13	0: Reserved for future use	0: Reserved for future use
12	Duplex mode: 1 = full duplex (required)	0: Reserved for future use
11:10	Speed: Bit 11, 10 **1 1 = 10 Gbps: 10GBASE-T, 10GBASE-R** 1 0 = 1000 Mbps: 1000BASE-TX, 1000BASE-X 0 1 = 100Mbps: 100BASE-TX, 100BASE-FX 0 0 = 10Mbps: 10BASET, 10BASE2, 10BASE5	0: Reserved for future use
9:1	0: Reserved for future use	0: Reserved for future use
0	0	1

Table 2.10 **XSGMII Base Page**

2.7.9 USXGMII

USXGMII is an extension of the XFI interface and provides the signaling and control for moving to a 100M, 1G, 2.5G, and 5G connection mode, in addition to the XFI rates of 10G.

USXGMII builds upon the existing specification for XFI and the existing 10GE specifications defined in 802.3-2005 (for details, see “Serial-GMII Specification Version 1.8“, Document ENG-46158, Cisco Systems, April 27, 2005 on page 107).

The creation of USXGMII requires that a minimal change be made to the existing XFI specification. For example, the addition of 100M, 1G, 2.5G, and 5G connection rates as described in the following sequence:

1) System interface and PHY connect and synchronize the XFI 10.3125 Gb/s 64B/66B SerDes link.

2) PHY uses Clause 28 autonegotiation over the MDI to establish a connection with the remote PHY, which is constrained by the abilities the local system interface communicated during step 1, above.

3) PHY uses SGMII (Clause 37) autonegotiation to inform the system interface about the rate it is selecting.

4) If a 10G connection is established, after receiving the acknowledgment from the system interface, the PHY switches over to 10G operation and traffic begins to flow once the 10GBASE-T training sequence completes.

5) If a 100M, 1G, 2.5G, or 5G connection is established, after receiving an acknowledgment from the system interface, the PHY stays in SGMII mode and traffic begins to flow after the link is established.

Table 2.11 shows the USXGMII Base Page.

Bit Number	usxgmiiChannelInfo[15:0] sent from PHY to System Interface	usxgmiiChannelInfo[15:0] sent from System Interface to PHY
15	Link: 1 = link up, 0 = link down	0: Reserved for future use
14	Reserved for Auto-Negotiation acknowledge	1
13	0: Reserved for future use	0: Reserved for future use
12	Duplex mode: 1 = full duplex (required) 0 = half duplex	0: Reserved for future use
11:9	Speed: Bit 11, 10, 9 0 0 0 = 10Mbps: 10BASET, 10BASE2, 10BASE5 0 0 1 = 100Mbps: 100BASE-TX, 100BASE-FX 0 1 0 = 1000 Mbps: 1000BASE-TX, 1000BASE-X 0 1 1 = 10 Gbps: 10GBASE-T, 10GBASE-R 1 0 0 = 2500 Mbps: AQrate 2.5G 1 0 1 = 5000 Mbps: AQrate 5G 1 1 0 = Reserved 1 1 1 = Reserved	0: Reserved for future use
8	EEE capability: 1= supported, 0 = not supported	0: Reserved for future use
7	EEE clock stop capability: 1= supported, 0 = not supported	0: Reserved for future use
6:1	0: Reserved for future use	0: Reserved for future use
0	1 = USXGMII supported device	1

Table 2.11 **USXGMII Base Page**

2.8 MDI

Table 2.12 represents the MDI signals and pins for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

In 10G mode, the line interface on the device family is capable of driving up to 100 meters of Cat 6a unshielded twisted pair, or 100 meters of Cat 7 shielded cable (100Ω differential impedance). The device family is also capable of driving up to 55 meters of Cat 6 cable, and a lesser distance using Cat 5e cable†.

In 2.5G and 5G modes, the device family can drive 100 meters using Cat 5e (or better) cable. In the 1G, or 100M modes, it can drive up to 130 meters using Cat 5e (or better) cable. The device family is designed to drive this via a quad, 50Ω, center-tapped 1:1 transformer connected to an RJ-45 PCB-mount jack.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Pair A	A_P A_N	C1 B1	B1 B2	I/O	PHY 0 Pair A of the device family line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.
Pair B	B_P B_N	A2 A3	A1 A2	I/O	PHY 0 Pair B of the device family line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.
Pair C	C_P C_N	A6 A5	A8 A7	I/O	PHY 0 Pair C of the device family line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.

Table 2.12 **MDI Signals**

† This distance is indeterminate because Cat 5e cable performance is not specified past 100MHz (for details, see “Information Technology - Generic cabling for customer premises”, ISO/IEC 11801, Second edition 2002-09 on page 107).

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Pair D	D_P D_N	A8 B8	B8 B7	I/O	PHY 0 Pair D of the device family line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.

Table 2.12 **MDI Signals** (continued)

The device family line interface supports automatic A/B and C/D pair swaps, polarity inversions, auto-X (MDI versus MDI-x operations), and semi-cross (A/B or C/D only).

In addition, it also supports provisionable ABCD to DCBA pair reversal for ease of routing with stack-jacks via bit 1.E400.1:0. Note that this reversal does not swap polarities (thus, A+ maps to D+, etc.).

2.9 Timing

The device family contains a high-performance synthesizer that is capable of producing all of the clocks required internally, as well as sourcing the recovered 50MHz CMOS clock for use by other components in the system.

This synthesizer operates from either an external 350µW 50.000MHz crystal or from a differential 50MHz clock. The 50MHz CMOS clock output is synchronized to the recovered clock, and is thus capable of being used in a synchronous Ethernet application. Enabling of this is done via the Global MMD.

Table 2.13 on page 61 shows the timing signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Clock Source Select	XTAL_SELECT_N	K7	F8	I	The 50MHz reference clock source selector for the device family. When XTAL_SELECT_N is pulled low, the XTAL_I and XTAL_O pins operate in crystal mode; otherwise they operate in LVDS oscillator input mode.
Crystal Input	XTAL_I	E8	D8	I	The 50MHz reference clock input for the device family. When XTAL_SELECT_N is pulled low, these pins operate in crystal mode. Otherwise, they are the differential LVDS inputs for an external oscillator, with XTAL_I being the positive input and XTAL_O being the negative input. In oscillator mode, this DC-coupled input has an internal 100Ω termination resistor associated with it.
Crystal Output	XTAL_O	D8	E8	O	The 50MHz crystal oscillator output of the device family. This connects to the output of an inverting amplifier. In XO mode, this is high-impedance.

Table 2.13 **Timing Signals**

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
PTP/1588 Sync	SYNC_1588	E2	D1	I	This is the PTP sync input used to align the PTP clocks on multiple PHYs on a platform to have the same time. The PHY timestamps the rising edge of this input and this timestamp can then be used on each of the PHYs to perform the alignment.
PTP External Clock	CLK_1588_P CLK_1588_N	H1 G1	N/A **Note:** This package does not support these pins.	I - LVDS	This is the PTP differential LVDS clock input. This input has a 100Ω termination resistor associated with it, and it will operate in the frequency range of 40MHz to 100MHz. This pin should be AC coupled.
Sync-E Primary Clock	CLKO_50M_A	G8	C3	O	The primary recovered clock output used for synchronous Ethernet (Sync-E).
Sync-E Secondary Clock	CLKO_50M_B	K4	D3	O	The secondary recovered clock output used for synchronous Ethernet (Sync-E).
Clock Frequency Select	CLK50M_SELECT_N	K5	N/A **Note:** This package does not support this pin.	I	This is the clock frequency select input used for selecting either 50MHz or 156.25MHz. When this signal is pulled low, the input clock is 50MHz. When this signal is pulled high, the input clock is 156.25MHz.

Table 2.13 **Timing Signals** (continued)

2.10 LED

The device family supports three 20mA, open-drain CMOS LED outputs. The configuration of the LEDs is done via the API.

Table 2.14 shows the LED signals for both the 7 mm x 11 mm package and the 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
LED [2:0]	LED0 LED1 LED2	H2 G2 G3	D6 F3 G6	O	LED0 output for PHY 0. These lines sense whether the LED is pulled high or low and drive accordingly. The configuration state of the LEDs is visible in the register space. On reset, these pins are set to high impedance.

Table 2.14 **LED Signals**

2.11 Reference Resistors

Table 2.15 shows the reference resistor signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

Note: The device family design relies on 1% precision resistors to calibrate its internal voltage levels.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Bandgap Reference Resistor	RREF_BG	B7	B5	Analog	The connection point for the bandgap reference resistor. This should be a precision 1%, 2.00kΩ resistor tied to ground.

Table 2.15 **Reference Resistor Signals**

2.12 JTAG/Test

The device family design supports an IEEE 1149.1 compliant JTAG interface, with 1149.6 AC JTAG support on the SerDes interface. Note that for normal operation, TRST_N should be held low.

Table 2.16 shows the JTAG and test signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
JTAG Clock	TCK	M1	C2	I	This is the JTAG clock input.
JTAG Data Input	TDI	L1	G7	I	This is the JTAG data input signal. This input has a pull-down that is associated with it.
JTAG Data Output	TDO	K1	H3	O	This is the JTAG data output signal. This is a 12mA output and it has a pull-down associated with it.
JTAG Reset	TRST_N	J3	H4	I	This is the JTAG reset signal. If JTAG is not used, this pin *must* be pulled low.
JTAG Test Mode State	TMS	J2	C1	I	This is the JTAG test mode state signal.

Table 2.16 **JTAG/Test Signals**

2.13 Debug

The device family supports a side-access port to the MDIO register space via a slave SMBus. Addressing for this SMBus is provisioned on a per PHY basis.

Note: It is recommended that every design connect these SMBus pins to a header to allow in-system debug. This removes the need to disconnect the MDIO lines, and allows for normal system operations to occur during debug.

Table 2.17 shows the debug signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Slave SMBus	SMB_DAT SMB_CLK	M8 L7	G4 E2	I/O	Data an clock signals for slave SMBus used for the debug port into the PHY MDIO register space, and these signals require an external pull-up to VDD_IO.

Table 2.17 **Debug Signals (7 mm x 11 mm Package)**

2.14 Power

The device family utilizes the following separate power supplies to minimize power consumption:

1) VDD
2) 1.0V
3) 2.0V

As mentioned previously, to provide flexibility for implementation, the device family design utilizes a programmable I/O voltage. The logic thresholds for the I/O are set at 70% and 30% of VDD_IO for V_{IH}/V_{OH} and V_{IL}/V_{OL}, respectively.

The VDD_IO voltage level affects MDC, MDIO, INT_N, and RST_N:

1) When the VDD_IO is set for 1.8V operation, the MDIO_1P8_SELECT_N pin *must* be pulled to ground.
2) When the VDD_IO is set for 3.3V operation, the MDIO_1P8_SELECT_N pin *must* be pulled to VDD_IO.

Table 2.18 shows the power signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
AVDD10	VA10	C6 D5	B4	Power	1.0V analog supply.
AVDD20	VA20	C4 D3	A5	Power	2.0V analog supply.
AVSS	AVSS	A1 A4 A7 B2 B3 B5 B6 C3 C5 C8 D4 D7	A3 A6 B3 B6	Power	Analog ground.
AVSS PLL	AVSS_PLL	B4	A4	Power	Analog ground for PHY PLL.
VDD	VDD	C2 C7 F5 F7 G4 G6 H5 H7 J4 J6 L3	C5 D4 E3 E5 F4	Power	0.7V digital supply.

Table 2.18 **Power Signals**

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
VDD IO Power Supply	VDD_IO	M6	F2 F6	Power	The power supply for the general I/O on the device family. High and low logic levels are scaled to 70% and 30% of the supply voltage, respectively.
VSS	VSS	E3 E7 F4 F6 G5 H4 H6 J5 L2 L6	C4 D5 E4 E6 F5	Power	Digital ground.
VSS SERDES	VSS_SRDS	M2 M3 N1 N4 N7	N/A **Note:** This package does not support these pins.	Power	SerDes ground.
V10_SRDS	V10_SRDS	L5	G5	Power	SerDes 1.0V digital supply
V20_SRDS	V20_SRDS	M4	G3	Power	SerDes 2.0V digital supply

Table 2.18 **Power Signals** (continued)

2.15 Reserved

Table 2.19 shows the reserved signals for both the 7 mm x 11 mm and the 7 mm x 7 mm packages.

Signal Name	Pin Name(s)	Package Pin Number(s)		Pin Type	Pin/Signal Description
		7 mm x 11 mm	7 mm x 7 mm		
Reserved No Connect (RNC)	RNC_J1 RNC_J7 RNC_K6 RNC_D7 RNC_H6	J1 J7 K6 -- --	-- -- -- D7 H6	N/A	Reserved no-connect signal.These pins must be left unconnected in the PCB design.
Reserved Ground (RG)	RG_D2 RG_N8 RG_E7	D2 N8 --	-- -- E7	I	Reserved ground signal. These pins must be connected to digital ground in the PCB design.
Floating	No Connect (NC)	K2 L4	N/A **Note:** This package does not support these pins.	N/A	These pins are floating in the package and they can be connected as conditions dictate.

Table 2.19 **Reserved Signals (7 mm x 11 mm Package)**

2.16 Pin-Out

The pin-out drawing for the AQR113-AQR114-AQR115 device, which is housed in a 7 mm x 11 mm, 104-pin FCBGA (8 rows x 13 rows) package, is shown in Figure 2.6 on page 69.

The pin-out drawing for the AQR113C-AQR114C-AQR115C device, which is housed in a 7 mm x 7 mm, 64-pin FCBGA (8 rows x 8 rows) package, is shown in Figure 2.7 on page 70.

Note: The signals are color coded to group similar functionalities together, and the pin-out drawing perspective view is looking from the top of the chip.

	1	2	3	4	5	6	7	8	
A	AVSS	B_P	B_N	AVSS	C_N	C_P	AVSS	D_P	A
B	A_N	AVSS	AVSS	AVSS_PLL	AVSS	AVSS	RREF_BG	D_N	B
C	A_P	VDD	AVSS	VA20	AVSS	VA10	VDD	AVSS	C
D	SIN	RG_D2	VA20	AVSS	VA10	TX_DC_SOF	AVSS	XTAL_O	D
E	SCLK	SYNC_1588	VSS	TX_DC_CLK	RX_DC_RST_N	TX_DC_DATA	VSS	XTAL_I	E
F	SOUT	CE_N	RST_N	VSS	VDD	VSS	VDD	ADDR0	F
G	CLK_1588_N	LED1	LED2	VDD	VSS	VDD	DC_MASTER_N	CLKO_50M_A	G
H	CLK_1588_P	LED0	VDD_IO_1P8_SELECT_N	VSS	VDD	VSS	VDD	MDIO	H
J	RNC_J1	TMS	TRST_N	VDD	VSS	VDD	RNC_J7	MDC	J
K	TDO	NC	RST_OUT_N	CLKO_50M_B	CLK50M_SELECT_N	RNC_K6	XTAL_SELECT_N	ADDR2	K
L	TDI	VSS	VDD	NC	V10_SRDS	VSS	SMB_CLK	INT_N	L
M	TCK	VSS_SRDS	VSS_SRDS	V20_SRDS	ADDR3	VDD_IO	ADDR1	SMB_DAT	M
N	VSS_SRDS	RX_P	RX_N	VSS_SRDS	TX_N	TX_P	VSS_SRDS	RG_N8	N
	1	2	3	4	5	6	7	8	

Figure 2.6 **AQR113-AQR114-AQR115 Pin-Out Drawing**

	1	2	3	4	5	6	7	8	
A	B_P	B_N	AVSS	AVSS_PLL	VA20	AVSS	C_N	C_P	A
B	A_P	A_N	AVSS	VA10	RREF_BG	AVSS	D_N	D_P	B
C	TMS	TCK	CLKO_50M_A	VSS	VDD	CE_N	SOUT	SCLK	C
D	SYNC_1588	MDIO	CLKO_50M_B	VDD	VSS	LED0	RNC_D7	XTAL_I	D
E	MDC	SMB_CLK	VDD	VSS	VDD	VSS	RG_E7	XTAL_O	E
F	VDD_IO_1P8_SELECT_N	VDD_IO	LED1	VDD	VSS	VDD_IO	SIN	XTAL_SELECT_N	F
G	RX_P	INT_N	V20_SRDS	SMB_DAT	V10_SRDS	LED2	TDI	TX_N	G
H	RX_N	RST_N	TDO	TRST_N	ADDR3	RNC_H6	RST_OUT_N	TX_P	H
	1	2	3	4	5	6	7	8	

Figure 2.7 **AQR113C-AQR114C-AQR115C Pin-Out Drawing**

Timing 3

3.1 MDIO

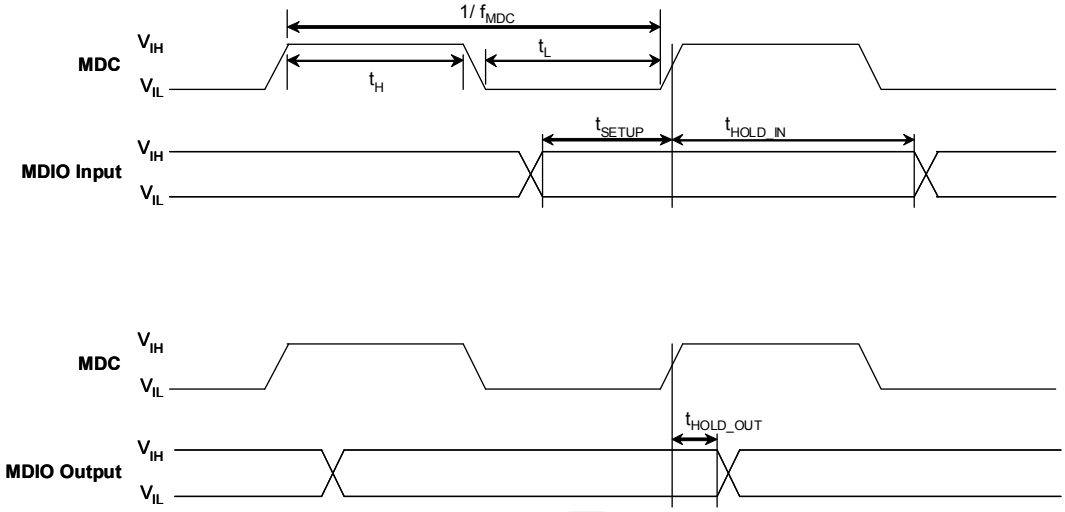


Figure 3.1 **MDIO Setup and Hold Times**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{MDC}	MDC Frequency				10.5	MHz
t_L	MDC Low Time		20			ns
t_H	MDC High Time		20			ns
t_{SETUP}	Input Setup Time		8			ns
t_{HOLD_IN}	Input Hold Time		10			ns
t_{HOLD_OUT}	Output Hold Time		29		38	ns

Table 3.1 **MDIO Timing**

Data is sampled on the rising edge of MDC at the PHY, and at the STA.

3.2 Interrupt

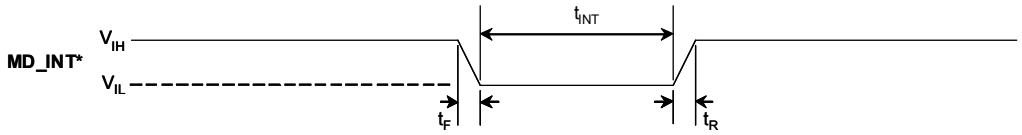


Figure 3.2 **Interrupt Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
t_F	Fall Time		1			ns
t_R	Rise Time		1			ns
t_{INT}	Interrupt Time		N/A[1]			ns

Table 3.2 **Interrupt timing**

1. INT* stays low until the interrupt is serviced.

3.3 Reset

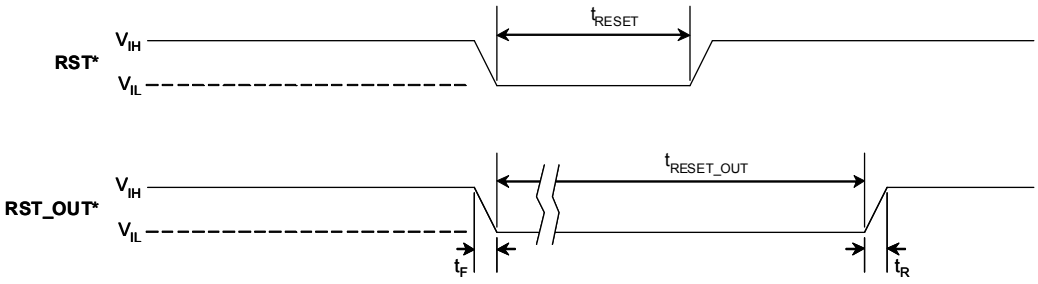


Figure 3.3 **Reset Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
t_{RESET}	Reset Time		100			ms
t_F	Fall Time		1			ns
t_R	Rise Time		1			ns
t_{RESET_OUT}	Reset Out Time	f_C = 50.00MHz	20			ms

Table 3.3 **Reset Timing**

3.4 SPI

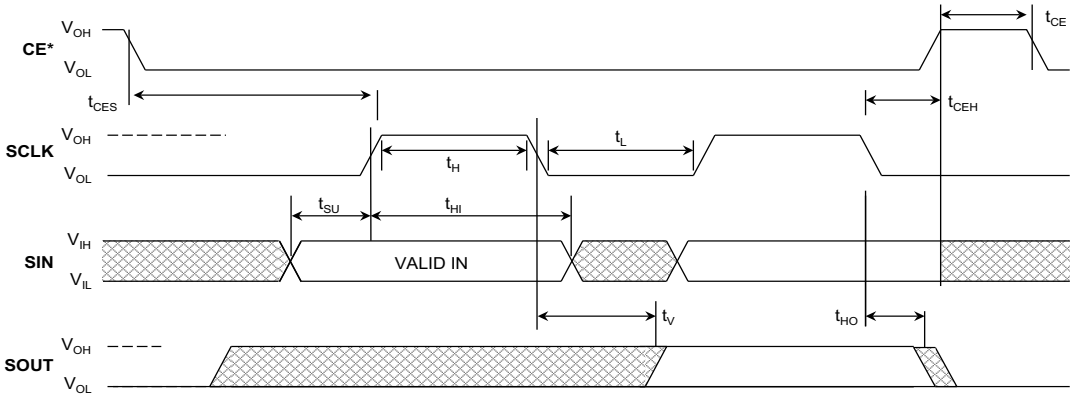


Figure 3.4 **SPI Timing Diagram**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
f_{SCLK}	SCLK Clock Frequency[1]		0		50.0	MHz
t_H	SCLK High Time		12			ns
t_L	SCLK Low Time		12			ns
t_{CE}	CE* High Time		50			ns
t_{CES}	CE* Setup Time		25			ns
t_{CEH}	CE* Hold Time		25			ns
t_{SU}	S_{IN} Setup Time		14			ns
t_{HI}	S_{IN} Hold Time		-4			ns
t_V	S_{OUT} Output Valid				4	ns
t_{HO}	S_{OUT} Hold Time		-4			ns

Table 3.4 **SPI Timing**

1. An attached FLASH device which supports 40MHz operation, must have a t_V (output valid time) of less than 12.5ns.

3.5 SerDes

The tables in this section provide the SerDes receive and transmit jitter tolerance specifications for the device family.

Maximum Total Jitter (TJ_{MAX})	Maximum Random Jitter (RJ_{MAX})	Maximum Data Dependent Jitter (DDJ_{MAX})	Maximum Deterministic Jitter (DJ_{MAX})	Maximum Periodic Jitter (PJ_{MAX})	Units
1.00	0.25	0.55	0.10	0.10	UIpp

Table 3.5 **SerDes Receive Jitter Tolerance Specifications**

Maximum Total Jitter (TJ_{MAX})	Maximum Random Jitter (RJ_{MAX})	Maximum Deterministic Jitter (DJ_{MAX})	Maximum Periodic Jitter (PJ_{MAX})	Units
0.25	0.15	0.05	0.05	UIpp

Table 3.6 **SerDes Transmit Jitter Tolerance Specifications**

The measurement bandwidth (BW) for these specs is from $\frac{f_{SYMBOL}}{1667}$ to ∞, as the tracking bandwidth of the PLL for the SerDes is up to $\frac{f_{SYMBOL}}{1667}$.

For instance, for KR, the symbol rate is 10.3125GHz, so $\frac{f_{SYMBOL}}{1667} \cong 6MHZ$. Thus, the measurement BW for the integrated jitter is from roughly 6MHz to infinity.

3.6 SGMII Transmit

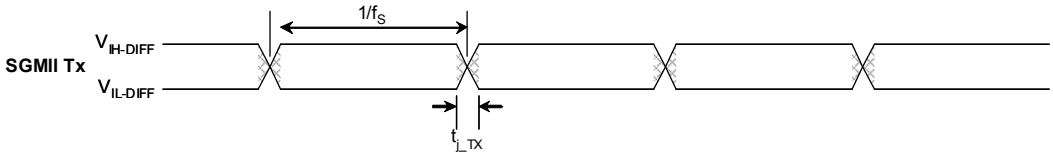


Figure 3.5 **SGMII Transmit Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_S	Symbol Rate			1.25		GS/s

Table 3.7 **SGMII Transmit Timing**

3.7 SGMII Receive

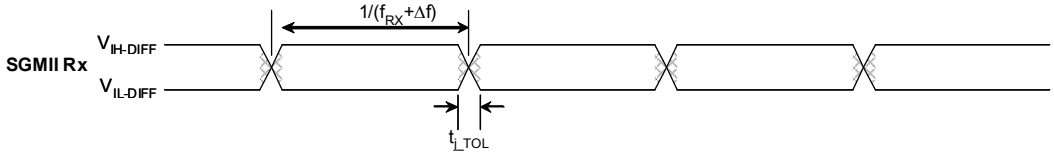


Figure 3.6 **SGMII Receive Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{RX}	Receive Symbol Rate			1.25		GS/s
Δ_f	Frequency Tolerance		-300		300	ppm

Table 3.8 **SGMII Receive Timing**

3.8 KR Transmit

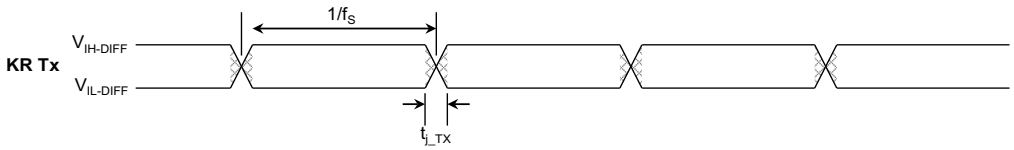


Figure 3.7 **KR Transmit Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_S	Symbol Rate			10.3125		GS/s

Table 3.9 **KR Transmit Timing**

3.9 KR Receive

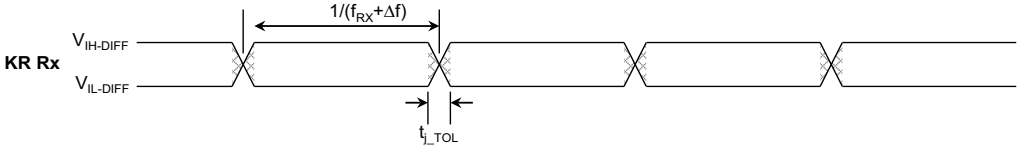


Figure 3.8 **KR Receive Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{RX}	Receive Symbol Rate			10.3125		GS/s
Δ_f	Frequency Tolerance		-50		50	ppm

Table 3.10 **KR Receive Timing**

3.10 2500BASE-X Transmit

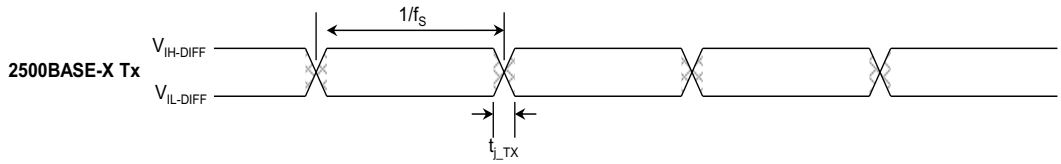


Figure 3.9 **2500BASE-X Transmit Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_S	Symbol Rate			3.125		GS/s

Table 3.11 **2500BASE-X Transmit Timing**

3.11 2500BASE-X Receive

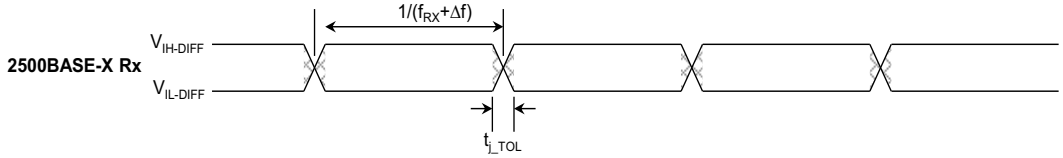


Figure 3.10 **2500BASE-X Receive Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{RX}	Receive Symbol Rate			3.125		GS/s
Δ_f	Frequency Tolerance		-300		300	ppm

Table 3.12 **2500BASE-X Receive Timing**

3.12 Clocks

3.12.1 Input

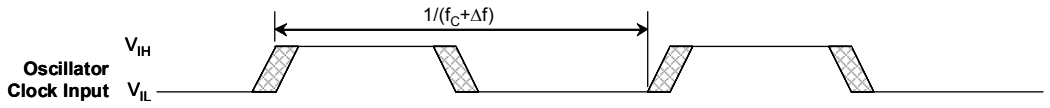


Figure 3.11 **50MHz Input Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_C	Clock Frequency			50.0		MHz
Δ_f	Frequency Tolerance		-50		50	ppm
t_j	RMS Jitter[1]	12KHz - 20MHz			1.0	ps
DC	Duty Cycle		45		55	%

Table 3.13 **50.000MHz Input Timing**

1. This includes all period jitter and tones.

The phase noise of the 50MHz input clock should be at least as good as the mask shown in Figure 3.12:

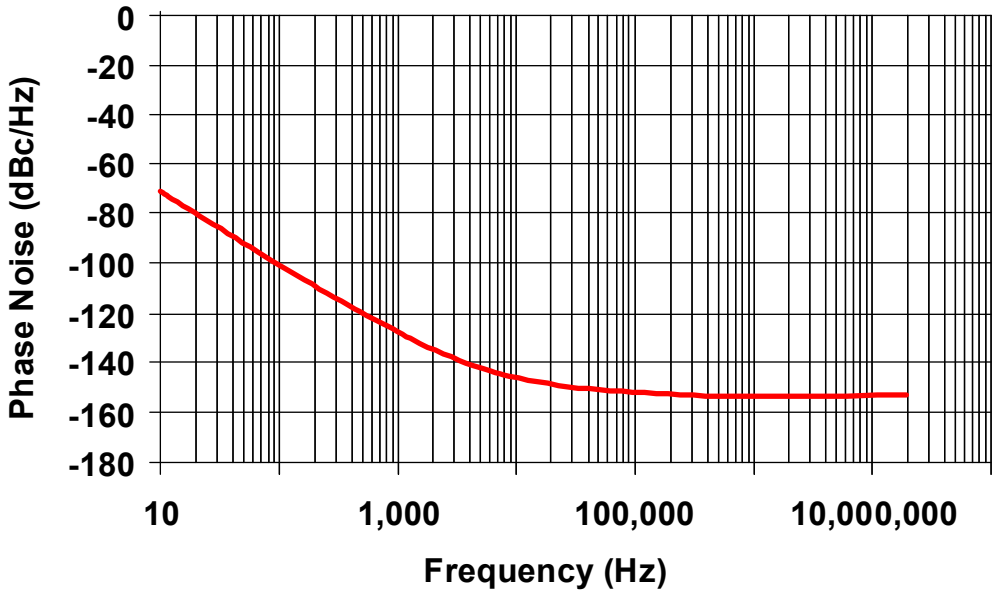


Figure 3.12 **50.000MHz Phase Noise Mask**

3.12.2 Output

Table 3.14 lists the device family 50MHz reference clock output timing information for its output clock (CLKO_50M_A). Note that the 50MHz clock is phase-locked to the incoming receive signal in both 1G and 10G slave modes. The result is that the frequency accuracy in these modes is a function of the corresponding far-end device's clock accuracy.

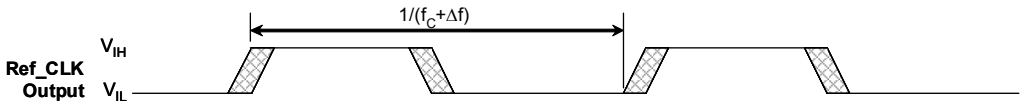


Figure 3.13 **50MHz Reference Clock Output Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_C	Clock Frequency			50.000		MHz
Δ_f	Frequency Tolerance		-50		50	ppm
t_j	RMS Period Jitter				1	ps
t_L	Clock Low Time		8		12	ns
t_H	Clock High Time		8		12	ns
t_R/t_F	Clock Rise/Fall Time	6pF load		2		ns
DC	Duty Cycle		45		55	%

Table 3.14 **50MHz Reference Clock Output Timing**

3.13 JTAG/Test

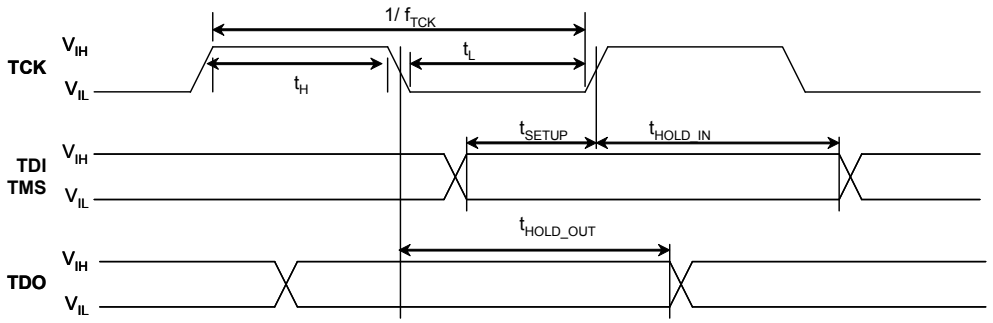


Figure 3.14 **JTAG/Test Timing Diagram**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{TCK}	Clock Frequency				20	MHz
t_L	Clock Low Time		20			ns
t_H	Clock High Time		20			ns
t_{SETUP}	Input Setup Time		10			ns
t_{HOLD_IN}	Input Hold Time		15			ns
t_{HOLD_OUT}	Output Hold Time		4		22	ns

Table 3.15 **JTAG/Test Timing**

Electrical Specifications 4

4.1 Absolute Maximum Ratings

Stresses that exceed the absolute maximum ratings listed in Table 4.1 may cause permanent device failure. Functionality at or exceeding these limits is not recommended nor implied. Any exposure to absolute maximum ratings for an extended period may affect device reliability.

Symbol	Parameter	Test Condition	Min	Max	Units
VDD	0.7V Digital Supply		-0.5	0.935	V
VA10	1.0V Analog Supply		-0.5	1.32	V
VA20	2.0V Analog Supply		-0.5	2.31	V
VDD_IO	1.8V VDD General I/O Supply		-0.5	1.98	V
	3.3V VDD General I/O Supply		-0.5	3.63	V
T_{STORE}	Storage Temperature		-55	150	°C

Table 4.1 **Device Family Absolute Maximum Ratings**

4.2 Recommended Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
VDD[1]	0.7V Supply		0.665	0.7	0.735	V
VA10[2]	1.0V Supply		0.95	1.0	1.05	V
VA20[3]	2.0V Supply		1.9	2.0	2.1	V
VDD_IO	1.8V I/O Supply		1.71	1.8	1.89	V
	3.3V I/O Supply		3.135	3.3	3.456	V
T[4]	Operating Temperature	Commercial Grade	0		108	°C
T_{JST}	Short-Term Junction Temperature		--		110	°C

Table 4.2 **Device Family Recommended Operating Conditions**

1. VDD includes the following supplies: VDD and VDD_SRDS.
2. VA10 includes the following supplies: VA10 and V10_SRDS.
3. VA20 includes the following supplies: VA20 and VA20_XTAL.
4. Minimum specification is ambient temperature and the maximum specification is junction temperature.

4.3 Power

The device family automatically adjusts is power consumption based on the length of the channel; consequently, there is no explicit “short-reach mode”†. However, the power consumption of the device family can be characterized over the IEEE 30-meter short-reach channel.

The following tables specify the power supply requirements and the operating current/power for the port for the device family in terms of both the full-reach and short-reach operation modes.

4.3.1 Operating Modes

The device family has several different operating regimes that each use different amounts of power, and these regimes are listed as follows:

1) **Low power (LP)**: In this mode, everything is shut off except for the internal microprocessor and the MDIO interface. This mode is designed for out-of-service ports, and is the lowest power operating mode.

2) **Autonegotiation (ANEG)**: In this mode, the device family attempts to autonegotiate with the far-end PHY, and is sending and trying to receive link pulses. This is second lowest power operating mode, and it usually lasts between 1.6 and 1.8 seconds‡.

3) **Training (TRNG)**: This is the highest power mode, and it occurs at the beginning of a 10GBASE-T/ 5GBASE-T/2.5GBASE-T/1000BASE-T/ 100BASE-TX/10BASE-T link training session. This training mode lasts for a maximum of 2 seconds. This sets the maximum requirements for the VA10, VA20, and VDD power supplies.

4) **10G Steady-State Operation (10GSS)**: This is the second highest power mode, and it occurs during normal steady-state link operations. This sets the maximum requirements for the thermal design, and is the maximum for the VDD power supply.

5) **5G Steady-State Operation (5GSS)**: This is the power mode seen during normal 5GBASE-T operations.

† Thus, when PHY power consumption is characterized at 30 meters, this is simply what represents the power consumption of the PHY when it is operating on a 30-meter link.

‡ This autonegotiation time assumes that an active link-partner is present. If one is not present, the device family continues attempting to autonegotiate until a PHY connection is made.

6) **2.5G Steady-State Operation (2.5GSS)**: This is the power mode seen during normal 2.5GBASE-T operations.

7) **1G Steady-State Operation (1GSS)**: This is the power mode seen during normal 1000BASE-T operations.

8) **100M Steady-State Operation (100MSS)**: This is the power mode seen during normal 100BASE-TX operations.

An example of the power consumption versus time for some of these modes in 10G operation is shown in Figure 4.1.

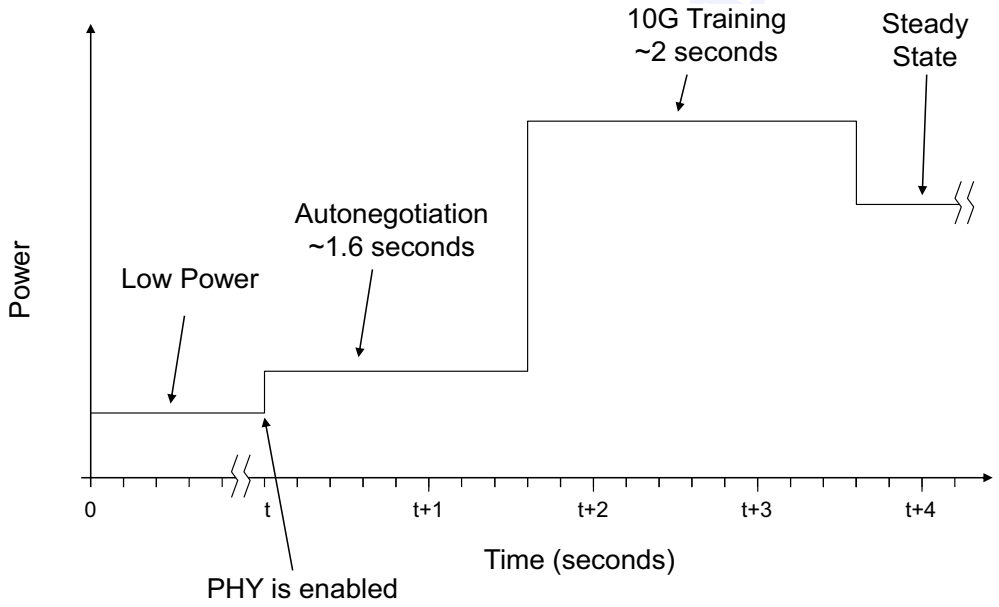


Figure 4.1 **Power Versus Time**

In Figure 4.1, the device starts off in low-power mode, and then at time *t*, the device family is enabled, and autonegotiation begins.

After 10GBASE-T is agreed on as the connection rate, 10GBASE-T training starts, and then after 2 seconds, it enters into the 10GBASE-T steady-state.

4.3.2 Latency

The device family is designed to minimize latency, which represents the time period between the request and the response to transfer data from one location to another at a specific rate.

Table 4.3 lists some example transmission rates that are available in the device family compared to IEEE specification standards for the following network rates:

• 10G
• 5G
• 2.5G

Network Rate	Latency Value	IEEE Specification Value
10G	1.3µS	2.5µS
5G	1.5µS	2.87µS
2.5G	2.7µS	5.12µS

Table 4.3 **Example Latency Values per Network Rates**

4.4 Power Supplies

This section provides information about the power supplies for the device family.

4.4.1 VA20, VA10, and VDD Supply Specifications

Table 4.4 provides the DC and AC power supply requirements for the device family:

• VA20 includes the following supplies: VA20 and VA20_XTAL
• VA10 includes the following supplies: VA10 and V10_SRDS
• VDD includes the following supplies: VDD and VDD_SRDS

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$VA20_{TOTAL}$	Input Voltage[1]		TBD	TBD	TBD	V
$VA20_{RIPPLE}$	Input Voltage Ripple	Peak-to-Peak	TBD	TBD	TBD	mV
$VA10_{TOTAL}$	Input Voltage[1]		TBD	TBD	TBD	V
$VA10_{RIPPLE}$	Input Voltage Ripple	Peak-to-Peak	TBD	TBD	TBD	mV
$V_{VDDTOTAL}$	Input Voltage[1]		TBD	TBD	TBD	V
$V_{VDDRIPPLE}$	Input Voltage Ripple	Peak-to-Peak	TBD	TBD	TBD	mV

Table 4.4 **VA20, VA10, and VDD Electrical Parameters**

1. The input voltage is specified as DC accuracy.

4.5 Other Power Supplies

4.5.1 VDD_IO Supply Specifications

Table 4.5 provides DC and AC power supply requirements for the VDD_IO supply for the device family. Note that VDD_IO operates at either 1.8V or 3.3V.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
VDD_IO_{TOTAL}	1.8V Input Voltage[1, 2]		TBD	TBD	TBD	V
	3.3V Input Voltage[1, 2]		TBD	TBD	TBD	V
VDD_IO_{RIPPLE}	1.8V Input Voltage Ripple	Peak-to-Peak	TBD	TBD	TBD	mV
	3.3V Input Voltage Ripple	Peak-to-Peak	TBD	TBD	TBD	mV

Table 4.5 **VDD_IO Electrical Parameters**

1. The input voltage is specified as DC accuracy.
2. VDD_IO current varies with the MDIO load/activity and non-management I/O usage. Aquantia Corp. has reserved 100mA per port on the reference test boards as a worst-case condition.

4.6 Steady-State Operating Conditions

4.6.1 Typical Steady-State Operating Conditions

Table 4.6 provides the typical port steady-state current and power for the device family.

Symbol	Parameter	Test Condition	10G[1]	5G[2]	2.5G[3]	Units
$I_{VA20TOTAL}$	Input Current	Steady-State (typical)	TBD	TBD	TBD	mA
$I_{VA10TOTAL}$	Input Current	Steady-State (typical)	TBD	TBD	TBD	mA
$I_{VDDTOTAL}$	Input Current	Steady-State (typical)	TBD	TBD	TBD	mA
$P_{TOTAL\_TYP\_SS}$	Power	Steady-State (typical)	TBD	TBD	TBD	W

Table 4.6 **Typical Steady-State Parameters**

1. Typical supplies, 30 meters Cat 6A, $T_J = 70^oC$.
2. Typical supplies, 30 meters Cat 5e, $T_J = 70^oC$.
3. Typical supplies, 30 meters Cat 5e, $T_J = 70^oC$.

4.6.2 Maximum Steady-State Operating Conditions

Table 4.7 provides the maximum port steady-state current and power for the device family.

Symbol	Parameter	Test Condition	10G[1]	5G[2]	2.5G[3]	Units
$I_{VA20TOTAL}$	Input Current	Steady-State (maximum)	TBD	TBD	TBD	mA
$I_{VA10TOTAL}$	Input Current	Steady-State (maximum)	TBD	TBD	TBD	mA
$I_{VDDTOTAL}$	Input Current	Steady-State (maximum)	TBD	TBD	TBD	mA
$P_{TOTAL\_MAX\_SS}$	Power	Steady-State (maximum)	TBD	TBD	TBD	W

Table 4.7 **Maximum Steady-State Parameters**

1. Maximum supplies, 100 meters Cat 6A, T_J = 108°C.
2. Maximum supplies, 100 meters Cat 5e, T_J = 108°C.
3. Maximum supplies, 100 meters Cat 5e, T_J = 108°C.

4.7 Instantaneous Current Consumption

Table 4.8 provides the maximum port transient current during training for the device family. These values do not necessarily take place simultaneously, and are intended to be used for voltage regulator (VR) design.

Note: The listed values are not representative of the device under steady-state operation.

Symbol	Parameter	Test Condition	10G[1]	5G[2]	2.5G[3]	Units
$I_{VA20TOTAL\_MAX}$	Input Current per port	Training (maximum)	TBD	TBD	TBD	mA
$I_{VA10TOTAL\_MAX}$	Input Current per port	Training (maximum)	TBD	TBD	TBD	mA
$I_{VDDTOTAL\_MAX}$	Input Current per port	Training (maximum)	TBD	TBD	TBD	mA

Table 4.8 **Training Parameters**

1. 10G Training, T_J = 108°C.
2. 5G Training, T_J = 108°C.
3. 2.5G Training, T_J = 108°C.

4.8 Support for Low-Power Modes

Table 4.9 lists and describes several example low-power modes that are supported by the device family.

Mode	Power/Units	Description
100Mbps WoL	300mW	Link is up in 100Mbps mode. In this mode, the system-side SerDes is off and the WoL logic in the PHY is active to both receive and match wake packets.
Energy Detect	150mW	No link and system-side SerDes is off. In this energy detect mode, the PHY is in a state where it detects incoming signals from link partners. In this mode, the PHY wakes up the MAC and enables system-side SerDes if the presence of a link partner is detected.
Disable	75mW	No functionality expected in PHY. In this mode, either a Disable or Reset pin on the PHY should put it into the lowest power mode possible.

Table 4.9 **Low-Power Mode Support**

4.9 Management Interface

The management interface includes the following signals:

1) MDC

2) MDIO

3) RST_N

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{IL}	Input low voltage				0.54	V
V_{IH}	Input high voltage		1.26			V
V_{OL}	Output low voltage	I_{OL} = -4mA	0.0		0.2	V
V_{OH}	Output high voltage	I_{OH} = 0mA				V
		I_{OH} = 10mA				V
I_{OL}	Output low current	V_{OL} = 0.2V				mA
I_{OH}[1]	Output high current	V_{OH} = 1.0V				mA
I_{LKG}	Tristate Leakage	V_{IN} = 0V or V_{CC}	-10		10	µA
C_i	Input capacitance				10	pF
C_L	Maximum capacitive load				470	pF

Table 4.10 **1.8V Mode MDIO Electrical Interface Characteristics**

1. I_{OH} parameter is not applicable to open drain drivers (for example, the MDIO data line).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{IL}	Input low voltage				30	%VDD_IO
V_{IH}	Input high voltage		70			%VDD_IO
V_{OL}	Output low voltage	I_{OL} = -4mA	0		20	%VDD_IO
V_{OH}	Output high voltage	I_{OH} = 0mA	80		120	%VDD_IO
		I_{OH} = 10mA	80		120	%VDD_IO
I_{OL}	Output low current	V_{OL} = 20% VDD_IO	4			mA
I_{OH}[1]	Output high current	V_{OH} = 80% VDD_IO			0	mA
I_{LKG}	Tristate Leakage	V_{IN} = 0V or V_{CC}	-10		10	µA
C_i	Input capacitance				10	pF
C_L	Maximum capacitive load				120	pF

Table 4.11 **70% / 30% VDD_IO Mode MDIO Electrical Interface Characteristics**

1. I_{OH} parameter is not applicable to open drain drivers (for example, the MDIO data line).

4.10 I/O

All of the non-management interface I/O on the device family run from VDD_IO and use the same I/O cell with the following characteristics as listed in Table 4.14.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				30	%VDD_IO
V_{IH}	Input High Voltage		70			%VDD_IO
V_{OL}	Output Low Voltage	I_{OL} = -4mA	0		20	%VDD_IO
V_{OH}	Output High Voltage	I_{OH} = 0mA	80		120	%VDD_IO
		I_{OH} = 10mA	80		120	%VDD_IO
I_{OL}	Output Low Current	V_{OL} = 20% VDD_IO	17.79	30.17	42.71	mA
I_{OH}[1]	Output High current	V_{OH} = 80% VDD_IO	16.67	26.33	39.32	mA
I_{LKG}	Tristate Leakage	V_{IN} = 0V or V_{CC}	-10		10	µA
C_I	Input Capacitance				10	pF
C_L	Maximum Capacitive Load				120	pF

Table 4.12 **I/O Pin Electrical Parameters**

1. I_{OH} parameter is not applicable to open drain drivers (for example, the MDIO data line).

Note: The SPI interface is 3.3V tolerant.

4.11 Serial FLASH

Table 4.13 lists and provides the SPI pin capacitance and Table 4.14 lists and provides the SPI DC characteristics supported by the device family.

Symbol	Parameter	Test Condition	Max	Units
C_{OUT}	Output Capacitance (SCLK, CS*, SOUT)	V_{OUT} = 0V	5	pF
C_{IN}	Input Capacitance (SIN)	V_{IN} = 0V	5	pF

Table 4.13 **SPI Pin Capacitance**

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
I_{LKG}	Tristate Leakage	V_{IN} = 0V or V_{CC}		-10		10	µA
V_{IL}	Input Low Voltage					20	%VDD_IO
V_{IH}	Input High Voltage			80			%VDD_IO
V_{OL}	Output Low Voltage		I_{OL} = 4mA			20	%VDD_IO
V_{OH}	Output High Voltage		I_{OH} = -4mA	80			%VDD_IO
I_{OL}	Output low current			4			mA
I_{OH}	Output high current					-4	mA

Table 4.14 **SPI DC Characteristics**

4.12 SerDes

Table 4.15 lists and provides SerDes transmitter characteristics values, and Table 4.16 lists and provides SerDes receiver characteristics values.

Parameter	Test Condition	Min	Typ	Max	Units
Output Voltage[1]	Peak-to-peak differential	400		1000	mV
Transmit Common Mode Voltage		200		700	mV
Differential Output Impedance	Programmable	80	100	120	Ω
Common Mode Output Impedance		20	25	30	Ω

Table 4.15 **SerDes Transmitter Characteristics**

1. Near-end programmable output range.

Parameter	Test Condition	Min	Typ	Max	Units
Input Voltage	Peak-to-peak differential	50		2000	mV
Input Common Mode Voltage	Peak-to-peak differential	650		1000	mV
Input Loss of Signal Voltage	Peak-to-peak differential	75	120	175	mV
Differential Input Impedance[1]	Programmable	80		120	Ω
Common Mode Input Impedance		20	25	27.5	Ω
Receiver Differential Return Loss	DC	-20			dB
	5GHz	-5			dB
Receiver Common-Mode Return Loss	DC	-10			dB
	5GHz	-6			dB

Table 4.16 **SerDes Receiver Characteristics**

1. This is programmable to ±10%.

4.13 Line (MDI)

Table 4.17 lists and provides MDI electrical parameters, and the device family uses a voltage-mode driver to drive the MDI, so only decoupling is required on the transformer center-tap.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{OH-DIFF}$	Differential Output Voltage				2.0	$V_{peak-peak}$
C_{IN}	Input Capacitance				2.5	pF
R_{IN}	Input Resistance		48	50	52	Ω

Table 4.17 **MDI Electrical Parameters**

4.14 Reference Clocks

4.14.1 Input Clock Pins XTAL_I and XTAL_O

Symbol	Parameter	Min	Typ	Max	Units
V_{SWING}	Single-Ended Input Voltage Swing		0.35		V
V_{COMMON}	Common-Mode Voltage Level		1.2		V
V_{IH}	Input High		1.375		V
V_{IL}	Input Low		1.025		V
C_{IN}	Input Capacitance			1	pF
$Z_{IN-DIFF}$	Input Impedance		100		Ω
$R_{IN-DIFF}$	Input Termination		100		Ω

Table 4.18 **LVDS 50MHz Input Electrical Parameters**

4.14.2 Input Clock Pins CLK_1588_P and CLK_1588_N

Symbol	Parameter	Min	Typ	Max	Units
V_{SWING}	Single-Ended Input Voltage Swing	0.30	0.35	0.40	V
V_{COMMON}	Common-Mode Voltage Level[1]		0.175		V
V_{IH}	Input High	1.35	1.45	1.1025	V
V_{IL}	Input Low	0.55	0.65	0.75	V
f_{CLK_1588}	Operating Frequency	40		100	MHz
C_{IN}	Input Capacitance			1	pF
$Z_{IN-DIFF}$	Input Impedance		100		Ω
$R_{IN-DIFF}$	Input Termination		100		Ω

Table 4.19 **CLK_1588 Input Electrical Parameters**

1. CLK_1588 support AC-coupled LVDS and LVPECL clock.

4.15 Reference Resistors

Parameter	Test Condition	Min	Typ	Max	Units
Reference Resistance	Tied to 0V		2.00		kΩ
Resistor Accuracy				1	%
Maximum Power				5	mW
Temperature Variation			50		ppm/°C

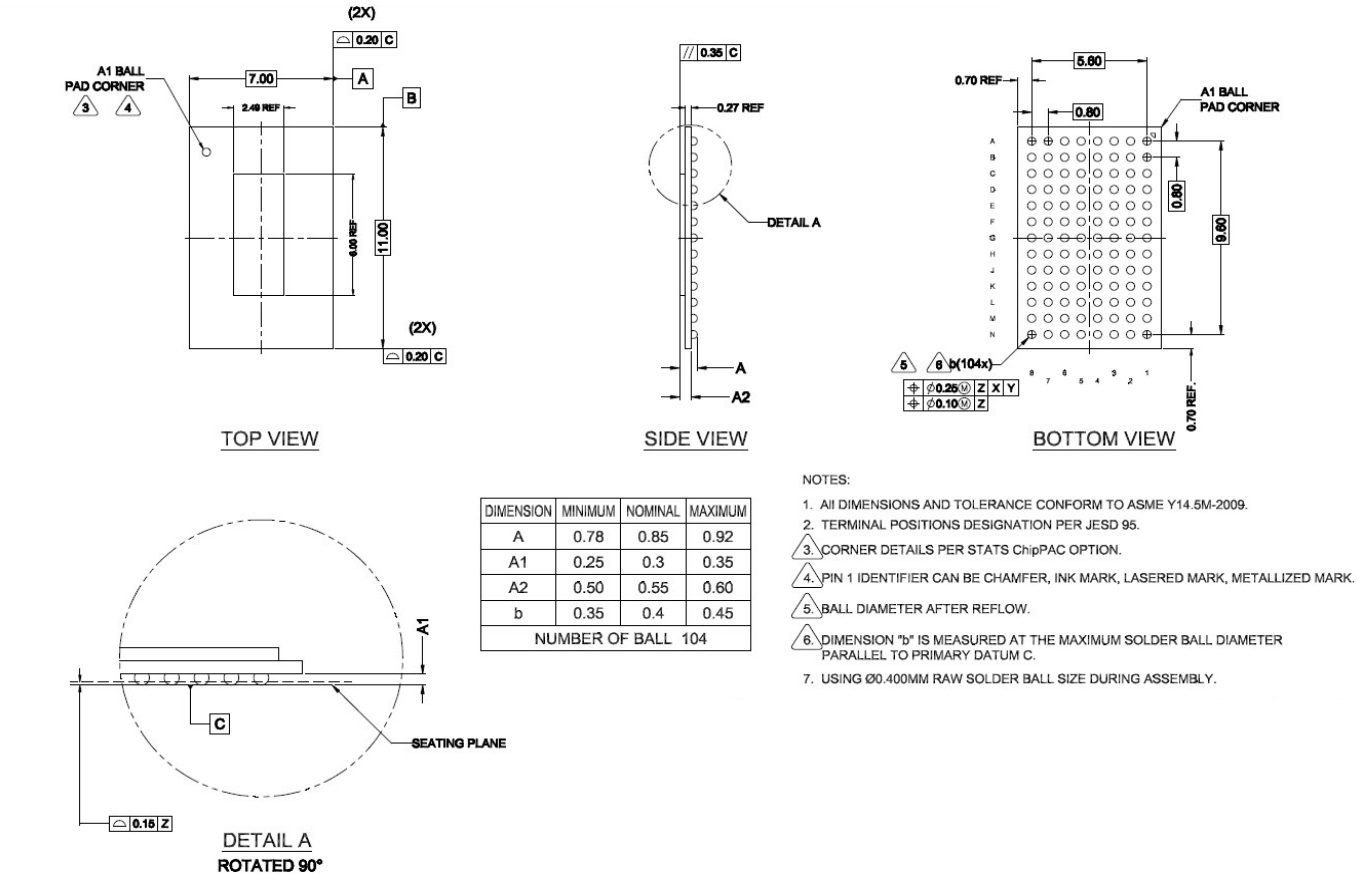
Table 4.20 **Bandgap Reference Resistor Electrical Parameters**

Package 5

5.1 Mechanical

The AQR113-AQR114-AQR115 is packaged in a 7 mm x 11 mm, 104-pin FCBGA (8 rows x 13 rows). Figure 5.1 shows this mechanical drawing package.

The AQR113C-AQR114C-AQR115C is packaged in a 7 mm x 7 mm, 64-pin FCBGA (8 rows x 8 rows). Figure 5.2 on page 96 shows this mechanical drawing package.

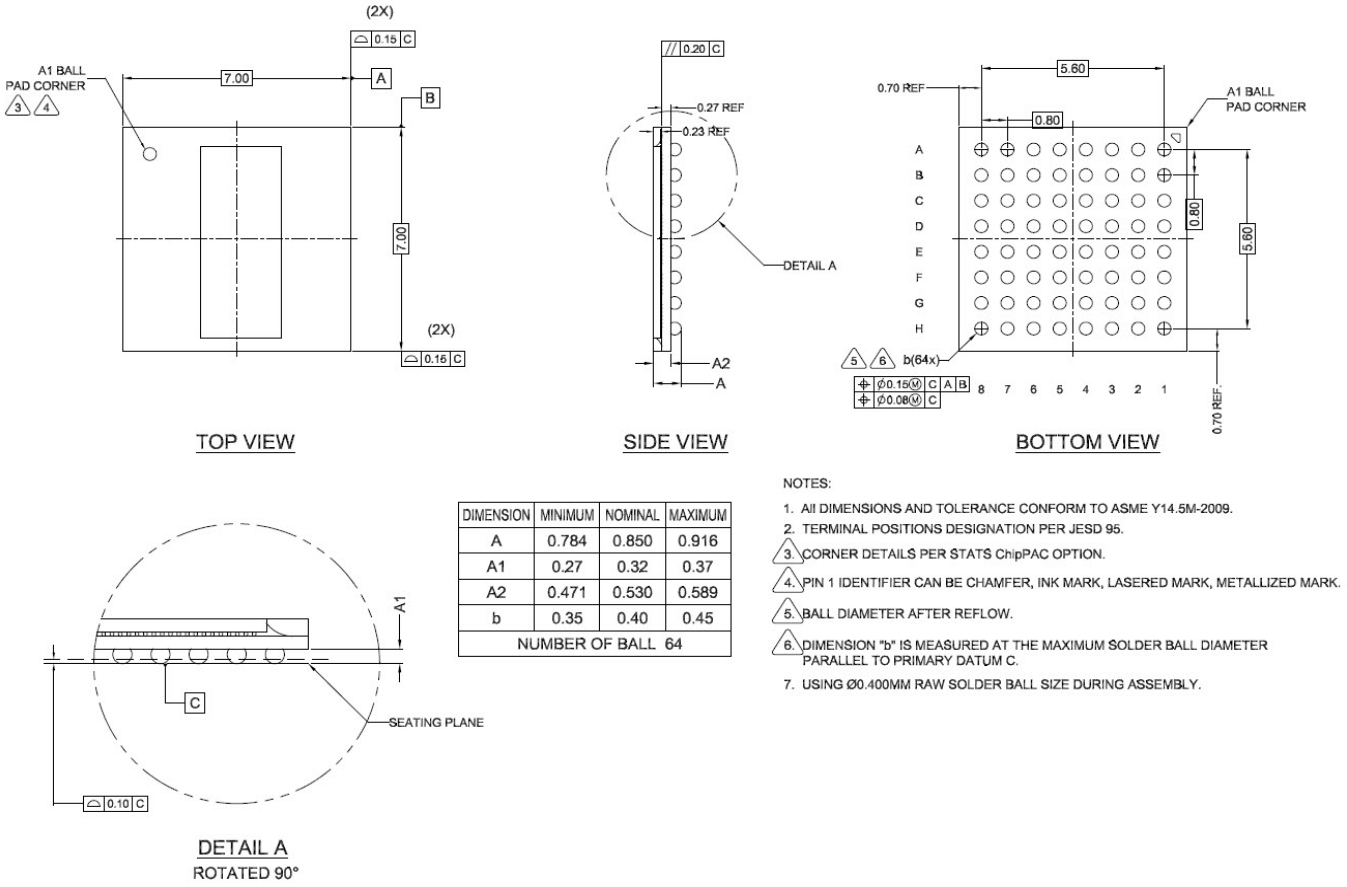


DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.78	0.85	0.92
A1	0.25	0.3	0.35
A2	0.50	0.55	0.60
b	0.35	0.4	0.45
NUMBER OF BALL 104			

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
3. CORNER DETAILS PER STATS ChipPAC OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, LASERED MARK, METALLIZED MARK.
5. BALL DIAMETER AFTER REFLOW.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
7. USING Ø0.400MM RAW SOLDER BALL SIZE DURING ASSEMBLY.

Figure 5.1 **AQR113-AQR114-AQR115 Mechanical Drawing**



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.784	0.850	0.916
A1	0.27	0.32	0.37
A2	0.471	0.530	0.589
b	0.35	0.40	0.45
NUMBER OF BALL 64			

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
3. CORNER DETAILS PER STATS ChipPAC OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, LASERED MARK, METALLIZED MARK.
5. BALL DIAMETER AFTER REFLOW.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
7. USING Ø0.400MM RAW SOLDER BALL SIZE DURING ASSEMBLY.

Figure 5.2 **AQR113C-AQR114C-AQR1115C Mechanical Drawing**

5.2 Thermal

5.2.1 Theta Js

The values of the various θ_Js for the device family are listed in Table 5.1:

Name	Thermal Coefficient	Test Condition	Value	Units
7 mm x 7 mm Package				
Theta Junction to Ambient	θ_{JA}	Still air at 55°C	23.51	°C/W
Theta Junction to Board	θ_{JB}		7.66	°C/W
Theta Junction to Case	θ_{JC}		0.11	°C/W
7 mm x 11 mm Package				
Theta Junction to Ambient	θ_{JA}	Still air at 55°C	21.22	°C/W
Theta Junction to Board	θ_{JB}		6.74	°C/W
Theta Junction to Case	θ_{JC}		0.10	°C/W

Table 5.1 **Theta Js**

Note: The thermal values listed in Table 5.1 are based on using the Flotherm® simulation model with Packet Details Markup Language (PDML) that generated a set of thermal parameters.

Aquantia recommends that customers use their own system thermal parameters, re-generate new thermal numbers using the available .pdml file, and use these newly generated numbers to design the thermal elements suitable for their own system and its requirements.

5.2.2 Thermal Model

For the device family, Aquantia supplies a Flotherm® model with Packet Details Markup Language (PDML).

5.3 Standard Reflow Profile for Lead-Free Packages

The information in this section of this datasheet is for reference purposes only. Aquantia advises customers to optimize their own board-level parameters to best ensure acceptable levels of quality, reliability, and manufacturing yield.

Table 5.2 on page 98 and Figure 5.3 on page 99 provide some guidelines for Pb-free reflow profile.

Note: The Pb-free reflow profile guidelines are based on IPC JEDEC J-STD-020.

Profile Feature	Pb-Free Assembly
Preheat/Soak	
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_s) from (T_{smin}) to (T_{smax})	60-120 seconds
Ramp-Up Rate (T_L to T_P)	3°C/second maximum
Liquidous Temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak Package Body Temperature (T_p)	260°C **Note:** Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
Time (t_p)* within 5°C of the specified classification temperature (T_c), see Figure 5.3.	30* seconds
Ramp-Down Rate (T_p to T_L)	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum
Moisture Sensitivity Level (MSL)	Level 3

Table 5.2 **Pb-Free Reflow Profile Guidelines**

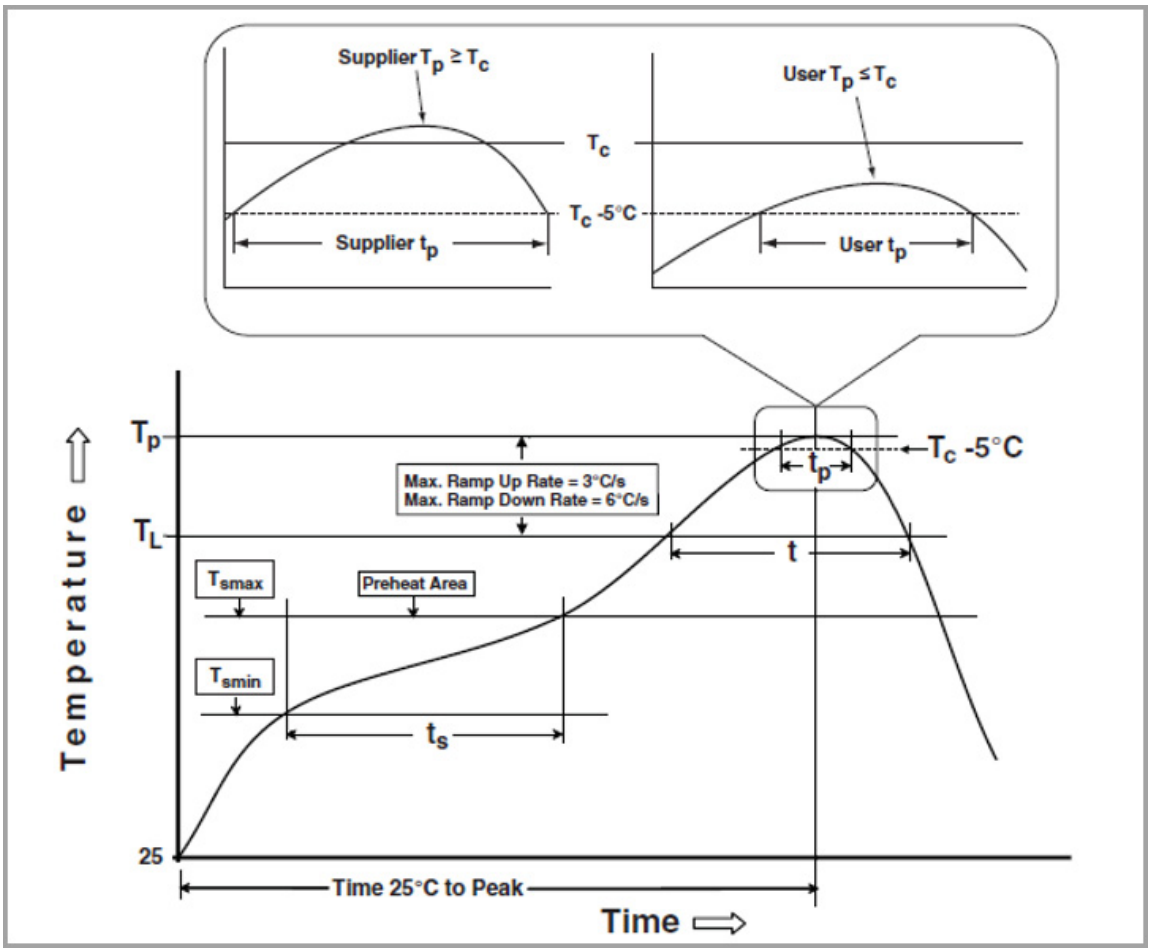


Figure 5.3 **Reflow Profile**

Register Map 6

6.1 Introduction

The device family is internally divided into a series of MDIO Manageable Devices (MMDs), each of which performs a logical function as per the 10GBASE-T standard (Figure 6.1 shows a block diagram of this partitioning).

Here the MMD #1 contains the PMA, which is basically the analog front-end of the chip. This is connected to MMD #3, which contains the PCS, which handles the 10GBASE-T transmission frame coding and decoding, including the 128-DSQ and Low-Density Parity-Check (LDPC) work.

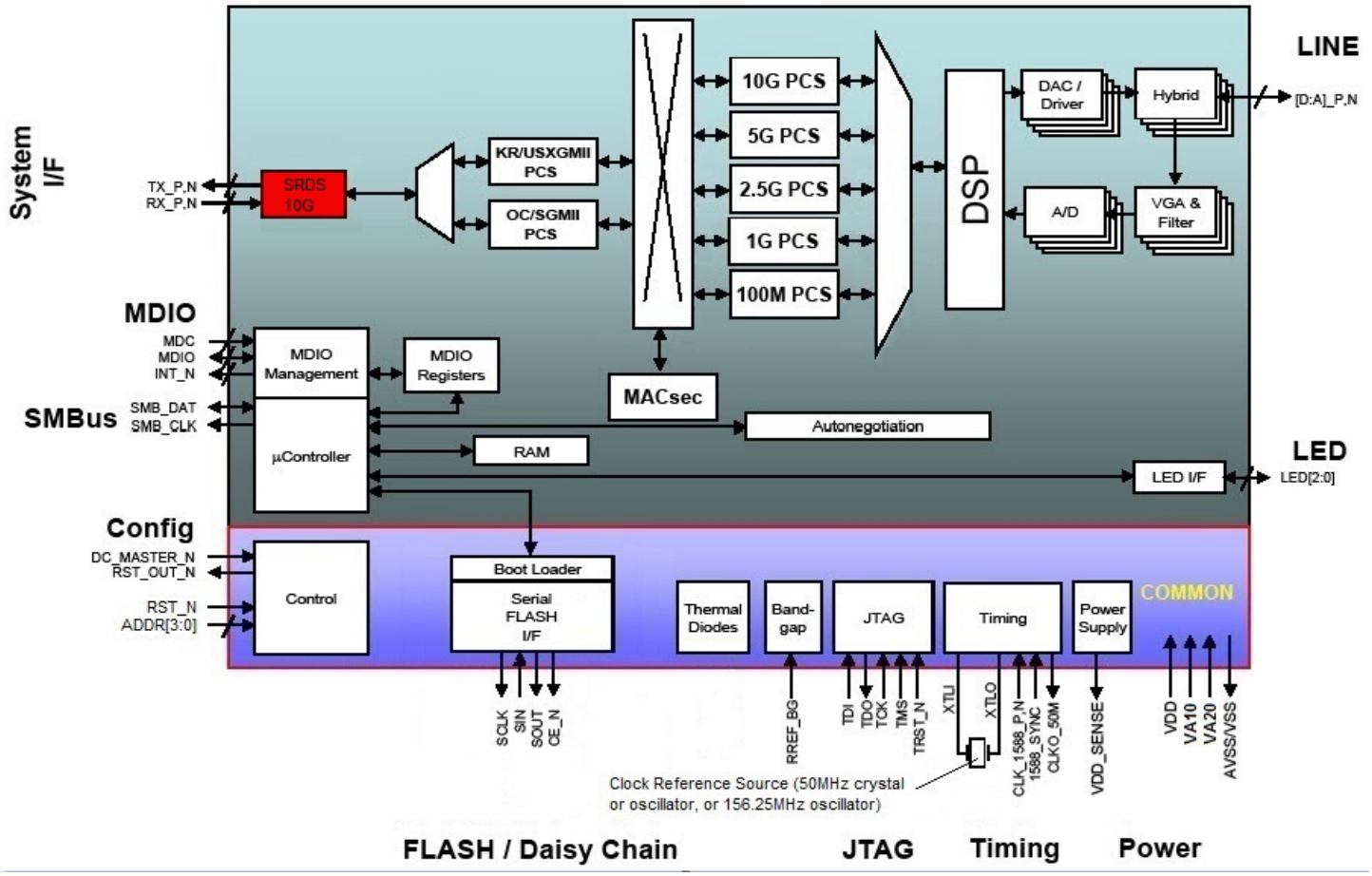


Figure 6.1 **MDIO Manageable Devices Block Diagram**

This block is in turn connected to MMD #4, which contains the SerDes PCS. In addition to these MMDs, there are three others of note:

1) MMD #7, which contains the autonegotiation function.

2) MMD #29, which contains the controls for the GbE and 100M PCS machinery.

3) MMD# 30, which contains the global control functionality for the device family.

Note: While not shown, but also present within the device family, is MMD #31, which is used for proprietary purposes as an adjunct to the PMA.

6.2 Register Structure

Table 6.1 shows a map of these regions. Any attempt to read from the reserved MMD addresses will return a value of 0x00, and any writes to these addresses will have no effect.

5-Bit Device Address (Hex)	MMD Name
0	reserved
1	PMA/PMD (128 DSQ)
2	reserved
3	PCS (64/65B coder/decoder)
4	PHY XS
5 →6	reserved
7	Auto-negotiation
8 →1C	reserved
1D	Clause 22 Extension
1E	Global
1F	Aquantia Proprietary

Table 6.1 **MMD Device Addresses**

6.3 Format and Nomenclature

Registers within the device are referenced in the following format:

Region.Register.Bit

1) ***Region*** corresponds to the MMD region that is being addressed
2) ***Register*** corresponds to the register within that MMD region
3) ***Bit*** corresponds to the bit within the specific register

Note: All registers within the MDIO register space are 16 bits. The address of the register is the 16-bit MDIO address.

All read and write operation are *word based*, which means that the entire 16-bit register is read or written (versus individual bits being read or written). Within the MDIO register space, there are several different bit types. A list of these bit types is found in Table 6.2.

Abbreviation	Type	Description
LL	Latching Low	If the condition the bit is monitoring goes low, this bit latches low, generates a maskable interrupt, and stays low until read. Reading this bit resets it to one. This bit is read-only.
LH	Latching High	If the condition the bit is monitoring goes high, this bit latches high, generates a maskable interrupt, and stays high until read. Reading this bit resets it to zero. This bit is read-only.
LRF	Latch Rising or Falling	Set high on either a rising or falling edge. If a transition occurs, this bit latches high, generates a maskable interrupt, and stays high until read. Reading this bit resets it to zero. This bit is read-only.
PD	Provisionable Defaults	Indicates that the default value associated with this field is provisionable.
RO	Read Only	Read-only field. Writes are ignored.
ROS	Read Only Static	Read-only and static field. The value does not change.
R/W	Read/Write	Field can be both read from and written to.
SC	Self-Clearing	A read/write register which resets itself upon completion of an action.

Table 6.2 **MDIO Register Space Bit Field Types**

Abbreviation	Type	Description
SCT	Saturating Counter	A read-only counter that saturates at the limit, and is cleared on read.
SCTL	Saturating Counter LSW	The Least Significant Word of a Saturating Counter. This register clears the pair to zero on read and snapshots the mate MSW to shadow memory, awaiting read.
SCTM	Saturating Counter MSW	The Most Significant Word of a Saturating Counter. Reading this completes the read process of the register pair.

Table 6.2 **MDIO Register Space Bit Field Types** (continued)

6.4 Structure

The following structure is used for registers:

1) All Clause 45 registers (the registers that are defined in Clause 45) are placed in their respective areas within the MMDs as specified.

2) X2 registers are placed in MMD #1.

3) Aquantia-specific registers that are associated with each of the Clause 45 MMDs are placed in the Aquantia specific area beginning at 0xC000, according to the register map shown in Table 6.3.

Base Offset (Hex)	Description
C000	TX and Overall MMD Control
C400	TX and Overall MMD Provisioning
C800	TX and Overall MMD State
CC00	TX and Overall MMD Alarms
D000	Standard Interrupt Mask
D400	TX and Overall MMD Interrupt Mask
D800	TX and Overall MMD Debug
DC00	Reserved
E000	RX Control
E400	RX Provisioning
E800	RX State

Table 6.3 **Register Layout**

Base Offset (Hex)	Description
EC00	RX Alarms
F000	Standard Interrupt Mask
F400	RX Interrupt Mask
F800	RX Debug
FC00	Global Interrupt Flags

Table 6.3 **Register Layout** (continued)

The table is split into a transmit and a receive portion, with the transmit portion also containing any overall Aquantia specific registers for the MMD. Table 6.4 lists the following definitions that apply to the terms within the register layout.

Term	Definition
Control	Action bits that affect the operation of the MMD, such as reset.
Provisioning	Static provisioning bits that control the behavior of the MMD.
State	Bits that reflect the state of the MMD.
Alarm	Bits that can generate maskable interrupts.
Standard Interrupt Mask	Interrupt masks for alarm bits defined in the Clause 45 register set.
Aquantia Specific Interrupt Mask	Interrupt masks for Aquantia Specific alarms.

Table 6.4 **Terms Used within the Register Layout**

4) Interrupts are handled in an hierarchical fashion, with the top level interrupt indication being the INT* interrupt pin that is on the device.

Below this are two maskable interrupt trees; one tree is composed of standard interrupts, and the other tree is composed of Aquantia-defined interrupts. The top level summary register for these trees resides at the end of the register space in MMD #30 - the Aquantia Global MMD (1E.FC00). Feeding this are interrupt registers from each of the individual MMDs.

a) The standard interrupt tree is designed so that the source of any interrupt can be determined in a maximum of two reads.

b) The Aquantia-defined interrupt tree requires at most three reads to determine the source of an interrupt.

c) All interrupts are maskable, whether they are from the Standard interrupt tree, or from the Aquantia-defined interrupt tree.

Note: The device family supports IEEE 802.3 Clause 45-compliant MDIO, and it also supports minimal Clause 22 MDIO interface for use with legacy 1G switches operating at 1G and 2.5G rates. For 1G applications, operating at that rate over two-pair, Clause 22 is preferred.

6.5 Register Tables Documentation

The register tables that support the single-port, quad-port, and octal-port devices are described in a separate Aquantia register table document that covers all of the following Aquantia Gen 4 multi-gigabit Ethernet PHY transceiver datasheets:

- AQR113C-AQR114C-AQR115C (single-port PHY device)
- AQR413C-AQR414C-AQR415C (quad-port PHY device)
- AQR813-AQR814-AQR815 (octal-port PHY device)

Note: To access the *Aquantia Gen 4 Multi-Gigabit Ethernet PHY Transceiver Register Specification*, log in to the Aquantia Portal using valid credentials:

https://portal.aquantia.com/user

The registers described in the register tables document are listed by the numerical order of their MMD address. Associated with these registers is a set of C-language header files and the associated Doxygen documentation for them. The header files contain all of the appropriate C-structures that allow access to the registers and fields within the following sets of register tables:

- PMA registers
- PCS registers
- PHY XS registers
- Autonegotiation registers
- 100BASE-TX and 1000BASE-T registers
- Global registers
- SEC Ingress and Egress registers

Note: For specific details about the registers that support the Gen 4 Ethernet PHY devices, see the *Aquantia Gen 4 Multi-Gigabit Ethernet PHY Transceiver Register Specification*.

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