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RTL9311R-CG

LAYER 3 STACKABLE 24*10/100/1000M + 4*10G PORT SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL9311R chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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1. General Description

The RTL9311R-CG is a layer 3 Stackable Gigabit Ethernet switch device with 64Gbps forwarding bandwidth. The RTL9311R-CG is a cost-effective solution for Small-Medium Business (SMB) and Carrier Ethernet Access/Edge applications with wire-speed performance for 24GE+4*10GE platforms.

The device integrates a Dual-Core 1GHz MIPS InterAptive CPU subsystem. It supports a 32-bit data bus, 32M-Byte SPI flash (3-byte mode) or, 64MB SPI flash (4-byte mode), and 2G-Byte DDR3/DDR4 SDRAMs (maximum). An embedded 64KB SRAM can be used for time-sensitive applications. For external CPU connection, PCIe Gen2 is supported.

The device has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-and-port-based, MAC-based, and Flow-based capability. It also supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (both Independent and Shared VLAN Learning) for flexible network topology architecture. In network access applications it provides IEEE802.1ad (Q-in-Q) for double tag insertion and removal function. In additions, VLAN translation function is also supported for Metro Ethernet applications.

32K entries L2 MAC table are supported with 2-left 4-way hashing algorithm which can effectively reduce collision ratio. An independent 4K-entry Multicast table is used to support Multicast functions, such as IGMP snooping.

The device supports a 4K-entry VLAN/Ingress/Egress Access Control List (ACL). The ACL function supports L2/L3/L4 match fields and performs configurable actions, such as Drop/Permit/Redirect/Mirror/Logging/Policing/Ingress VLAN conversion/Egress VLAN conversion/QoS remarking/VLAN tag status assignment.

Per-port ingress/egress bandwidth control and per-queue egress bandwidth control are supported. The device provides three types of packet scheduling, including SP (Strict Priority), WFQ (Weighted Fair Queuing), and WRR (Weighted Round Robin). Each port has 8 physical queues and each queue provides a leaky-bucket to shape the incoming traffic into the average rate behavior. The Broadcast/Multicast/Unknown-Multicast/Unknown-Unicast storm suppression function can inhibit external and internal malicious attacks.

The device supports 4-sets of port mirror configurations to mirror ingress and egress traffic. RSPAN, sFlow are also supported for traffic monitoring purposes. For network management purposes, complete MIB counters are supported to provide forwarding statistics in real time. The Link aggregation function enhances link redundancy and increases bandwidth linearly.

In addition to traditional pipeline, the device embeds an OpenFlow pipeline which comprises four Ingress Flow Tables and One Egress Flow Table. OpenFlow-hybrid switch or OpenFlow-only switch can be supported

2. Features

- Hardware Interface
  - 128Gbps switch capacity
  - Supports 3 pairs of 10Gbps XSGMII to 24 ports 10/100/1000M Ethernet PHY and 4 pairs of 10GBase-R
  - Embedded CPU: MIPS InterAptiv, dual-core, up to 1GHz
    - ICache: 32KB
    - DCache: 32KB
    - L2Cache: 256KB
    - SRAM: On-Chip, 64KB
    - ROM: On-Chip, 16KB
  - DRAM
    - DDR3/DDR4, up to total 2GB address space
    - 16/32-bit, up to 800MHz
    - 2 * 16-bit Chip supported, combined as 32-bit
  - SPI-NOR Flash
    - up to total 64MB address space
    - up to 100MHz
  - SPI-NAND Flash
    - up to total 512MB address space
    - up to 100MHz
    - 2 * Chip Select supported
  - 2 * UART supported
  - USB Host 2.0 supported
  - 32 * GPIO pins with interrupt function
    - SPI master combo with GPIO pins
    - EEPROM SMI master combo with GPIO pins
  - External CPU interface
    - Supports PCIe Gen2 interface as external CPU connection
- VLAN
  - 1Q and QinQ VLAN
    - 4K VLANs
    - IVL, SVL, IVL/SVL mixed mode
    - Flexible QinQ which supports forwarding base on inner or outer tag
  - Protocol VLAN
    - Global 8 protocol VLAN configurations. Per port can specify the mapping VLAN
  - Mac-based VLAN
    - share with 2K Ingress VLAN Translation table
  - IP-Subnet-based VLAN
    - share with 2K Ingress VLAN Translation table
  - VLAN Translation
    - 2K Ingress and 1K Egress
  - N:1 VLAN Translation
    - Via MAC Address Table
  - VLAN Profile
    - 16 VLAN profiles which define L2 learning enable/disable and unknown L2/IPv4/IPv6 multicast flooding domain
  - VLAN Filtering
    - Per ingress port and egress port enable VLAN filtering
- MAC and Port Capability
  - MAC Address Table Size
    - 32K (2*16K 4-way hash)
  - 4K Multicast Table Size
  - L2 Entry Notification
    - Offload SW effort for maintaining a synchronous L2 table with HW
  - 16Mbit Packet Buffer
  - Jumbo frame up to 12KB
- Mirror/Sampling
  - Port Mirroring

- 4 mirror sets
- Each mirror set can specify one mirroring port and multiple mirrored ports
- Mirror Isolation
- Flow-based mirror by ACL

- RSPAN
  - Source, Intermediate, Destination Switch
- sFlow
  - Ingress Port, Egress Port

- Trunk (IEEE802.3ad LACP)
  - 128 Groups
  - Distribution Algorithm for Load Balance
    - SPN/SMAC/DMAC/SIP/DIP/SPORT /DPORT
  - Ports for Each Group
    - Up to 8 ports
  - Trunk Fail Over
    - Hardware auto fail-over for link down ports

- Multicast
  - IGMP/MLD ASM snooping
    - ASM and SSM
  - L2 Multicast
    - Up to 32K Groups with 4K different Port Mask
  - IP Multicast Replication
    - Up to 16K replications (VLAN*Multicast groups)

- Bridge
  - Spanning tree algorithm
    - STP/RSTP/MSTP
  - 128 Multiple Spanning Tree Instance

- QoS
  - Amount of Queues
    - Normal port 8 egress queues
    - CPU port 32 queues
  - Storm Control
    - Per port specify BPS/PPS and rate
    - Unknown unicast
    - Unknown+Known unicast
    - Unknown multicast
    - Unknown+Known multicast
    - Broadcast
  - Control Protocol Strom Control
    - Per ingress port specify BPDU/ARP/IGMP suppression rate for against protocol attack
  - Ingress Bandwidth Control
    - Per port specify rate 0~10G, unit is 16Kbps
    - Input queue shaping
  - Egress Bandwidth Control
    - Per port specify rate 0~10G, unit is 16Kbps. CPU port can specify BPS or PPS mode
  - Scheduling Method
    - Per queue supports Assured or Fixed BW
    - Scheduling algorithm: WRR, WFQ, Strict, Strict+WRR, Strict+WFQ
  - Simple WRED
  - Remarking
    - Per egress port enable remarking
    - Inner VLAN
    - Outer VLAN
    - DSCP
    - DEI

- ACL
  - Number of Entries
    - 4K (share with OpenFlow)
  - 240-bits Entry Width
  - Template Number
    - total 10 template(5 pre-defined, 5 user defined)
  - ACL Phase

- VLAN/Ingress/Egress ACL and each phase's size is adjustable

- Meter/Marking
  - 512 policer which can be configured as DLB or srTCM or trTCM
  - Hierarchical policing
  - CAR supportive
- Counter
  - 4K packet counter and byte counter
  - Multiple counter execution
- Key
  - L2 ~L4 headers
  - User Defined Fields

- Security
  - IP+MAC+PORT+VLAN Binding
    - 1K flexible binding entry
  - MAC Learning Constraint
    - System/Port/VLAN-based
  - L2~L4 DoS prevention
  - MAC White List
    - Combine with L2 table
  - MAC Black Hole
    - Source and Destination MAC
  - Port Movement
    - Per port specify dynamic and static port movement action

- Layer 3
  - IP Routing
    - IPv4/IPv6 unicast and multicast routing
    - 12K network route and 12K host route
    - Longest prefix match (LPM) based routing
  - Policy-Based Routing by ACL
  - ECMP/WCMP
    - Distribution by source/destination IP address, DSCP, TCP/UDP port
    - Dynamic Load Balancing
  - Tunneling
    - L3 GRE
    - 6 to 4
    - ISATAP
    - IP-in-IP
    - Configured Tunnel

- Management/Carrier Ethernet
  - H/W OAM Loopback
    - Per port specify Multiplexer and Parser state
  - H/W OAM Dying Gasp
    - Software-Defined Payload
  - 802.1ag CFM for ERPS
    - Link fault detection for G.8031/8032 Support
    - 8 instances which can have different CCM payload
    - HW transmits CCM packet from 1~1024ms
    - Trigger interrupt when link fault is detected
  - Y.1731 CFM
    - One-Way/Two-Way ETH-DM
  - IEEE 1588 v1/v2
    - Support by PHY
  - Synchronous Ethernet supported by PHY

- SDN (Software Defined Network)
  - OpenFlow
    - OpenFlow v1.5.1 Compliant
    - OpenFlow hybrid switch
    - 32K flow entries(4K Full Match+16K L2+12K L3)
    - Five Flow Tables (3 Full Match+L2 Optimized+L3 Optimized)
    - 4 Ingress Flow Tables + 1 Egress Flow Table
    - Extensible Flow Tables
    - Group table supported
    - Meter table supported

- Virtual Network Function

- 802.1BR(Bridge Port Extension)
  - Control Bridge (8K Multicast Replication Number)
  - 32K ECID Channel for Port Extender Bridge
  - 256 Name Space Group for Port Extender Bridge
  - ECID Extension
  - ETAG-based QoS
  - Fast link fault detection by CCM (1~1024ms)
- Remote Device Access
  - Remote Register/Table/PHY access
  - Remote Interrupt
- Stacking Supported Feature
  - 128 Trunk across devices
  - 4 Mirror across devices

■ Stacking Capability

- Maximum 16 Stackable Device
- Stacking Topology
  - Line and Ring
- Stacking Port
  - Max. 16 stacking ports
  - 4 extra Q for CPU Communication and HW communication

■ Others

- 28nm CMOS process
- 3.3V/0.9V power input
- 1.5V for DDR3
- 1.2V for DDR4
- HFC FBGA 673 package

3. Block Diagram

*3.1. RTL9311R (24G+4*10G) Block Diagram*

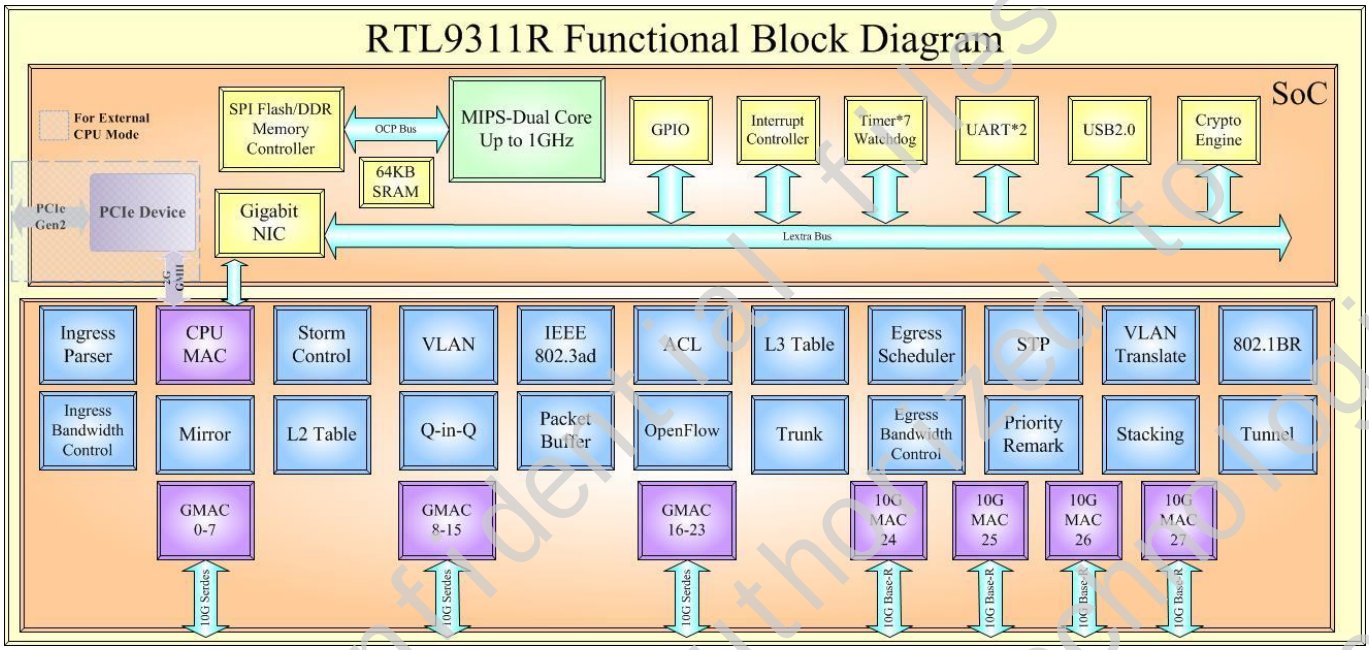


Figure 1. 9311R (24G + 4*10G) Block Diagram

4. System Applications

4.1. 24 10/100/1000Base-T + 4 SFP+

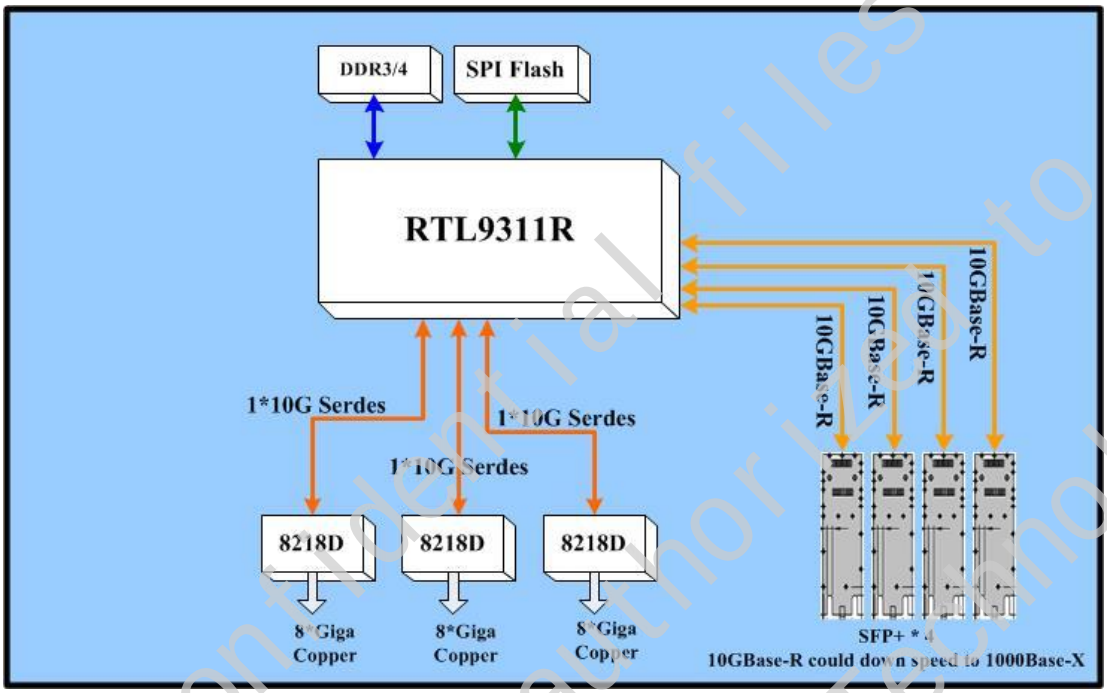


Figure 2. 24 10/100/1000Base-T + 4 SFP+

5. Pin Assignments

*5.1. RTL9311R (24G+4*10G) Pin Layout*

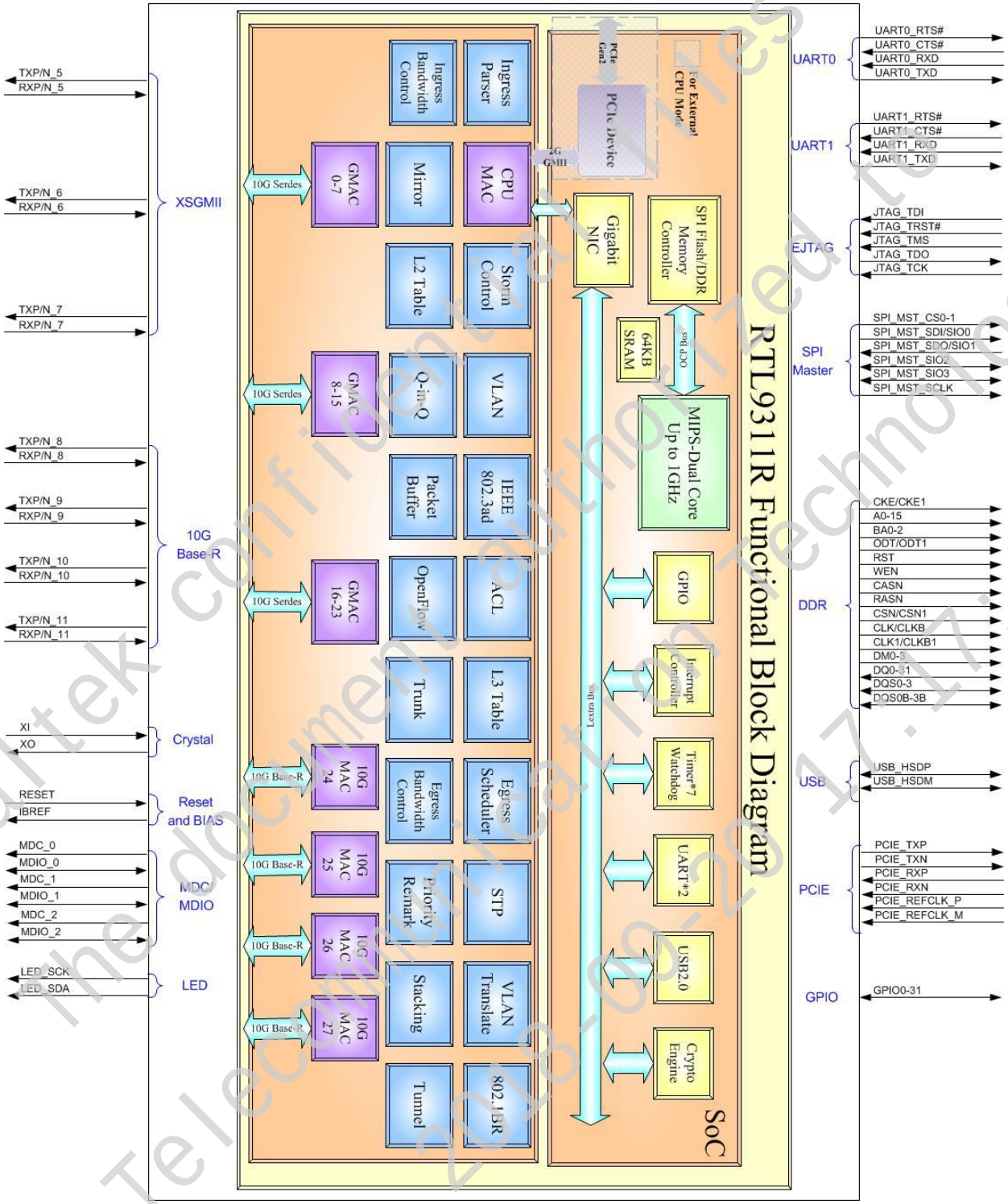


Figure 3. RTL9311R (24G+4*10G) Pin Layout

5.2. RTL9311R (24G+4*10G) Pin Assignments (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	RSVD	RSVD	RSVD	RSVD		RSVD	RSVD			RSVD	RSVD	SGND	RSVD	RSVD	RSVD	RSVD
B	RSVD	RSVD	SGND	SGND	RSVD	RSVD	SGND		RSVD	RSVD	RSVD	SGND	RSVD	RSVD	RSVD	RSVD
C		RSVD	RSVD	SVDDT RX4	SVDDT RX4	SGND	SGND	RSVD	RSVD	SGND	SGND	SGND	SGND	SGND	SGND	SGND
D			RSVD	SVDDT RX4	SVDDT RX4	SVDDT RX3	SVDDT RX3	SVDD H_2	SVDD_ CMU2	SVDDC K2	SVDDT RX2	SVDDT RX2	SVDDT RX1	SVDD_ CMU0	SVDDT RX0	SVDD H_0
E	TXP_5	SGND	SGND	SGND	SVDDC K4	SVDDT RX3	SVDDT RX3		SVDD_ RGCM U2		SVDDT RX2	SVDDT RX2	SVDDT RX1		SVDDT RX0	
F	TXN_5	RSVD	SGND	SGND	SVDD_ CMU4		SVDD H_4									
G		RSVD	RXP_5	SGND	SVDD_ RGCM U4											
H			RXN_5	SVDDT RX5	SVDDT RX5											SVDD H_CKO
J	TXP_6	RSVD	SGND	SVDDT RX5	SVDDT RX5										SVDD H_CKO	SVDD H_CKO
K	TXN_6	RSVD	SGND	SVDDT RX6	SVDDT RX6										SVDD H_CKO	SGND
L		RSVD	RXP_6	SVDDT RX6	SVDDT RX6										SGND	SGND
M			RXN_6	SGND	SVDD_ CMU6										SGND	SGND
N	TXP_7	SGND	SGND	SGND	SVDD_ RGCM U6	SVDD H_6									SGND	SGND
P	TXN_7	RSVD	SGND	SGND	SVDDC K6										SGND	SGND
R		RSVD	RXP_7	SVDDT RX7	SVDDT RX7											
T			RXN_7	SVDDT RX7	SVDDT RX7							DGND	DGND	DGND	DGND	DGND
U	PWRM ON	RSVD	RSVD	AGND_ XTAL	SVDDT RX8	SVDDT RX8						DGND	DGND	DGND	DGND	DVDD L
V	XO	RSVD	RSVD	AVDD H_XTA L	SVDDT RX8	SVDDT RX8						DGND	DGND	DGND	DGND	DVDD L
W	XI	RSVD	IBRFE	AVDD L_XTA L	SVDDC K8										SGND	DGND
Y		RSVD	RSVD	AVDD _BG	SVDD_ CMU8	SVDD H_8									SGND	DGND
AA	RESET B	RSVD	SGND	AVDD H_BG	SVDD_ RGCM U8										SGND	SGND
AB	TXP_8	RSVD	SGND	AGND_ BG	SVDDT RX9	SVDDT RX9									SGND	SGND
AC	TXN_8	RSVD	SGND	AGND_ BG	SVDDT RX9	SVDDT RX9									SGND	SGND
AD		RSVD	RXP_8	SVDDT RX10	SVDDT RX10	SVDDC K10									SGND	SGND
AE			RXN_8	SVDDT RX10	SVDDT RX10										SVDD H_CKO	SVDD H_CKO
AF	TXP_9	SGND	SGND	SGND	SVDD_ RGCM U10	SVDD H_10		SVDD H_12								SVDD H_CKO
AG	TXN_9	RSVD	SGND	SGND	SGND	SVDD_ CMU10	SGND	SVDDC K12		SVDD_ CMU12	DDR_I ATA_B US	RSVD	RSVD	RSVD	BOOT_ SEL	DDR_T YPE_S EL_1
AH		RSVD	SVDDT RX11	SVDDT RX11	SVDDT RX12	SVDDT RX12	SGND	SVDD_ RGCM U12	SVDDT RX13	SVDDT RX13	IFU_PA TCH_E N	RSVD	RSVD	RSVD	I2C_D ATA_E NDIAN _SEL	DDR_T YPE_S EL_0
AJ	RXP_9	SGND	SVDDT RX11	SVDDT RX11	SVDDT RX12	SVDDT RX12	SGND	SGND	SVDDT RX13	SVDDT RX13	RSVD		RSVD		RSVD	
AK	RXN_9	SGND	RXP_1 0	RXN_1 0	SGND	SGND	RXP_1 1	RXN_1 1	SGND	SGND	RSVD	RSVD	SGND	SGND	RSVD	RSVD
AL	RSVD	RSVD	RSVD		SGND	RSVD	RSVD		RSVD	RSVD	RSVD		SGND	RSVD	RSVD	
AM	TXP_10	TXN_1 0			TXP_11	TXN_1 1			RSVD	RSVD			RSVD	RSVD		

Figure 4. RTL9311R (24G+4*10G) Pin Assignments (Top View)

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
RSVD	RSVD	MDC_1	MDC_0	SPI_SDO/SIO1	SPI_SIO2	SPI_SCLK	SPI_CS#[0]	RSVD	RSVD	REG_IF_SEL	RSVD	RSVD	HW_RESET_EN	USB_LED	USB_HSDP	A
SGND	RSVD	MDIO_1	MDIO_0	SPI_SDI/SIO0	SPI_SIO3	SPI_RSTN	SPI_CS#[1]	RST_OUT	RSVD	SYS_LED_EN	RSVD	RSVD	USB_VDDH	USB_GND	USB_HSDM	B
SGND	RSVD	DVDDH_2	DVDDH_1	DVDDH_12				PERSTB	RSVD	EXT_CPU_EN	RST_CMD_DIS	RSVD	USB_VDDH	USB_GND	USB_GND	C
RSVD	RSVD								AGND_PLL	AVDDH_PLL	AVDDL_PLL	USB_VDDL	USB_VDDL	PCIE_RXN	PCIE_RXP	D
	DVDDH	DVDDH	DVDDH	DVDDL	DVDDL	DGND	DGND		AGND_PLL	AVDDH_PLL	AVDDL_PLL	USB_VDDL	USB_VDDL	PCIE_GND	PCIE_GND	E
	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DGND						PCIE_VDDL	PCIE_GND	PCIE_REFCLK_P	F
	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DGND						PCIE_VDDL	PCIE_GND	PCIE_REFCLK_M	G
DGND	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DGND						PCIE_VDDL	PCIE_GND	PCIE_GND	H
DGND	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DGND						PCIE_VDDL	PCIE_TXP	PCIE_TXN	J
DGND	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DVDDL_CPU					RSVD	CKE_CKE	RSVD		K
DGND	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DVDDL_CPU			RSVD	A3_WE_N/A14	BA0_X	DGND	ODT_X		L
DGND	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DVDDL_CPU			DGND	X_A0	X_BG0	RST_RST	A2_BA0		M
DGND	DGND	DGND	DGND	DVDDL	DVDDL	DVDDL_CPU	DVDDL_CPU			DGND	A7_A8	A5_A6	DGND	A13_A11	A9_A2	N
DGND	DGND	DGND	DVDDL	DVDDL	DVDDL	DVDDL_CPU	DVDDL_CPU			DGND	BA2_X	A0_X	WEN_A10/AP	CASN_ACT_n		P
DGND	DGND	DGND	DVDDL	DVDDL	DVDDL	DVDDL				DGND	A11_A4	RASN_PAR	DGND	A14_A12/BC_N	A1_A3	R
DGND	DGND	DGND	DVDDL	DVDDL	DVDDL	DVDDL				DGND	A6_RAS_N/A16	A8_ODT	X_A1	BA1_A7		T
DVDDL	DVDDL	DVDDL	DVDDL	DVDDL	DVDDL	DVDDL					A4_A13	A12_A9	DGND	A15_A14	X_TEN	U
DVDDL	DVDDL	DVDDL	DVDDL	DVDDL	DVDDL	DVDDL				MVDDH	X_ALERT_1	RSVD	CLKB_CLKB	CLK_CLK		V
DGND	DGND	DGND	DVDDL	DVDDL	DVDDL	DVDDL					x_ALERT	A10_A5	RSVD	RSVD		W
DGND	DGND	DGND	DGND	MVDD	MVDD	MVDD				RSVD	CSN_CSN	X_CASN/A15	DGND	DM0_DM0_n/DBIL_n	DGND	Y
DGND	DVDDH	DVDDH	DVDDH_7	MVDD	MVDD	MVDD				RSVD	DQ10_DQ15	DQ8_DQ13	DQ1_DQ1	DQ5_DQ5		AA
DGND	DVDDH_13	DVDDH	DVDDH_6	MVDD	MVDD	MVDD				DGND	DQ12_DQ9	DQ14_DQ11	DGND	DQ3_DQ3	DQ7_DQ7	AB
	DVDDH_3	DVDDH_4	DVDDH_5	MVDD	MVDD	MVDD				DGND	DQ4_DQ4	DQS1_DQS1	DQS1B_DQS1B	DQ6_DQ2		AC
										DGND	DQ13_DQ10	DQ15_DQ8	DGND	DQ2_DQ0	DQ0_DQ0	AD
										DQ11_DQ14	DM1_DM1_n/DBIU_n	DQ9_DQ12	DQS0B_DQS0B	DQS0_DQS0		AE
										DGND	DGND	DGND	DGND	DM2_DM2_n/DBIL_n	DGND	AF
	RSVD	GPIO_17/SDA2	GPIO_20/SDA5	GPIO_26/SDA11	RSVD	RSVD	UART1_RTS#	UART1_CTS#	UART0_RTS#	DGND	DQ26_DQ31	DQ24_DQ29	DQ17_DQ17	DQ21_DQ21		AG
GPIO_27	RSVD	GPIO_16/SDA1	GPIO_19/SDA4	GPIO_25/SDA10	GPIO_12/SPI_CS#1	GPIO_5/JTAG_TRST#	RSVD	UART1_TXD	UART0_CTS#	DGND	DQ28_DQ25	DQ30_DQ27	DGND	DQ19_DQ19	DQ23_DQ23	AH
GPIO_31/LED_SYNC		GPIO_15/SDA0		GPIO_24/SDA9		GPIO_3/JTAG_TMS		UART1_RXD		DGND	DQ53_DQS3	DQS3B_DQS3B	DQ20_DQ20	DQ22_DQ18		AJ
GPIO_28	LED_SDA/LED_MDIO	GPIO_13/SCL0	GPIO_18/SDA3	GPIO_23/SDA8	GPIO_11/SPI_CS#0	GPIO_4/JTAG_TCK	GPIO_6/JTAG_TDI	GPIO_0/SYS_LED	SPI_SLV_SDO				DQ29_DQ26	DQ31_DQ24	DGND	DQ18_DQ22	DQ16_DQ16	AK
MDIO_2	LED_SCK/LED_MDIO	GPIO_30/SC_MDIO	GPIO_14/SCL1	GPIO_22/SDA7	GPIO_10/SPI_MOSI	GPIO_8/SPI_SCK	GPIO_7/JTAG_TDO	GPIO_2/GPIO_MDIO	SPI_SLV_CS#	DM3_DM3_n/DBIU_n	DQ27_DQ30	DQ25_DQ28	DQS2B_DQS2B	DQS2_DQS2		AL
MDC_2		GPIO_29/SC_MDC		GPIO_21/SDA6		GPIO_9/SPI_MISO		GPIO_1/GPIO_MDC		SPI_SLV_SDI/I2C_SDA	SPI_SLV_SCLK/I2C_SCK	UART0_RXD	UART0_TXD	RSVD		AM
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	

Figure 5. RTL9311R (24G+4*10G) Pin Assignments (Top View) (Continued)

5.3. Pin Assignments Table Definitions

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

DP: Digital Power Pin

DG: Digital Ground Pin

SP: SERDES Power Pin

MP: DDR Power Pin

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Direction Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

SG: SERDES Ground Pin

RP: Reference voltage for data for DDR SDRAM

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75KΩ)

I_{PD}: Input Pin With Pull-Down Resistor; (Typical Value = 75KΩ)

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75KΩ)

O_{PD}: Output Pin With Pull-Down Resistor; (Typical Value = 75KΩ)

5.4. RTL9311R (24G+4*10G) Pin Assignments Table

Table 1. RTL9311R (24G+4*10G) Pin Assignments Table

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type	RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
RESERVED	A1	-	RESERVED	A15	-
RESERVED	A2	-	RESERVED	A16	-
RESERVED	A3	-	RESERVED	A17	-
RESERVED	A4	-	RESERVED	A18	-
-	-	-	MDC_1	A19	O
RESERVED	A6	-	MDC_0	A20	O
RESERVED	A7	-	SPI_SDO/SIO1	A21	I/O
-	-	-	SPI_SIO2	A22	I/O
-	-	-	SPI_SCLK	A23	O
RESERVED	A10	-	SPI_CS#[0]	A24	O
RESERVED	A11	-	RESERVED	A25	-
SGND	A12	SG	RESERVED	A26	-
RESERVED	A13	-	REG_IF_SEL	A27	I
RESERVED	A14	-	RESERVED	A28	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
RESERVED	A29	-
HW_RESET_EN	A30	I
USB_LED	A31	O
USB_HSDP	A32	AI/O
RESERVED	B1	-
RESERVED	B2	-
SGND	B3	SG
SGND	B4	SG
RESERVED	B5	-
RESERVED	B6	-
SGND	B7	SG
-	-	-
RESERVED	B9	-
RESERVED	B10	-
RESERVED	B11	-
SGND	B12	SG
RESERVED	B13	-
RESERVED	B14	-
RESERVED	B15	-
RESERVED	B16	-
SGND	B17	SG
RESERVED	B18	-
MDIO_1	B19	I/O
MDIO_0	B20	I/O
SPI_SDI/SIO0	B21	I/O
SPI_SIO3	B22	I/O
SPI_RSTN	B23	O
SPI_CS#[1]	B24	O
RST_OUT	B25	O
RESERVED	B26	-
SYS_LED_EN	B27	I
RESERVED	B28	-
RESERVED	B29	-
USB_VDDH	B30	AP
USB_GND	B31	AG
USB_HSDM	B32	AI/O
-	-	-
RESERVED	C2	-
RESERVED	C3	-
SVDDTRX4	C4	SP
SVDDTRX4	C5	SP
SGND	C6	SG
SGND	C7	SG
RESERVED	C8	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
RESERVED	C9	-
SGND	C10	SG
SGND	C11	SG
SGND	C12	SG
SGND	C13	SG
SGND	C14	SG
SGND	C15	SG
SGND	C16	SG
SGND	C17	SG
RESERVED	C18	-
DVDDH_2	C19	DP
DVDDH_1	C20	DP
DVDDH_12	C21	DP
-	-	-
-	-	-
-	-	-
PERSTB	C25	I
RESERVED	C26	-
EXT_CPU_EN	C27	I
RST_CMD_DIS	C28	I
RESERVED	C29	-
USB_VDDH	C30	AP
USB_GND	C31	AG
USB_GND	C32	AG
-	-	-
-	-	-
RESERVED	D3	-
SVDDTRX4	D4	SP
SVDDTRX4	D5	SP
SVDDTRX3	D6	SP
SVDDTRX3	D7	SP
SVDDH_2	D8	SP
SVDD_CMU2	D9	SP
SVDDCK2	D10	SP
SVDDTRX2	D11	SP
SVDDTRX2	D12	SP
SVDDTRX1	D13	SP
SVDD_CMU0	D14	SP
SVDDTRX0	D15	SP
SVDDH_0	D16	SP
RESERVED	D17	-
RESERVED	D18	-
-	-	-
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
AGND_PLL	D26	AG
AVDDH_PLL	D27	AP
AVDDL_PLL	D28	AP
USB_VDDL	D29	AP
USB_VDDL	D30	AP
PCIE_RXN	D31	AI
PCIE_RXP	D32	AI
TXP_5	E1	AO
SGND	E2	SG
SGND	E3	SG
SGND	E4	SG
SVDDCK4	E5	SP
SVDDTRX3	E6	SP
SVDDTRX3	E7	SP
-	-	-
SVDD_RGCMU2	E9	SP
-	-	-
SVDDTRX2	E11	SP
SVDDTRX2	E12	SP
SVDDTRX1	E13	SP
-	-	-
SVDDTRX0	E15	SP
-	-	-
-	-	-
DVDDH	E18	DP
DVDDH	E19	DP
DVDDH	E20	DP
DVDDL	E21	DP
DVDDL	E22	DP
DGND	E23	DG
DGND	E24	DG
-	-	-
AGND_PLL	E26	AG
AVDDH_PLL	E27	AP
AVDDL_PLL	E28	AP
USB_VDDL	E29	AP
USB_VDDL	E30	AP
PCIE_GND	E31	AG
PCIE_GND	E32	AG

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
TXN_5	F1	AO
RESERVED	F2	-
SGND	F3	SG
SGND	F4	SG
SVDD_CMU4	F5	AP
-	-	-
SVDDH_4	F7	AP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	F18	DG
DGND	F19	DG
DGND	F20	DG
DVDDL	F21	DP
DVDDL	F22	DP
DVDDL_CPU	F23	DP
DGND	F24	DG
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
PCIE_VDDL	F30	AP
PCIE_GND	F31	AG
PCIE_REFCLK_P	F32	AI
-	-	-
RESERVED	G2	-
RXP_5	G3	AI
SGND	G4	SG
SVDD_RGCMU4	G5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	G18	DG
DGND	G19	DG
DGND	G20	DG
DVDDL	G21	DP
DVDDL	G22	DP
DVDDL_CPU	G23	DP
DGND	G24	DG
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
PCIE_VDDL	G30	AP
PCIE_GND	G31	AG
PCIE_REFCLK_M	G32	AI
-	-	-
-	-	-
RXN_5	H3	AI
SVDDTRX5	H4	SP
SVDDTRX5	H5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SVDDH_CKO	H16	SP
DGND	H17	DG
DGND	H18	DG
DGND	H19	DG
DGND	H20	DG
DVDDL	H21	DP
DVDDL	H22	DP
DVDDL_CPU	H23	DP
DGND	H24	DG

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
PCIE_VDDL	H30	AP
PCIE_GND	H31	AG
PCIE_GND	H32	AG
TXP_6	J1	AO
RESERVED	J2	-
SGND	J3	SG
SVDDTRX5	J4	SP
SVDDTRX5	J5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SVDDH_CKO	J15	SP
SVDDH_CKO	J16	SP
DGND	J17	DG
DGND	J18	DG
DGND	J19	DG
DGND	J20	DG
DVDDL	J21	DP
DVDDL	J22	DP
DVDDL_CPU	J23	DP
DGND	J24	DG
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
PCIE_VDDL	J30	AP
PCIE_TXP	J31	AO
PCIE_TXN	J32	AO
TXN_6	K1	AO
RESERVED	K2	-
SGND	K3	SG
SVDDTRX6	K4	SP

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
SVDDTRX6	K5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SVDDH_CKO	K15	SP
SGND	K16	SG
DGND	K17	DG
DGND	K18	DG
DGND	K19	DG
DGND	K20	DG
DVDDL	K21	DP
DVDDL	K22	DP
DVDDL_CPU	K23	DP
DVDDL_CPU	K24	DP
-	-	-
-	-	-
-	-	-
-	-	-
RESERVED	K29	-
CKE_CKE	K30	O
RESERVED	K31	-
-	-	-
-	-	-
RESERVED	L2	-
RXP_6	L3	AI
SVDDTRX6	L4	SP
SVDDTRX6	L5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	L15	SG
SGND	L16	SG

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
DGND	L17	DG
DGND	L18	DG
DGND	L19	DG
DGND	L20	DG
DVDDL	L21	DP
DVDDL	L22	DP
DVDDL_CPU	L23	DP
DVDDL_CPU	L24	DP
-	-	-
-	-	-
RESERVED	L27	-
A3_WE_N/A14	L28	O
BA0_X	L29	O
DGND	L30	DG
ODT_X	L31	O
-	-	-
-	-	-
-	-	-
RXN_6	M3	AI
SGND	M4	SG
SVDD_CMU6	M5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	M15	SG
SGND	M16	SG
DGND	M17	DG
DGND	M18	DG
DGND	M19	DG
DGND	M20	DG
DVDDL	M21	DP
DVDDL	M22	DP
DVDDL_CPU	M23	DP
DVDDL_CPU	M24	DP
-	-	-
-	-	-
DGND	M27	DG
X_A0	M28	O

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
X_BG0	M29	O
RST_RST	M30	O
A2_BA0	M31	O
-	-	-
TXP_7	N1	AO
SGND	N2	SG
SGND	N3	SG
SGND	N4	SG
SVDD_RGCMU6	N5	SP
SVDDH_6	N6	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	N15	SG
SGND	N16	SG
DGND	N17	DG
DGND	N18	DG
DGND	N19	DG
DGND	N20	DG
DVDDL	N21	DP
DVDDL	N22	DP
DVDDL_CPU	N23	DP
DVDDL_CPU	N24	DP
-	-	-
-	-	-
DGND	N27	DG
A7_A8	N28	O
A5_A6	N29	O
DGND	N30	DG
A13_A11	N31	O
A9_A2	N32	O
TXN_7	P1	AO
RESERVED	P2	-
SGND	P3	SG
SGND	P4	SG
SVDDCK6	P5	SP
-	-	-
-	-	-
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
RESERVED	-	-
RESERVED	-	-
RESERVED	-	-
RESERVED	-	-
RESERVED	-	-
RESERVED	-	-
SGND	P15	SG
SGND	P16	SG
DGND	P17	DG
DGND	P18	DG
DGND	P19	DG
DVDDL	P20	DP
DVDDL	P21	DP
DVDDL	P22	DP
DVDDL_CPU	P23	DP
DVDDL_CPU	P24	DP
-	-	-
-	-	-
DGND	P27	DG
BA2_X	P28	O
A0_X	P29	O
WEN_A10/AP	P30	O
CASN_ACT_n	P31	O
-	-	-
-	-	-
RESERVED	R2	-
RXP_7	R3	AI
SVDDTRX7	R4	SP
SVDDTRX7	R5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	R17	DG
DGND	R18	DG
DGND	R19	DG
DVDDL	R20	DP

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
DVDDL	R21	DP
DVDDL	R22	DP
DVDDL	R23	DP
-	-	-
-	-	-
-	-	-
DGND	R27	DG
A11_A4	R28	O
RASN_PAR	R29	O
DGND	R30	DG
A14_A12/BC_N	R31	O
A1_A3	R32	O
-	-	-
-	-	-
RXN_7	T3	AI
SVDDTRX7	T4	SP
SVDDTRX7	T5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	T12	DG
DGND	T13	DG
DGND	T14	DG
DGND	T15	DG
DGND	T16	DG
DGND	T17	DG
DGND	T18	DG
DGND	T19	DG
DVDDL	T20	DP
DVDDL	T21	DP
DVDDL	T22	DP
DVDDL	T23	DP
-	-	-
-	-	-
-	-	-
DGND	T27	DG
A6_RAS_N/A16	T28	O
A8_ODT	T29	O
X_A1	T30	O
BA1_A7	T31	O
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
PWRMON	U1	AI
RESERVED	U2	-
RESERVED	U3	-
AGND_XTAL	U4	AG
SVDDTRX8	U5	SP
SVDDTRX8	U6	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	U12	DG
DGND	U13	DG
DGND	U14	DG
DGND	U15	DG
DVDDL	U16	DP
DVDDL	U17	DP
DVDDL	U18	DP
DVDDL	U19	DP
DVDDL	U20	DP
DVDDL	U21	DP
DVDDL	U22	DP
DVDDL	U23	DP
-	-	-
-	-	-
-	-	-
-	-	-
A4_A13	U28	O
A12_A9	U29	O
DGND	U30	DG
A15_BA1	U31	O
X_TEN	U32	O
XO	V1	AO
RESERVED	V2	-
RESERVED	V3	-
AVDDH_XTAL	V4	AP
SVDDTRX8	V5	SP
SVDDTRX8	V6	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	V12	DG

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
DGND	V13	DG
DGND	V14	DG
DGND	V15	DG
DVDDL	V16	DP
DVDDL	V17	DP
DVDDL	V18	DP
DVDDL	V19	DP
DVDDL	V20	DP
DVDDL	V21	DP
DVDDL	V22	DP
DVDDL	V23	DP
-	-	-
-	-	-
-	-	-
MVDDH	V27	MP
X_ALERT_1	V28	I/O
RESERVED	V29	-
CLKB_CLKB	V30	O
CLK_CLK	V31	O
-	-	-
XI	W1	AI
RESERVED	W2	-
IBRFE	W3	AI/O
AVDDL_XTAL	W4	AP
SVDDCK8	W5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	W15	SG
DGND	W16	DG
DGND	W17	DG
DGND	W18	DG
DGND	W19	DG
DVDDL	W20	DP
DVDDL	W21	DP
DVDDL	W22	DP
DVDDL	W23	DP
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
-	-	-
-	-	-
-	-	-
x_ALERT	W28	I/O
A10_A5	W29	O
RESERVED	W30	-
RESERVED	W31	-
-	-	-
-	-	-
RESERVED	Y2	-
RESERVED	Y3	-
AVDDL_BG	Y4	AP
SVDD_CMU8	Y5	SP
SVDDH_8	Y6	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	Y15	SG
DGND	Y16	DG
DGND	Y17	DG
DGND	Y18	DG
DGND	Y19	DG
DGND	Y20	DG
MVDD	Y21	MP
MVDD	Y22	MP
MVDD	Y23	MP
-	-	-
-	-	-
-	-	-
RESERVED	Y27	-
CSN_CSN	Y28	O
X_CASN/A15	Y29	O
DGND	Y30	DG
DM0_DM0_n/DBIL_n	Y31	O
DGND	Y32	DG
RESETB	AA1	AI
RESERVED	AA2	-
SGND	AA3	SG
AVDDH_BG	AA4	AP

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
SVDD_RGCMU8	AA5	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	AA15	SG
SGND	AA16	SG
DGND	AA17	DG
DVDDH	AA18	DP
DVDDH	AA19	DP
DVDDH_7	AA20	DP
MVDD	AA21	MP
MVDD	AA22	MP
MVDD	AA23	MP
-	-	-
-	-	-
-	-	-
RESERVED	AA27	-
DQ10_DQ15	AA28	I/O
DQ8_DQ13	AA29	I/O
DQ1_DQ1	AA30	I/O
DQ5_DQ5	AA31	I/O
-	-	-
TXP_8	AB1	AO
RESERVED	AB2	-
SGND	AB3	SG
AGND_BG	AB4	AG
SVDDTRX9	AB5	SP
SVDDTRX9	AB6	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	AB15	SG
SGND	AB16	SG

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
DGND	AB17	DG
DVDDH_13	AB18	DP
DVDDH	AB19	DP
DVDDH_6	AB20	DP
MVDD	AB21	MP
MVDD	AB22	MP
MVDD	AB23	MP
-	-	-
-	-	-
-	-	-
DGND	AB27	DG
DQ12_DQ9	AB28	I/O
DQ14_DQ11	AB29	I/O
DGND	AB30	DG
DQ3_DQ3	AB31	I/O
DQ7_DQ7	AB32	I/O
TXN_8	AC1	AO
RESERVED	AC2	-
SGND	AC3	SG
AGND_BG	AC4	AG
SVDDTRX9	AC5	SP
SVDDTRX9	AC6	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	AC15	SG
SGND	AC16	SG
-	-	-
DVDDH_3	AC18	DP
DVDDH_4	AC19	DP
DVDDH_5	AC20	DP
MVDD	AC21	MP
MVDD	AC22	MP
MVDD	AC23	MP
-	-	-
-	-	-
-	-	-
DGND	AC27	DG
DQ4_DQ4	AC28	I/O

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
DQS1_DQS1	AC29	I/O
DQS1B_DQS1B	AC30	I/O
DQ6_DQ2	AC31	I/O
-	-	-
-	-	-
RESERVED	AD2	-
RXP_8	AD3	AI
SVDDTRX10	AD4	SP
SVDDTRX10	AD5	SP
SVDDCK10	AD6	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SGND	AD15	SG
SGND	AD16	SG
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	AD27	DG
DQ13_DQ10	AD28	I/O
DQ15_DQ8	AD29	I/O
DGND	AD30	DG
DQ2_DQ6	AD31	I/O
DQ0_DQ0	AD32	I/O
-	-	-
-	-	-
RXN_8	AE3	AI
SVDDTRX10	AE4	SP
SVDDTRX10	AE5	SP
-	-	-
-	-	-
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SVDDH_CKO	AE15	SP
SVDDH_CKO	AE16	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DQ11_DQ14	AE27	I/O
DM1_DM1_n/DBIU_n	AE28	O
DQ9_DQ12	AE29	I/O
DQS0B_DQS0B	AE30	I/O
DQS0_DQS0	AE31	I/O
-	-	-
TXP_9	AF1	AO
SGND	AF2	SG
SGND	AF3	SG
SGND	AF4	SG
SVDD_RGCMU10	AF5	SP
SVDDH_10	AF6	SP
-	-	-
SVDDH_12	AF8	SP
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
SVDDH_CKO	AF16	SP
-	-	-
-	-	-
-	-	-
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
DGND	AF27	DG
DGND	AF28	DG
DGND	AF29	DG
DGND	AF30	DG
DM2_DM2_n/DBIL_n	AF31	O
DGND	AF32	DG
TXN_9	AG1	AO
RESERVED	AG2	-
SGND	AG3	SG
SGND	AG4	SG
SGND	AG5	SG
SVDD_CMU10	AG6	SP
SGND	AG7	SG
SVDDCK12	AG8	SP
-	-	-
SVDD_CMU12	AG10	SP
DDR_DATA_BUS	AG11	I
RESERVED	AG12	-
RESERVED	AG13	-
RESERVED	AG14	-
BOOT_SEL	AG15	I
DDR_TYPE_SEL_1	AG16	I
-	-	-
RESERVED	AG18	-
GPIO_17 / SDA2	AG19	I/O
GPIO_20 / SDA5	AG20	I/O
GPIO_26 / SDA11	AG21	I/O
RESERVED	AG22	-
RESERVED	AG23	-
UART1_RTS#	AG24	O
UART1_CTS#	AG25	I
UART0_RTS#	AG26	O
DGND	AG27	DG
DQ26_DQ31	AG28	I/O
DQ24_DQ29	AG29	I/O
DQ17_DQ17	AG30	I/O
DQ21_DQ21	AG31	I/O
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
-	-	-
RESERVED	AH2	-
SVDDTRX11	AH3	SP
SVDDTRX11	AH4	SP
SVDDTRX12	AH5	SP
SVDDTRX12	AH6	SP
SGND	AH7	SG
SVDD_RGCMU12	AH8	SP
SVDDTRX13	AH9	SP
SVDDTRX13	AH10	SP
IFU_PATCH_EN	AH11	I
RESERVED	AH12	-
RESERVED	AH13	-
RESERVED	AH14	-
I2C_DATA_ENDIAN_SEL	AH15	I
DDR_TYPE_SEL_0	AH16	I
GPIO_27	AH17	I/O
RESERVED	AH18	-
GPIO_16 / SDA1	AH19	I/O
GPIO_19 / SDA4	AH20	I/O
GPIO_25 / SDA10	AH21	I/O
GPIO_12 / SPI_CS#1	AH22	I/O
GPIO_5 / JTAG_TRST#	AH23	I/O
RESERVED	AH24	-
UART1_TXD	AH25	O
UART0_CTS#	AH26	I
DGND	AH27	DG
DQ28_DQ25	AH28	I/O
DQ30_DQ27	AH29	I/O
DGND	AH30	DG
DQ19_DQ19	AH31	I/O
DQ23_DQ23	AH32	I/O
RXP_9	AJ1	AI
SGND	AJ2	SG
SVDDTRX11	AJ3	SP
SVDDTRX11	AJ4	SP
SVDDTRX12	AJ5	SP
SVDDTRX12	AJ6	SP
SGND	AJ7	SG
SGND	AJ8	SG
SVDDTRX13	AJ9	SP
SVDDTRX13	AJ10	SP
RESERVED	AJ11	-
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
RESERVED	AJ13	-
-	-	-
RESERVED	AJ15	-
-	-	-
GPIO_31 / LED_SYNC	AJ17	I/O
-	-	-
GPIO_15 / SDA0	AJ19	I/O
-	-	-
GPIO_24 / SDA9	AJ21	I/O
-	-	-
GPIO_3 / JTAG_TMS	AJ23	I/O
-	-	-
UART1_RXD	AJ25	I
-	-	-
DGND	AJ27	DG
DQS3_DQS3	AJ28	I/O
DQS3B_DQS3B	AJ29	I/O
DQ20_DQ20	AJ30	I/O
DQ22_DQ18	AJ31	I/O
-	-	-
RXN_9	AK1	AI
SGND	AK2	SG
RXP_10	AK3	AI
RXN_10	AK4	AI
SGND	AK5	SG
SGND	AK6	SG
RXP_11	AK7	AI
RXN_11	AK8	AI
SGND	AK9	SG
SGND	AK10	SG
RESERVED	AK11	-
RESERVED	AK12	-
SGND	AK13	SG
SGND	AK14	SG
RESERVED	AK15	-
RESERVED	AK16	-
GPIO_28	AK17	I/O
LED_SDA / LED_MDIO	AK18	I/O
GPIO_13 / SCL0	AK19	I/O
GPIO_18 / SDA3	AK20	I/O
GPIO_23 / SDA8	AK21	I/O
GPIO_11 / SPI_CS#0	AK22	I/O
GPIO_4 / JTAG_TCK	AK23	I/O
GPIO_6 / JTAG_TDI	AK24	I/O

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
GPIO_0 / SYS_LED	AK25	I/O
SPI_SLV_SDO	AK26	O
-	-	-
DQ29_DQ26	AK28	I/O
DQ31_DQ24	AK29	I/O
DGND	AK30	DG
DQ18_DQ22	AK31	I/O
DQ16_DQ16	AK32	I/O
RESERVED	AL1	-
RESERVED	AL2	-
RESERVED	AL3	-
-	-	-
SGND	AL5	SG
RESERVED	AL6	-
RESERVED	AL7	-
-	-	-
RESERVED	AL9	-
RESERVED	AL10	-
RESERVED	AL11	-
-	-	-
SGND	AL13	SG
RESERVED	AL14	-
RESERVED	AL15	-
-	-	-
MDIO_2	AL17	I/O
LED_SCK / LED_MDC	AL18	O
GPIO_30 / SC_MDIO	AL19	I/O
GPIO_14 / SCL1	AL20	I/O
GPIO_22 / SDA7	AL21	I/O
GPIO_10 / SPI_MOSI	AL22	I/O
GPIO_8 / SPI_SCK	AL23	I/O
GPIO_7 / JTAG_TDO	AL24	I/O
GPIO_2 / GPIO_MDIO	AL25	I/O
SPI_SLV_CS#	AL26	I
DM3_DM3_n/DBIU_n	AL27	O
DQ27_DQ30	AL28	I/O
DQ25_DQ28	AL29	I/O
DQS2B_DQS2B	AL30	I/O
DQS2_DQS2	AL31	I/O
-	-	-
TXP_10	AM1	AO
TXN_10	AM2	AO
-	-	-
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
TXP_11	AM5	AO
TXN_11	AM6	AO
-	-	-
-	-	-
RESERVED	AM9	-
RESERVED	AM10	-
-	-	-
-	-	-
RESERVED	AM13	-
RESERVED	AM14	-
-	-	-
-	-	-
MDC_2	AM17	O
-	-	-

RTL9311R (24G+4*10G) Pin Name	Pin No.	Type
GPIO_29 / SC_MDC	AM19	I/O
-	-	-
GPIO_21 / SDA6	AM21	I/O
-	-	-
GPIO_9 / SPI_MISO	AM23	I/O
-	-	-
GPIO_1 / GPIO_MDC	AM25	I/O
-	-	-
SPI_SLV_SDI / I2C_SDA	AM27	I/O
SPI_SLV_SCLK / I2C_SCK	AM28	I
UART0_RXD	AM29	I
UART0_TXD	AM30	O
RESERVED	AM31	-
-	-	-

6. Pin Descriptions

6.1. DDR3 SDRAM Interface

Table 2. DDR3 SDRAM Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
DQ[31:0]	AK29, AH29, AK28, AH28, AL28, AG28, AL29, AG29, AH32, AJ31, AG31, AJ30, AH31, AK31, AG30, AK32, AD29, AB29, AD28, AB28, AE27, AA28, AE29, AA29, AB32, AC31, AA31, AC28, AB31, AD31, AA30, AD32	I/O	Data Input/Output: Bi-directional data bus. These pins must be floating when not used.
A[15:0]	U31, R31, N31, U29, R28, W29, N32, T29, N28, T28, N29, U28, L28, M31, R32, P29	O	Address Outputs.
BA[2:0]	P28, T31, L29	O	Bank Address Outputs.
DM[3:0]	AL27, AF31, AE28, Y31	O	Data Masks.
RASN, CASN, WEN	R29, P31, P30	O	Command Outputs: RASN, CASN, WEN (along with CS#) define the command being entered.
CSN	Y28	O	Chip Select: CSN enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CSN is registered HIGH.
CLK, CLKB	V31, V30	O	Clock: CLK and CLKB are differential clock outputs.
CKE	K30	O	Clock Enable: CKE HIGH activates.
DQS0, DQS0B, DQS1, DQS1B, DQS2, DQS2B, DQS3, DQS3B	AE31, AE30 AC29, AC30 AL31, AL30 AJ28, AJ29	I/O	Data strobe. These pins must be floating when not used.
RST	M30	O	Active Low Reset.
ODT	L31	O	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM.

6.2. DDR4 SDRAM Interface

Table 3. DDR4 SDRAM Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
DQ[31:0]	AG28, AL28, AG29, AL29, AH29, AK28, AH28, AK29, AH32, AK31, AG31, AJ30, AH31, AJ31, AG30, AK32, AA28, AE27, AA29, AE29, AB29, AD28, AB28, AD29, AB32, AD31, AA31, AC28, AB31, AC31, AA30, AD32	I/O	Data Input/Output: Bi-directional data bus. These pins must be floating when not used.
A[16:0]	T28, Y29, L28, U28, R31, N31, P30, U29, N28, T31, N29, W29, R28, R32, N32, T30, M28	O	Address Outputs.
BA[1:0]	U31, M31	O	Bank Address Outputs.
DM3_n/DBIU_n DM2_n/DBIL_n DM1_n/DBIU_n DM0_n/DBIL_n	AL27, AF31, AE28, Y31	O	Data Masks and Data Bus Inversion.
RAS_N/A16, CASN/A15, WE_N/A14	T28 Y29 L28	O	Command Outputs: RASN, CASN, WEN (along with CS#) define the command being entered.
CSN	Y28	O	Chip Select: CSN enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CSN is registered HIGH.
CLK, CLKB	V31, V30	O	Clock: CLK and CLKB are differential clock outputs.
CKE	K30	O	Clock Enable: CKE HIGH activates.
DQS0, DQS0B, DQS1, DQS1B, DQS2, DQS2B, DQS3, DQS3B	AE31, AE30 AC29, AC30 AL31, AL30 AJ28, AJ29	I/O	Data strobe. These pins must be floating when not used.
RST	M30	O	Active Low Reset.
ODT	T29	O	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM.
ACT_n	P31	O	Activation command output
BG0	M29	O	Bank group output
A10/AP	P30	O	Auto-precharge
A12/BC_N	R31	O	Burst chop
PAR	R29	O	Command and address parity output
ALERT, ALERT_1	W28, V28	I/O	Alert: It has multi functions such as CRC error flag, command and address parity error flag. These pins must be connected to MVDD with 10K ohm resistor.
TEN	U32	O	Connectivity test mode enable

6.3. SPI Flash Controller Interface

Table 4. SPI Flash Controller Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
SPI_CS#[1:0]	B24, A24	O	Chip select 1-0.
SPI_SCLK	A23	O	Clock output.
SPI_SDI/SIO0	B21	I/O	Serial data output (for 1Xi/O)/ Serial data input & output (for 2Xi/O or 4Xi/O). This pin must be floating when not used.
SPI_SDO/SIO1	A21	I/O	Serial data input (for 1Xi/O)/ Serial data input & output (for 2Xi/O or 4Xi/O). This pin must be floating when not used.
SPI_SIO2	A22	I/O	Serial data input & output (for 4Xi/O). This pin must be floating when not used.
SPI_SIO3	B22	I/O	Serial data input & output (for 4Xi/O). This pin must be floating when not used.
SPI_RSTN	B23	O	Hardware Reset output (active low)

6.4. UART Interface

Table 5. UART Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
UART0_TXD	AM30	O	UART0 Interface Transmit Data.
UART0_RXD	AM29	I	UART0 Interface Receive Data. This pin must be pulled high with a 10K ohm resistor when not used.
UART0_RTS#	AG26	O	UART0 Interface Request to Send.
UART0_CTS#	AH26	I	UART0 Interface Clear to Send. This pin must be pulled low with a 1K ohm resistor when not used.
UART1_TXD	AH25	O	UART1 Interface Transmit Data.
UART1_RXD	AJ25	I	UART1 Interface Receive Data. This pin must be pulled high with a 10K ohm resistor when not used.
UART1_RTS#	AG24	O	UART1 Interface Request to Send.
UART1_CTS#	AG25	I	UART1 Interface Clear to Send. This pin must be pulled low with a 1K ohm resistor when not used.

6.5. EJTAG Interface

Table 6. EJTAG Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
JTAG_TMS	AJ23	I	JTAG Test Mode Select. This pin must be floating when not used.
JTAG_TCK	AK23	I	JTAG Test Clock Input. This pin must be floating when not used.
JTAG_TRST#	AH23	I	JTAG Test Reset. *Note: The pin must be external pulled down via a 1Kohm resistor.* This pin must be floating when not used.
JTAG_TDI	AK24	I	JTAG Test Data Input. This pin must be floating when not used.
JTAG_TDO	AL24	O	JTAG Test Data Output.

6.6. GPIO Interface

Table 7. GPIO Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
GPIO[31:0]	AJ17, AL19, AM19, AK17, AH17, AG21, AH21, AJ21, AK21, AL21, AM21, AG20, AH20, AK20, AG19, AH19, AJ19, AL20, AK19, AH22, AK22, AL22, AM23, AL23, AL24, AK24, AH23, AK23, AJ23, AL25, AM25, AK25	I/O	General Purpose Input/Output. Provides configurable I/O ports that can be configured for either input or output. These pins must be floating when not used. GPIO[5] cannot connect with internal pull high device.

6.7. XSGMII Interface

Table 8. XSGMII Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
TXP_[7:5]/ TXN_[7:5]	N1, J1, E1 P1, K1, F1	AO	XSGMII (10.3125G) Transmit Data Differential Output Pair.
RXP_[7:5]/ RXN_[7:5]	R3, L3, G3 T3, M3, H3	AI	XSGMII (10.3125G) Receive Data Differential Input Pair. These pins must be connected with a series 50 ohm resistor and a 0.1 uF capacitor to ground when not used.

6.8. 10G Base-R Interface

Table 9. 10G Base-R Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
TXP_[11:8]/ TXN_[11:8]	AM5, AM1, AF1, AB1 AM6, AM2, AG1, AC1	AO	10G Base-R (10.3125G) Transmit Data Differential Output Pair.
RXP_[11:8]/ RXN_[11:8]	AK7, AK3, AJ1, AD3 AK8, AK4, AK1, AE3	AI	10G Base-R (10.3125G) Receive Data Differential Input Pair. These pins must be connected with a series 50 ohm resistor and a 0.1 uF capacitor to ground when not used.

6.9. USB Interface

Table 10. USB Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
USB_HSDM USB_HSDP	B32 A32	AI/O	USB Date Differential input/output Pair.

6.10. PCIE Interface

Table 11. PCIE Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
PCIE_TXP PCIE_TXN	J31 J32	AO	PCIE Transmit Data Differential Output Pair.
PCIE_RXP PCIE_RXN	D32 D31	AI	PCIE Receiver Data Differential Input Pair. These pins must be floating when not used.
PCIE_REFCLK_P PCIE_REFCLK_M	F32 G32	AI	PCIE Differential Clock Input Pair. (100Mhz) These pins must be floating when not used.
PERSTB	C25	I	For PCIE Device Reset. This pin must be floating when not used.

6.11. LED Interface

Table 12. LED Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
LED_SCK	AL18	O	Shift register clock output.
LED_SDA	AK18	O	Serial data output.
LED_SYNC	AJ17	O	Storage register clock output.
LED_MDC	AL18	O	Controller Clock for scan LED Mode.
LED_MDIO	AK18	I/O	Controller Data for serial LED Mode. This pin must be floating when not used.
SYS_LED	AK25	O	System LED.
USB_LED	A31	O	USB LED.

6.12. Miscellaneous Interface

Table 13. Miscellaneous Interface Pins

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
MDC_0	A20	O	MII 0 Management Interface Clock Pin.
MDIO_0	B20	I/O	MII 0 Management Interface Data Pin. This pin must be floating when not used.
MDC_1	A19	O	MII 1 Management Interface Clock Pin.
MDIO_1	B19	I/O	MII 1 Management Interface Data Pin. This pin must be floating when not used.
MDC_2	AM17	O	MII 2 Management Interface Clock Pin.
MDIO_2	AL17	I/O	MII 2 Management Interface Data Pin. This pin must be floating when not used.
XI	W1	AI	25MHz Crystal Clock Input Pin.
XO	V1	AO	25MHz Crystal Clock Output Pin.
RESETB	AA1	AI	System Pin Reset Input.
IBREF	W3	AI/O	Reference Resistor for BG. A 12KΩ (1%) resistor should be connected between IBREF and GND.
PWRMON	U1	AI	For power monitor use. This pin must be floating when not used.
RST_OUT	B25	O	For reset other device.
RESERVED	B28, C26, B26, Y3, AA2, AJ15, AG14, AH13, U3, AG12		Reserved. Must be pulled down with a 1K ohm resistor in normal operation.
RESERVED	A28, V3, AG13, W2, Y2, U2, V2, AH14		Reserved. Must be pulled up with a 10K ohm resistor in normal operation.
RESERVED	A18, B18, AM31		Reserved. Must be connected with a bead to DVDDH.
RESERVED	A13, A15, B13, B15, C9, C8, A4, A3, C3, D3, AK11, AK12, AK15, AK16		Reserved. Must be connected with a series 50 ohm resistor and a 0.1 uF capacitor to ground.
RESERVED	A2, A14, A16, A17, B2, B5, B6, B9, B10, B11, B14, B16, C2, F2, G2, J2, K2, K29, K31, L2, P2, R2, Y27, AA27, AB2, AC2, AD2, AG2, AH2, AL1, AL2, AL3, AL6, AL7, AL9, AL10, AL11, AL14, AL15, AJ13, AH12, AJ11, A25, A26, B29, C29, AG18, AH18, AG22, AG23, AH24, D17, A29, L27, V29, W30, W31, A11, A10, A7, A6, A1, B1, AM9, AM10, AM13, AM14		Reserved. Must be floating in normal operation.
RESERVED	C18		Reserved. Must be connected to DVDDL.
RESERVED	D18		Reserved. Must be connected to DGND

6.13. Configuration (Pin Strapping Function)

Table 14. Configuration Strapping Pins

Pin Name	Pin No.	Default	Description
	RTL9311R(24G+4*10G)		
SYS_LED_EN	B27	0b1	When enable System LED, the GPIO[0] change to system LED pin. 0b0: Disable system LED 0b1: Enable system LED
EXT_CPU_EN	C27	0b0	Enable external CPU. 0b0: Disable 0b1: Enable
DDR_TYPE_SEL [1:0]	AG16, AH16	0b00	DDR type selection. 0b00: DDR3 0b01: DDR4 0b10: Reserved 0b11: Reserved
BOOT_SEL	AG15	0b0	Boot selection. 0b0: SPI-NOR 0b1: ROM (SPI-NAND)
RST_CMD_DIS	C28	0b1	Indicated whether issuing 0x66, 0x99 SPI flash commands or not when before booting from SPI flash. 0b0: Issue 0x66, 0x99 SPI flash commands. 0b1: Issue no reset command.
DDR_DATA_BUS	AG11	0b0	Select DDR data bus width. 0b0: DQ16 0b1: DQ32
HW_RESET_EN	A30	0b1	Triggering hardware reset signal or not before booting from SPI flash. 0b0: Don't trigger hardware reset signal 0b1: Trigger hardware reset signal
iFU_PATCH_EN	AH11	0b1	Enable iA patch updated. 0b0: Disable 0b1: Enable

6.14. Power and GND

Table 15. Power and GND Pins

Pin Name	Pin No.	Type	Description
	RTL9311P(24G+4*10G)		
SVDDTRX0	D15, E15	SP	SERDES TX/RX Low Voltage Power.
SVDDTRX1	D13, E13		
SVDDTRX2	D11, D12, E11, E12		
SVDDTRX3	D6, D7, E6, E7		
SVDDTRX4	C4, C5, D4, D5		

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
SVDDTRX5	H4, H5, J4, J5		
SVDDTRX6	K4, K5, L4, L5		
SVDDTRX7	R4, R5, T4, T5		
SVDDTRX8	U5, U6, V5, V6		
SVDDTRX9	AB5, AB6, AC5, AC6		
SVDDTRX10	AD4, AD5, AE4, AE5		
SVDDTRX11	AH3, AH4, AJ3, AJ4		
SVDDTRX12	AH5, AH6, AJ5, AJ6		
SVDDTRX13	AH9, AH10, AJ9, AJ10		
SVDD_CMU0,2,4,6,8,10,12	D14, D9, F5, M5, Y5, AG6, AG10	SP	SERDES CMU Low Voltage Power.
SVDD_RGCMU2,4,6,8,10,12	E9, G5, N5, AA5, AF5, AH8	SP	SERDES RGCMU Low Voltage Power.
SVDDCK2,4,6,8,10,12	D10, E5, P5, W5, AD6, AG8	SP	SERDES CK Low Voltage Power.
SVDDH_CKO	H16, J16, J15, K15, AE15, AE16, AF16	SP	SERDES CKO High Voltage Power.
SVDDH_0,2,4,6,8,10,12	D16, D8, F7, N6, Y6, AF6, AF8	SP	SERDES High Voltage Power.
AVDDL_BG	Y4	AP	BG Low Voltage Power.
AVDDH_BG	AA4	AP	BG High Voltage Power.
AVDDL_XTAL	W4	AP	XTAL Low Voltage Power.
AVDDH_XTAL	V4	AP	XTAL High Voltage Power.
AVDDL_PLL	D28, E28	AP	PLL Low Voltage Power.
AVDDH_PLL	D27, E27	AP	PLL High Voltage Power.
PCIE_VDDL	F30, G30, H30, J30	AP	PCIE Low Voltage Power.
USB_VDDL	D29, D30, E29, E30	AP	USB Low Voltage Power.
USB_VDDH	B30, C30	AP	USB High Voltage Power.
MVDDH	V27	MP	DDR Controller High Voltage Power.
MVDD	Y21-23, AA21-23, AB21-23, AC21-23	MP	DDR Controller Low Voltage Power.
DVDDH	E18-20, AA18, AA19, AB19	DP	Digital Power for I/O Pins.
DVDDH_1	C20	DP	Digital Power for Group_1 I/O Pins.
DVDDH_2	C19	DP	Digital Power for Group_2 I/O Pins.
DVDDH_3	AC18	DP	Digital Power for Group_3 I/O Pins.
DVDDH_4	AC19	DP	Digital Power for Group_4 I/O Pins.
DVDDH_5	AC20	DP	Digital Power for Group_5 I/O Pins.
DVDDH_6	AB20	DP	Digital Power for Group_6 I/O Pins.
DVDDH_7	AA20	DP	Digital Power for Group_7 I/O Pins.
DVDDH_12	C21	DP	Digital Power for Group_12 I/O Pins.
DVDDH_13	AB18	DP	Digital Power for Group_13 I/O Pins.

Pin Name	Pin No.	Type	Description
	RTL9311R(24G+4*10G)		
DVDDL	E21, E22, F21, F22, G21, G22, H21, H22, J21, J22, K21, K22, L21, L22, M21, M22, N21, N22, P20-22, R20-23, T20-23, U16-23, V16-23, W20-23	DP	Digital Low Power for Digital Core.
DVDDL_CPU	F23, G23, H23, J23, K23, K24, L23, L24, M23, M24, N23, N24, P23, P24	DP	Digital Low Power for CPU.
DGND	E23, E24, F18-20, F24, G18-20, G24, H17-20, H24, J17-20, J24, K17-20, L17-20, L30, M17-20, M27, N17-20, N27, N30, P17-19, P27, R17-19, R27, R30, T12-19, T27, U12-15, U30, V12-15, W16-19, Y16-20, Y30, Y32, AA17, AB17, AB27, AB30, AC27, AD27, AD30, AF27-30, AF32, AG27, AH27, AH30, AJ27, AK30	DG	Digital Ground.
SGND	A12, B3, B4, B7, B12, B17, C6, C7, C10-17, E2-4, F3, F4, G4, J3, K3, K16, L15, L16, M4, M15, M16, N2-4, N15, N16, P3, P4, P15, P16, W15, Y15, AA3, AA15, AA16, AB3, AB15, AB16, AC3, AC15, AC16, AD15, AD16, AF2-4, AG3-5, AG7, AH7, AJ2, AJ7, AJ8, AK2, AK5, AK6, AK9, AK10, AK13, AK14, AL5, AL13	SG	SERDES Ground.
AGND_BG	AB4, AC4	AG	BG Ground.
AGND_XTAL	U4	AG	XTAL Ground.
AGND_PLL	D26, E26	AG	PLL Ground
PCIE_GND	E31, E32, F31, G31, H31, H32	AG	PCIE Ground
USB_GND	B31, C31, C32	AG	USB Ground

7. Switch Function Description

7.1. Hardware Reset and Software Reset

7.1.1. Hardware Reset

A hardware reset forces the device to start the initial power-on sequence. The hardware will strap pins to give all default values when the 'RESET' signal terminates. Next the configuration is cleared to chip default, and then the complete SRAM BIST (Built-In Self Test) process is run. Finally the packet buffer descriptors are initialized and internal registers can be accessed by the internal/external CPU.

7.1.2. Software Reset

The device supports three software resets, CPU&Memory reset, Switch NIC reset, and Switch chip reset. Reset sources are the signals that will trigger the reset command to the chip. All reset signals are low active.

- CPU & Memory reset: Resets MIPS InterAptive + Memory Controller + Peripheral + NIC
- Switch NIC reset: Resets NIC interface between CPU and Switch
- Switch chip reset: Resets whole switch core

7.2. Layer 2 Learning and Forwarding

The device has a 4K-entry VLAN table which is used by 802.1Q and Q-in-Q VLAN. It supports 4K FID (Filtering Database ID) in total. IVL (Individual VLAN Learning), SVL (Shared VLAN learning) and IVL/SVL mixed mode are supported and per VLAN basis can specify the VLAN learning mode for unicast/broadcast and L2/IP multicast traffic respectively.

7.2.1. Forwarding

IP multicast data packets involve L2 and port-mask table lookup. If the L2 table lookup returns a hit, the data packet is forwarded to all member ports and router ports retrieved from port-mask table. If the multicast address is not stored in the address table (i.e., lookup miss), the packet is broadcast to all ports of the broadcast domain. The VLAN Frame Forwarding Rules are defined as follows:

The received unknown unicast/unknown multicast/broadcast frame will be flooded to configured flooding ports within VLAN domain and the source port is excluded.

The received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded.

7.2.2. Learning

The device features a 32K-entry Layer 2 table. It uses a 2-left 4-way hashing structure to store L2 entries so that it could provide higher learning capability. Each entry can be recorded in one of the two formats, L2 Unicast and L2 Multicast. Both L2 Unicast and Multicast use (FID/VID, MAC) as hash key.

The learnt unicast entries are aged out after the specified aging period. The device per port supports a configuration to disable the aging out function.

7.2.3. MAC Filtering

Support Source/Destination MAC filtering or Secure Source MAC Address mode that device only accepts packets whose SA is known to system.

7.2.4. MAC Address Notification

Whenever Layer 2 table has changed by hardware, system could send a notification event to CPU to keep software database update-to-date. Such event includes New-learn, Aging-out and Station-move.

7.3. Layer 2 Learning Constraint

The device supports system-based, port-based, and VLAN-based layer 2 learning constraint. The function is to limit the number of learnt MAC addresses on the system, particularly port and VLAN.

For system-based learning constraint, there is a configuration for users to define the MAC address numbers that the system can learn. For port-based learning constraint, each port has a configuration to define the MAC address number that the port can learn. For VLAN-based learning constraint, there are 32 configurations supported to define the MAC address number that the particular VLAN can learn.

The packets are dropped, forwarded, or trapped to the CPU when the learnt L2 entries number reaches the limited number. Three learning constraint functions can work simultaneously and the action priority is Drop > Trap > Forward if the learning constraint actions are triggered at the same time.

7.4. Port Isolation

Port Isolation function is used to control whether the hosts can communicate with each other or not.

If we set the register to cut the connection between hosts, all packets from a host (downlink port) cannot be transmitted to another host directly. These packets can only be transmitted by passing through the router (uplink port) as illustrated below.

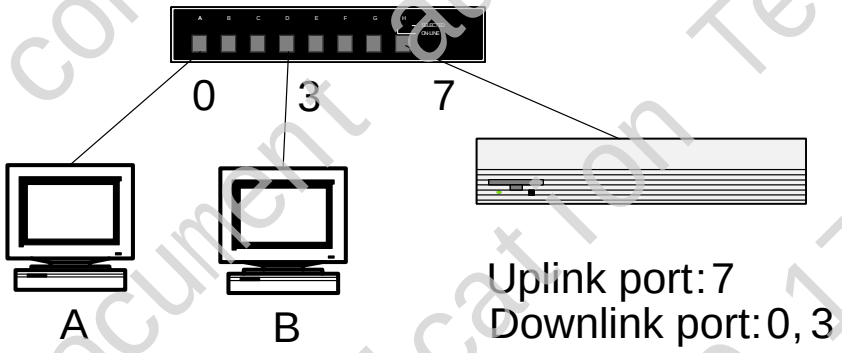


Figure 6. Port Isolation Example

Port-based port isolation is archived by providing a port mask configuration for each ingress port. The port mask is used to indicate the ports that allow forwarding of traffic.

The Mirroring function is not limited by the port isolation port mask, that is, the mirroring port does not have to be within the port mask.

In addition to port-based port isolation, there are 32 VLAN-based port isolation configurations supported in the device. Each configuration can specify the VLAN ID, Port Mask, and the enable state. The port mask definition of VLAN-based port isolation is different from port-based port isolation. Ports configured as 1 in this port mask could communicate with all ports belonging to the same specified VLAN while

ports configured as 0 could only communicate with ports configured as 1 belonging to the same specified VLAN.

7.5. Layer 2 Multicast and IP Multicast

There are two IP multicast frame types supported in device: IPv4 multicast and IPv6 multicast.

An IPv4 multicast frame must satisfy two conditions:

- The type must be IPv4
- DMAC =01-00-5E-XX-XX-XX

An IPv6 multicast frame must satisfy two conditions:

- The type must be IPv6
- DMAC =0x33-33-XX-XX-XX-XX

A packet is deemed a L2 multicast packet if it is not an IP multicast packet and DMAC[40]=1.

The device supports IGMPv1/2/3 and MLDv1/2. IGMP/MLD control packets can be trapped to the CPU for software to insert an IP multicast entry into the L2 table.

7.6. Reserved Multicast Address

There are several Reserved Multicast Address (RMA) definitions in the IEEE 802.1 standard. The device provides individual action for the RMA range from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F and four user defined RMA support. The action of each RMA includes Forward, Drop, and Trap to local/master CPU. Moreover, some specific RMA could be able to act as flood to all port. For application requirement, the RMA action has capability to bypass VLAN filtering and STP blocking while the action is set as "Trap to CPU". The most RMA action is system-wise, except for PTP/LLDP/EAPOL/BPDU are port-based configuration.

7.7. IEEE 802.1d/1w/1s (STP/RSTP/MSTP)

There are 128 spanning tree instances supported by the device. The CPU creates a different Port State for different spanning tree instances at each port. The device assigns a VID for a received packet, and look up the VLAN table to retrieve the Multiple Spanning Tree Instances (MSTI). Then it follows the port's MSTI state to complete its corresponding ingress/egress check. The Spanning Tree and Rapid Spanning Tree port states are shown below.

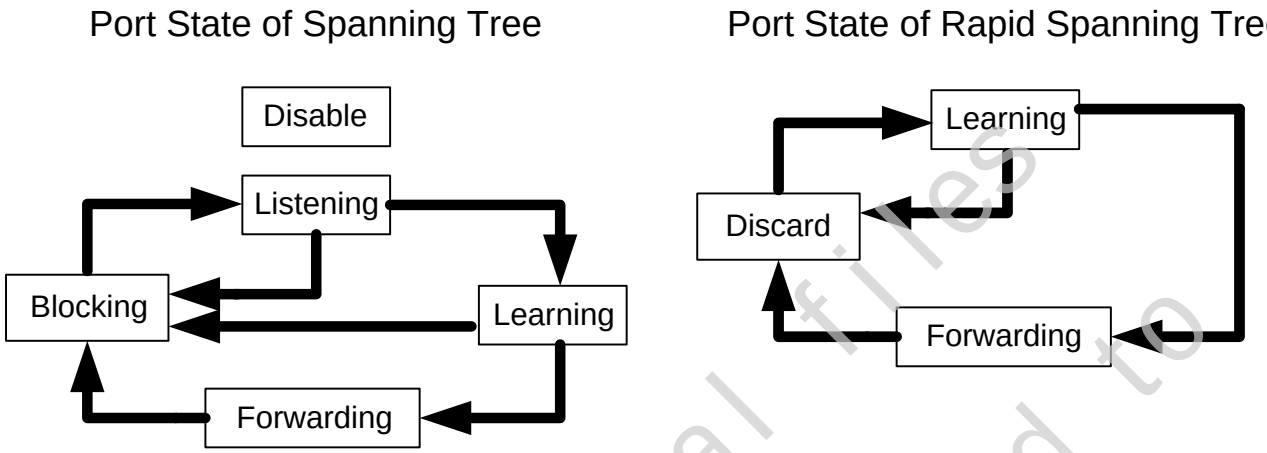


Figure 7. Spanning Tree and Rapid Spanning Tree Port States

When using IEEE 802.1D/1w/1s, the device supports four states for each port per instance:

- Disable

Except for software forwarding, the port will not transmit/receive packets, and will not perform learning.

- Blocking/Listening

Except for software forwarding, the port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning.

- Learning

The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets.

- Forwarding

The port will transmit/receive all packets, and will perform learning.

7.8. IEEE 802.1Q and Q-in-Q VLAN

The device has a 4K-entry VLAN table that is used by 802.1Q and Q-in-Q VLAN and shared by C-VLAN and S-VLAN. Up to three layer VLAN tags (Outer Tag, Inner Tag, Extra Tag) are supported for Q-in-Q applications. The device supports global four outer TPIDs, four inner TPIDs and one extra TPID which are all configurable and per port has a TPID mask to select the recognized TPID. For VLAN tag manipulation, VLAN untag set and the egress port tag status configurations are coordinated for determining the tag status for a packet.

Per ingress port and per tag status can specify the forwarding VLAN is either from inner tag or outer tag. Forwarding VLAN is used for doing VLAN table lookup and ingress/egress VLAN filtering.

The device also supports 8 protocol-based (IEEE 802.1v), 2K MAC-based/IP-subnet-based (shared with Ingress VLAN translation), and application-based VLANs.

Per VLAN provides a 16-bit group mask which can be used as a key by ACL, and provides forwarding options of some predefined types of packets (e.g. IGMP, MLD, DHCP, and ARP) for VLAN-based applications.

7.9. Ingress and Egress VLAN Translation

The device supports 2K ingress (shared with MAC-based/IP-based VLAN) and 1K egress VLAN translation table. They are used to support the 1:1 and port-based N:1 VLAN translation. For MAC-based N:1 VLAN translation, per egress port has a configuration to enable the function. In addition to the dedicated VLAN translation tables, VLAN translation can also be done by ACL.

For ingress VLAN translation, support (S+C/S/C/untag, ingress port) to (S'+C'/S'/C'/untag) translation. For egress VLAN translation, support (S+C/S/C/untag, egress port) to (S'+C'/S'/C'/untag) translation.

7.10. IEEE 802.3ad Link Aggregation

The device supports 802.3ad (Link Aggregation) for 26 groups (stand-alone mode)/ 128 groups (stacking mode) of link aggregators with up to 8 ports per-group. In stacking mode, a link aggregation group can contain member ports on different stacking devices.

Link aggregation group frames are sent to an aggregation port of the link aggregation group according to a distribution algorithm. Two trunk distribution algorithms are supported and per group can bind to a specific distribution algorithm. L2 and L3 packet can have different parameters of the distribution algorithm.

Each trunk group can optionally separate the known multicast and flooding traffic to the MSB port. Besides, H/W fail-over is also supported to prevent forwarding traffic to a link down port in stand-alone mode.

7.11. Mirroring and Sampling

There are four mirror configurations supported in the device. Each mirror configuration can specify the ingress and egress mirrored ports, mirroring port, isolation state, and enable state. Normal forwarding packet cannot be forwarded to the mirroring port if isolation state is enabled. The mirrored traffic can cross the VLAN, that is, the mirrored port and mirroring port can reside in different VLANs.

Multiple mirrored ports are matched for a multiple egress port packet; the packet transmitted through the lowest mirrored port ID is duplicated to the mirroring port. The mirroring port drops the mirrored traffic instead of triggering the flow control if it is congested.

The device supports ingress and egress port sFlow sampling. Each mirror session can specify the sample rate for packet sampling.

Mirror across stacking devices is supported. Ingress/egress mirrored ports and mirroring port can be on different stacking devices.

Flow-based mirroring and sampling can be supported by ACL.

7.12. Attack Prevention

Most common attacks can be blocked by the device including LAND attack, UDP Blat attack, TCP Blat attack, Ping of Death attack, Smurf attack, TCP NULL scan and so on. The attack prevention function is per port enabled and each attack type is globally enabled. Each attack type packet can be selected to drop or trap to CPU for further processing.

7.13. Layer 3 Routing

7.13.1. Unicast Routing

The device provides 1K L3 interface (shared with Tunnel interface), 12K hash-based (SRAM) L3 entries and 12K LPM-based (TCAM) L3 entries which can support 24K IPv4 unicast entries or 4K IPv6 unicast entries as maximum.

The device also provides 256 VRF (Virtual Routing and Forwarding) instances.

The device supports uRPF (unicast reverse path forwarding) check, ECMP (256 groups, each group can have maximum 8 different nexthops and traffic metering for each path), ICMP redirect, MTU check.

7.13.2. Multicast Routing

The device supports IPv4/IPv6 multicast routing, and provides maximum 6K IPv4/2K IPv6 multicast entries (which are shared with hash-based L3 unicast routing table).

The system supports (S, G) and (*, G) types of L3 IP multicast group, and packet replication which is able to process 16K (group * interface) multicast routed streams.

7.14. Tunnel

The device supports configured IP-in-IP (including IPv4-in-IPv4, IPv4-in-IPv6, IPv6-in-IPv4 and IPv6-in-IPv6) and GRE (IPv4/IPv6 + GRE + IPv4/IPv6) tunnels. Also supports ISATAP, 6to4 and 6RD auto tunnels. The system totally supports maximum 384 tunnels for configured/auto tunnels.

7.15. PIE (Packet Inspection Engine)

PIE is a 4K-entry search engine which is divided into 32 blocks. Each block contains 128 entries. Each block can be configured as VLAN, Ingress or Egress ACL. Each block can be assigned a group ID for block grouping. The block with lower group ID has higher priority. In addition to group ID, logic ID can also be assigned to block to prioritize blocks of the same block group.

7.15.1. VLAN ACL

The VLAN ACL function supports packet color-dependent drop, drop/permit/redirect/copy to CPU, log, mirror, policing, ingress inner VLAN assignment, ingress outer VLAN assignment, priority assignment, bypass, meta-data assignment and QoS remarking functionalities. When a PIE memory block is configured to VLAN ACL, it will execute the corresponding actions when a packet hits the entry.

Each VLAN ACL entry corresponds to multiple actions. When a multi-match occurs (i.e., there are several ACL entries matching concurrently), these matched actions will be divided into different action groups. Each group will then execute the lowest block logic ID of lowest block group ID address entry corresponding action.

7.15.2. Ingress ACL

The ingress ACL function supports packet color-dependent drop, drop/permit/redirect/copy to CPU, log, mirror, policing, egress inner VLAN assignment, egress outer VLAN assignment, priority assignment and QoS remarking functionalities. When a PIE memory block is configured to ingress ACL, it will execute the corresponding actions when a packet hits the entry.

Each ingress ACL entry corresponds to multiple actions. When a multi-match occurs (i.e., there are several ACL entries matching concurrently), these matched actions will be divided into different action groups. Each group will then execute the lowest block logic ID of lowest block group ID entry corresponding action.

7.15.3. Egress ACL

The egress ACL function supports packet color-dependent drop, log, policing, egress inner VLAN assignment, egress outer VLAN assignment, and QoS remarking functionalities. When a PIE memory block is configured to egress ACL, it will execute the corresponding actions when a packet hits the entry.

Each egress ACL entry corresponds to multiple actions. When a multi-match occurs (i.e., there are several ACL entries matching concurrently), these matched actions will be divided into different action groups. Each group will then execute the lowest block logic ID of lowest block group ID entry corresponding action.

7.15.4. Log Counter

The device supports per ACL entry a 42-bit byte counter and a 36-bit packet counter. Counters belong to different block groups can be increased concurrently when multiple matching.

7.16. OPENFLOW

In addition to normal pipeline, the device embeds an OpenFlow engine which complies with OpenFlow v.1.5.1. For cost saving and power reduction, the OpenFlow engine leverages the same physical hardware resources and configurations with ACL function. A packet can be forwarded to either normal or OpenFlow pipeline based on Classifier result to support OpenFlow hybrid switch.

The OpenFlow engine comprises four ingress flow tables and one egress flow table. Ingress Flow Table 0~3 and Egress Flow Table 0 leverages the hardware resource with VLAN ACL, L2 Table, L3 Table, Ingress ACL and Egress ACL, respectively.

Besides multiple flow tables, Meter table and Group table are also supported. Each meter entry supports dual meter bands which can have different rate and burst configurations. Drop and DSCP Remark band types are supported when the traffic rate is over. Group entry supports group type: Indirect/All/Select. Each group entry can contain up to 128 action buckets for multicast replication.

7.17. Traffic Suppression

The priority sequence for traffic suppression is: Ingress bandwidth control → ACL policing → Storm control → Egress bandwidth control

7.17.1. Ingress Bandwidth Control

The device supports ingress bandwidth control configuration for each port. The bandwidth setting ranges from 16Kbps and up to the port speed. The granularity is 16Kbps. The port acts as blocking while the rate is configured as 0. If the receiving packet rate is over the bandwidth setting, the device can optionally send a 'Pause ON' packet to slow down the transmission of link partner. For out of profile detection, per port supports a EXCEED flag to indicate whether the traffic rate ever over the bandwidth setting. To make sure the control packet has higher priority, the device has capability to bypass ingress bandwidth control for ARP/RMA/IGMP/RIP/OSPF/DHCP.

7.17.2. ACL Policing

The device supports 512 policers. Policers belong to different block groups can be executed concurrently to support hierarchy policing. The policer is flow controlled via leaky bucket. The rate ranges from 16Kbps~10Gbps with 16Kbps granularity and each policer entry has a 20-bit register to control the rate value.

Each ACL entry has an index to point to 512 ACL policers. One limitation is that different phase ACL or different block group cannot share the same policer.

7.17.3. Storm Control

The per-port L2 storm filtering control mechanism suppresses the flow rate of storm packets. The device supports five control types: Unknown Unicast, Unicast, Unknown Multicast, Multicast, and Broadcast Storm. The definitions of five traffic types are:

- Unknown Unicast: If the I/G bit of DMAC address (DMAC[40]) is 0, it is an unicast packet. The failure in L2 unicast table DA look-up is what called "Unknown Unicast".
- Unicast: If the I/G bit of DMAC address (DMAC[40]) is 0, it is an unicast packet.
- Unknown Multicast: If the I/G bit of DMAC address (DMAC[40]) is 1, it is a multicast packet. The failure in L2 multicast table DA look-up is what called 'Unknown Multicast'.
- Multicast: The success of L2 multicast table DA look-up for a multicast packet is called the 'Known Multicast'. System's Multicast Storm Filtering Control includes Unknown and Known Multicast.

- Broadcast: DMAC = FF-FF-FF-FF-FF-FF is called the ‘Broadcast packet’.

The traffic rate for these five types can be set on a per-port basis and per port per control type supports a EXCEED flag to indicate whether the traffic rate ever overran. PPS (Packet-Per-Second) or BPS (Bit-Per-Second) counting mode can be selected system-wise.

7.17.4. Egress Bandwidth Control

Egress bandwidth control configurations are supported to each port and each egress queue. Per-queue is also provided assured bandwidth and maximum bandwidth. Each bandwidth setting ranges from 16Kbps~10Gbps. The granularity is 16Kbps, and each port has a 20-bit register to control the bandwidth.

7.18. Priority Decision

There are eleven types of priority decision source for the device:

- VLAN ACL
- Routing
- MAC-based/IP-subnet-based VLAN
- Protocol-and-port-based VLAN
- DSCP
- Outer Tag
- Inner Tag
- 802.1BR
- Tunnel
- MPLS
- Port

For each receiving packet it will be given an internal priority, and the packet is then en-queued to the output queue according to its internal priority. The internal priority is from one of the twelve priority source. Each priority source has a weight configuration; the priority source with larger weight is taken as the internal priority. If all of priority source weights are the same, system follows the sequence as above to decide the internal priority (VLAN ACL and Port are highest priority and lowest priority respectively).

7.19. Packet Scheduling

The Packet Scheduler controls the multiple traffic classes (i.e., controls the packet sending sequence of the priority queue). The device scheduling algorithm is divided into Weighted Fair-Queuing (WFQ) and Weighted Round-Robin (WRR). Note that the Strict Priority queue is the highest priority of all queues, and overrides WFQ & WRR. A larger strict priority queue ID indicates the priority is higher.

The Scheduler operates as follows:

- Weighted Fair-Queuing (WFQ): Byte-count
- Weighted Round-Robin (WRR): Packet-count

WFQ and WRR cannot exist at the same time. Both WFQ and WRR are round robin, from large queue ID to small.

7.20. Egress Packet Remarking

Remarking can be divided into Inner 1p, Outer 1p, DEI and DSCP Remarking. Per egress port per type supports a configuration to turn on the remarking function. For Inner 1p Remarking and Outer 1p Remarking, the remarking source can be internal priority, original inner 1p priority, original outer 1p priority or original DSCP value. For DEI Remarking, the remarking source can be either from internal priority or internal drop precedence (DP). For DSCP Remarking, the remarking source can be internal priority, original inner 1p priority, original outer 1p priority, original DSCP value, internal DP and internal-priority-and-internal-DP.

7.21. Buffer Management

7.21.1. IEEE 802.3x Flow Control

The device supports IEEE 802.3x full duplex flow control. If the packet buffer used by a port is over the pause threshold, a pause-on frame is sent to indicate to the link partner to stop the transmission. When the frame buffer used by a port drops below the pause threshold, it sends a pause-off frame. The Tx pause frame format is shown in below.

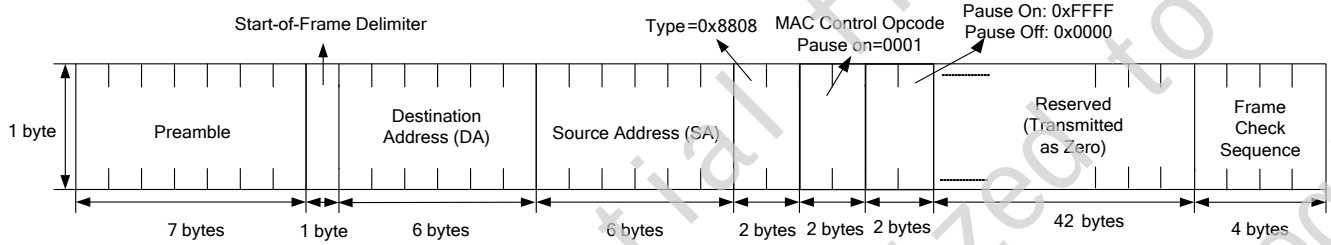


Figure 8. Tx Pause Frame Format

The flow control mechanism of the device is implemented on the Ingress side. It counts the received pages on the Ingress side in order to determine on which port it should send out pause on/off packets. Figure 9 shows the flow control state machine.

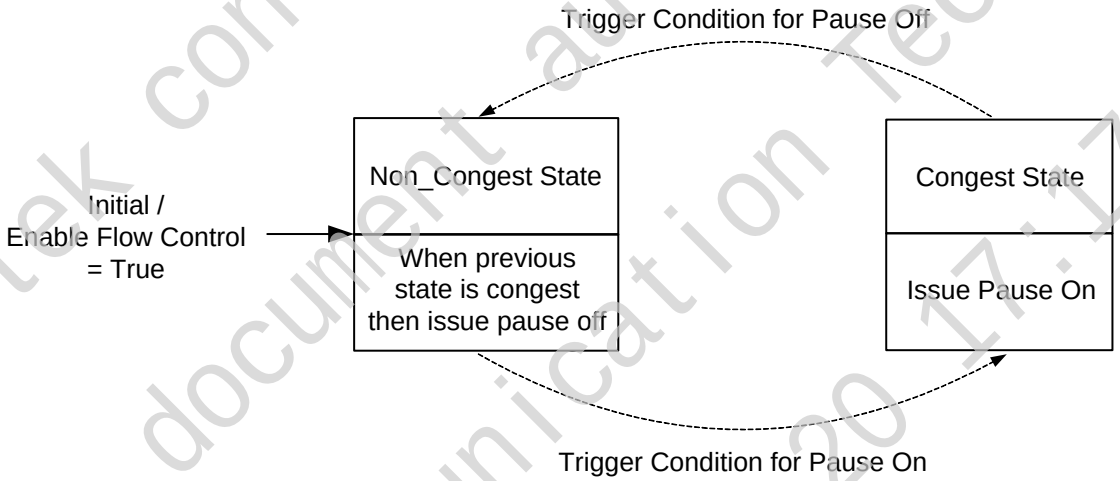


Figure 9. Flow Control State Machine

The first flow control state is 'Non_Congest'. This is continuously monitored for the pause-on trigger condition, at which point it enters the 'Congest' state. In the congest state, it is continuously monitored for the pause-off trigger condition, at which point it re-enters the 'Non_Congest' state.

7.21.2. Half Duplex Backpressure

There are two mechanisms for half duplex backpressure (Backpressure is for input buffer overflow).

7.21.2.1 Collision-Based Backpressure (Jam Mode)

If the input buffer used by a ingress port over the configured threshold, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- When the link partner detects the collision, it waits for a random backoff time. The device will handle packets that are in the input packet buffer during this time.
- RXDV and TXEN will be driven to high. The device will send a 4-byte Jam signal (pattern is 0xAA). Then the device will drive TXEN to low.
- When the link partner receives the Jam signal, it will feedback a 4-byte signal.
- The link partner waits for a random backoff time then re-sends the packet.

7.21.2.2 Carrier-Based Backpressure (Defer Mode)

If the packet buffer used by an ingress port over the configured threshold, this mechanism will send a 2k-bytes defer signal (pattern is 0x55) to defer the other station's transmission. The device will continuously send the defer signal until the packet buffer usage is under the threshold.

7.21.3. SWRED (Simple Weighted Random Early Detection)

When SWRED is not configured, output buffers fill during periods of congestion. When the buffers are full, tail drop occurs; all additional packets are dropped. Since the packets are dropped all at once, global synchronization of TCP hosts can occur as multiple TCP hosts reduce their transmission rates. The congestion clears, and the TCP hosts increase their transmissions rates, resulting in waves of congestion followed by periods where the transmission link is not fully used.

SWRED reduces the chances of tail drop by selectively dropping packets when the output interface begins to show signs of congestion. By dropping some packets early rather than waiting until the buffer is full, SWRED avoids dropping large numbers of packets at once and minimizes the chances of global synchronization. Thus, SWRED allows the transmission line to be used fully at all times.

The device SWRED provides separate thresholds and weights for different drop precedence (0: Green, 1: Yellow, 2: Red), allowing you to provide different qualities of service for different traffic. It simplifies the calculation of packet marking probability as shown in Figure 10.

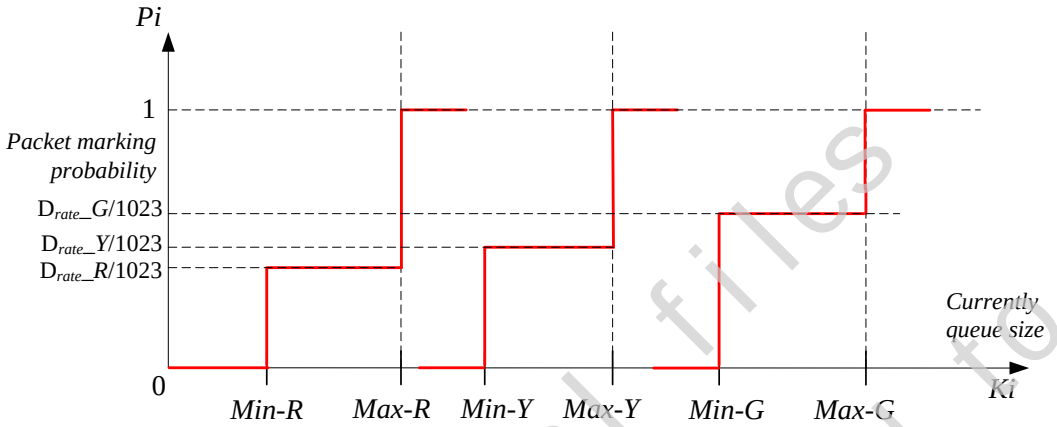


Figure 10. SWRED Packet Marking Probability of Different Drop Precedence

7.22. srTCM/trTCM (Single/Two Rate Three Color Marker)

The device supports 512 ACL policers which can also be used as color-aware/color-blind srTCM (Single Rate Three Color Marker) and color-aware/color-blind trTCM (Two Rate Three Color Marker).

The srTCM meters a traffic stream and marks its packets according to three traffic parameters, Committed Information Rate (CIR), Committed Burst Size (CBS), and Excess Burst Size (EBS), to Green, Yellow, or Red.

The trTCM meters a traffic stream and marks its packets based on two rates, Peak Information Rate (PIR) and Committed Information Rate (CIR), and their associated burst sizes to be green, yellow, or red.

Each policer can specify the counting mode to be either PPS (Packet-Per-Second) or BPS (Bit-Per-Second).

The packet is marked a color by srTCM/trTCM and the color is then referenced by associated ACL entry to perform drop or remark action. The color of packet is also referenced by SWRED to perform egress random dropping for congestion avoidance.

7.23. 802.1BR Bridge Port Extension

BPE (Bridge Port Extension) provides the capability to extend MAC service over an Extended Bridge. This capability may be used to extend a bridge over multiple physical devices or the mac service of a virtual end station. The data center topology experiences a dramatic increase number of Ethernet switches. BPE simplifies the complexity of vSwitch and the loading of hypervisor.

Compared to the traditional stacking which has the higher cost of maintenance, BPE reduces the cost by Extended Bridge.

Each port on the device could be configured as (CB) Controlling Bridge or (PE) Port Extender. The traffic is forwarded via E-channel through the identification of ETAG. According to the E-CID (E-channel ID) in the ETAG, the traffic could be classified as point-to-point (unicast) or point-to-multipoint

(multicast). E-CID and NSG (Namespace Group) are used for DA lookup while the port is configured as PE mode.

7.24. Management Information Base (MIB)

The supported MIB (Management Information Base) counters include:

- TCP/IP-based MIB-II (RFC 1213)
- Ethernet-like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (Remote Network Monitoring) MIB (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

7.25. NIC and CPU Tag Forwarding

The NIC interface is used for receiving packets from the CPU, or transmitting packets to the CPU. The architecture is shown in below.

When a packet is sent from the switch core to the CPU port, the CPU tag can carry status information. The CPU tag can be divided into a transmit CPU tag, and a receive CPU tag. The transmit CPU Tag can force the egress port mask. The receive CPU Tag indicates the ingress port the packet came from and the reason why it was sent to the CPU. If no transmit CPU tag is attached, normal L2 table lookup is taken to forward the packet.

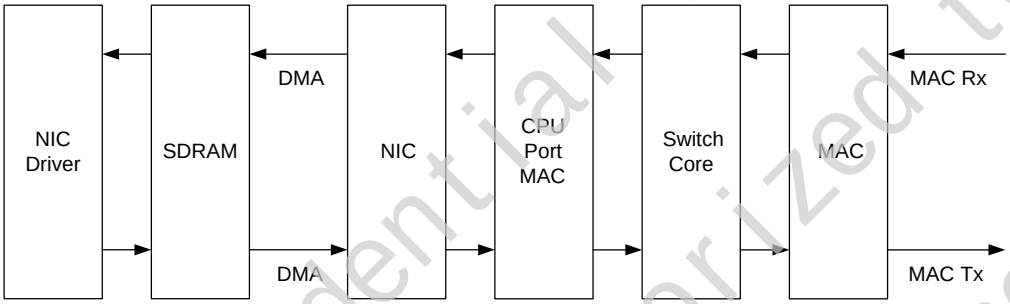


Figure 11. NIC Architecture

7.26. Table Access

The device employs an indirect method to set the control register and the data register to complete SRAM Table Access:

1. Set the register to determine which table and which entry is to be accessed.
2. Determine the read or write operation.
3. Hardware executes table access.

Read: After the control register setup has been completed by software, hardware starts accessing and retrieves the data into the data register. Software then reads this data from the data register.

Write: Software puts the data in the data register and indicates the write operation in the control register. Then hardware writes the data from the data register to the table.

7.27. External PHY Register Access

The device supports PHY access control registers to indirectly access an external PHY via the MDC/MDIO interface.

7.28. OAM (Operation, Administration, Maintenance)

7.28.1. 802.3ah OAM

IEEE 802.3ah OAM provides mechanisms useful for monitoring link operation such as remote fault indication and remote loopback control. In general, OAM provides network operators the ability to monitor the health of the network and quickly determine the location of failing links or fault conditions.

The OAM loopback function supported by the device is wire-speed guaranteed and the source/destination MAC address can be swapped for the loopback packet.

The device also supports Y.1731 ETH-DM (Ethernet Delay Measurement) to measure frame delay and frame delay variation between peers.

7.28.2. 802.1ag CFM

CFM (Connectivity Fault Management) specifies protocols and protocol entities within the architecture of VLAN-aware Bridges that provide capabilities for detecting, verifying, and isolating connectivity failures in Virtual Bridged Local Area Networks. CFM describes the protocols and procedures used by Maintenance Points to detect and diagnose connectivity faults within a MD (Maintenance Domain).

CFM provides three protocols in order to achieve end-to-end connectivity fault management.

1. Continuity Check Protocol
2. Loopback Protocol
3. Linktrace Protocol

The device could identify CFM packet and process these packets according to the configuration of each MD Level (0~7).

To off load the CPU intensive, CCM (Continuity Check Message) packets are generated and transmitted by the hardware.

7.29. EEE

EEE proposes a low power idle (LPI) mode where the MAC and PHY can shut down parts of electric circuits to reduce power consumption. If there is no traffic to be transmitted, the TX part of a port can enter LPI mode to sleep. If the link partner enters TX LPI mode, the connected port can enter RX LPI mode.

The device per port can enable the TX/RX EEE function separately for different link speed (excludes 10Mbps).

8. CPU Sub-system Function Description

8.1. CPU Core

- MIPS InterAptive, Dual Core up to 1GHz
- 32KB I-Cache
- 32KB D-Cache
- 256KB L2 Cache

8.2. SPI NOR Flash Controller

The device supports serial/dual/quad SPI Flash access with the specification below.

- Up to 100MHz in serial SPI Flash
- Two chip select with up to 32MB (3-byte mode), 64MB (4-byte mode)
- Programmed I/O interface and memory-mapped I/O interface for read operation is supported
- Cached read access

8.3. SPI NAND Flash Controller

- Up to 100MHz in serial SPI Flash
- up to total 512MB address space
- 2 * Chip Select supported

8.4. DDR Memory Controller

DDR3/DDR4 are supported with the specification below.

- DDR3/DDR4, up to total 2GB address space
- 16/32-bit, up to 800MHz
- 2 * 16-bit Chip supported, combined as 32-bit

9. Electrical AC/DC Characteristics

9.1. Operating Range

Table 16. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Junction Temperature (Tj)	-	-	115	°C
SVDDH_CKO, SVDDH, AVDDH_BG, AVDDH_XTAL, AVDDH_PLL, USB_VDDH, MVDDH, DVDDH Supply Voltage Range	3.135	3.3	3.465	V
SVDDTRX, SVDD_CMU, SVDD_RGCMU, SVDDCK, AVDDL_BG, AVDDL_XTAL, AVDDL_PLL, PCIE_VDDL, USB_VDDL, DVDDL, DVDDL_CPU, Supply Voltage Range	0.855	0.9	0.945	V
MVDD Supply Voltage Range (for DDR3)	1.425	1.5	1.575	V
Storage Temperature	-10	-	+125	°C

9.2. DC Characteristics

Table 17. DC Characteristics for 24G+4*10G with 16-bit DDR at Tj=115°C

Symbol	Parameter	Min	Typical	Max	Units
I_{VDDL}	Power Supply Current for all Low Voltage Power (0.9V)	-	TBD	-	A
I_{VDDH}	Power Supply Current for all High Voltage Power (3.3V)	-	TBD	-	A
I_{MVDD}	Power Supply Current for DDR Controller Low Voltage Power (1.5V)	-	TBD	-	A
PS	Total Power Consumption for All Ports	-	TBD	-	W

Note: Recommend to add 20% tolerance for power solution.

Table 18. DC Characteristics (DVDDH=3.3V)

Symbol	Parameter	Min	Typical	Max	Units
V_{IH}	Input-High Voltage	2.0	-	-	V
V_{IL}	Input-Low Voltage	-	-	0.8	V
V_{OH}	Output-High Voltage	2.4	-	-	V
V_{OL}	Output-Low Voltage	-	-	0.4	V

9.3. AC Characteristics

9.3.1. Clock Characteristics

Table 19. XTALI (XI) Characteristics

Parameter	Min	Typical	Max	Units
Frequency of XTALI	-	25	-	MHz
Frequency Tolerance of XTALI	-50	-	+50	ppm
Duty Cycle of XTALI	40	-	60	%
Rise Time of XTALI	-	-	12.5	ns

Parameter	Min	Typical	Max	Units
Fall Time of XTALI	-	-	12.5	ns
Jitter of XTALI	-	-	200	ps

9.3.2. 1.25G Serdes Differential Transmitter Characteristics

Table 20. 1.25G Serdes Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI UI	Unit Interval 1000Base-X/SGMII 100Base-FX	799.76 7.9976	800 8.0	800.24 8.0024	ps ns	
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	800	1300	mV	
T_TJ	Output Total Jitter			0.375	UI	

9.3.3. 1.25G Serdes Differential Receiver Characteristics

Table 21. 1.25G Serdes Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI UI	Unit Interval 1000Base-X/SGMII 100Base-FX	799.76 7.9976	800 8.0	800.24 8.0024	ps ns	
$V_{RX-DIFFp-p}$	Input Differential Voltage	300	-	2000	mV	
R_{RX}	Differential Resistance		100		ohm	

9.3.4. XSGMII Differential Transmitter Characteristics

Table 22. XSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval		97		ps	
Vdiff	Differential Output Voltage	400		900	mV	
TJ	Total Jitter			0.28	Uipp	
	Transmitter output impedance on chip		100		ohm	

9.3.5. XSGMII Differential Receiver Characteristics

Table 23. XSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval		97		ps	
Vdiff	Differential Input Voltage Swing	200		950	mV	
	Receiver input impedance on chip		100		ohm	

9.3.6. 10GBase-R Differential Transmitter Characteristics

Table 24. 10GBase-R Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval		97		ps	
Vdiff	Differential Output Voltage	400		900	mV	
TJ	Total Jitter			0.28	Uipp	
	Transmitter output impedance on chip		100		ohm	

9.3.7. 10GBase-R Differential Receiver Characteristics

Table 25. 10GBase-R Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval		97		ps	
Vdiff	Differential Input Voltage Swing	200		950	mV	
	Receiver input impedance on chip		100		ohm	

9.3.8. DDR3 Characteristics

The RLT9311R DDR3 Interface fully meets the timing requirements defined in “DDR3 SDRAM Specification JESD79-3F” (Reference Contents [13] on page 167)

9.3.9. DDR4 Characteristics

The RLT9311R DDR4 Interface fully meets the timing requirements defined in “DDR4 SDRAM Specification JESD79-4B” (Reference Contents [13] on page 226)

9.3.10. SPI Flash Controller Interface Characteristics

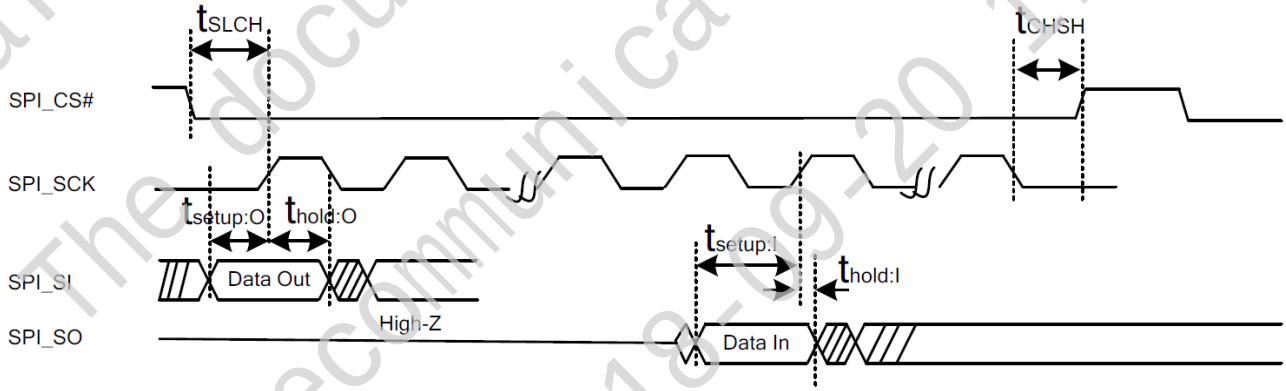


Figure 12. SPI Flash Controller Interface Timing

Table 26. SPI Flash Controller Interface Timing Characteristics

Symbol	Parameter	I/O	Min	Typical	Max	Units	Note
T_{CYC}	CLK Output Cycle Time	O	-	38.8	-	ns	
T_{DUTY}	Duty Cycle of CLK	O	-	50	-	%	
t_{SLCH}	CS# Active Setup Time	O	-	45	-	ns	
t_{CHSH}	CS# Active Hold Time	O	-	25	-	ns	
$T_{setup:O}$	Data Output setup time	O	-	15	-	ns	
$T_{hold:O}$	Data Output hold time	O	-	23	-	ns	
$T_{setup:I}$	Data Input setup time	I	2.33	-	-	ns	
$T_{hold:I}$	Data Input hold time	I	1	-	-	ns	

9.3.11. EJTAG Timing Characteristics

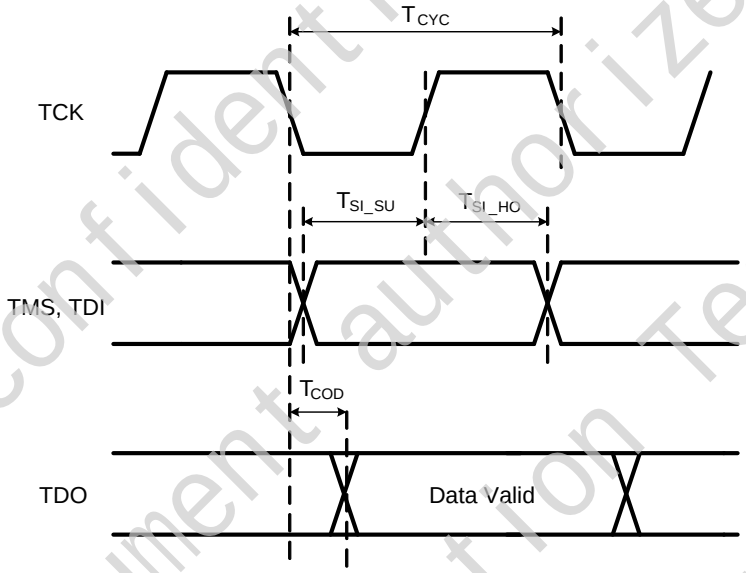


Figure 13. EJTAG Timing

Table 27. EJTAG Interface Timing Characteristics

Symbol	Parameter	I/O	Min	Typical	Max	Units
T_{CYC}	CLK Input Cycle Time	I	30	-	-	ns
T_{SI_SU}	TMS and TDI Setup Times	I	1.86	-	-	ns
T_{SI_HO}	TMS and TDI Hold Times	I	1	-	-	ns
T_{COD}	TDO Output Delay	O	-	12	-	ns

9.3.12. SMI (MDC/MDIO) Interface Characteristics

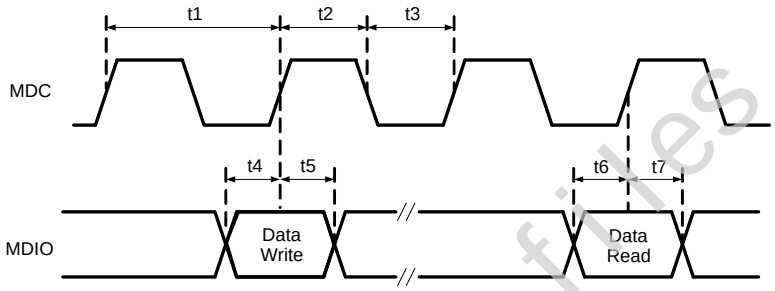


Figure 14. SMI (MDC/MDIO) Timing

Table 28. SMI (MDC/MDIO) Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
t1	MDC Clock Period	-	400	-	ns
t2	MDC High Time	-	200	-	ns
t3	MDC Low Time	-	200	-	ns
t4	MDIO to MDC Rising Setup Time (Write Data)	-	200	-	ns
t5	MDIO to MDC Rising Hold Time (Write Data)	-	200	-	ns
t6	MDIO to MDC Rising Setup Time (Read Data)	40	-	-	ns
t7	MDIO to MDC rising hold time (Read Data)	2	-	-	ns

9.3.13. LED Timing Characteristics

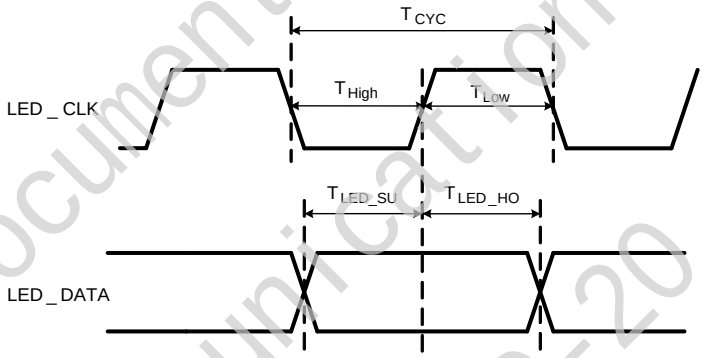


Figure 15. LED Timing

Table 29. Serial LED Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
T_{CYC}	LED Clock Period	O	-	200	-	ns
T_{High}	LED High Time	O	-	100	-	ns
T_{Low}	LED Low Time	O	-	100	-	ns
T_{OSU}	LED_DATA to LED_CLK Rising Setup Time	O	-	100	-	ns
T_{OH}	LED_DATA to LED_CLK Rising Hold Time	O	-	100	-	ns

Table 30. Scan Bi-Color LED Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
T_{CYC}	LED Clock Period	O	-	400	-	ns
T_{High}	LED High Time	O	-	200	-	ns
T_{Low}	LED Low Time	O	-	200	-	ns
T_{OSU}	LED_DATA to LED_CLK Rising Setup Time	O	-	200	-	ns
T_{OH}	LED_DATA to LED_CLK Rising Hold Time	O	-	200	-	ns

Table 31. Scan Single-Color LED Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
T_{CYC}	LED Clock Period	O	-	400	-	ns
T_{High}	LED High Time	O	-	200	-	ns
T_{Low}	LED Low Time	O	-	200	-	ns
T_{OSU}	LED_DATA to LED_CLK Rising Setup Time	O	-	200	-	ns
T_{OH}	LED_DATA to LED_CLK Rising Hold Time	O	-	200	-	ns

9.3.14. SPI Master Timing Characteristics

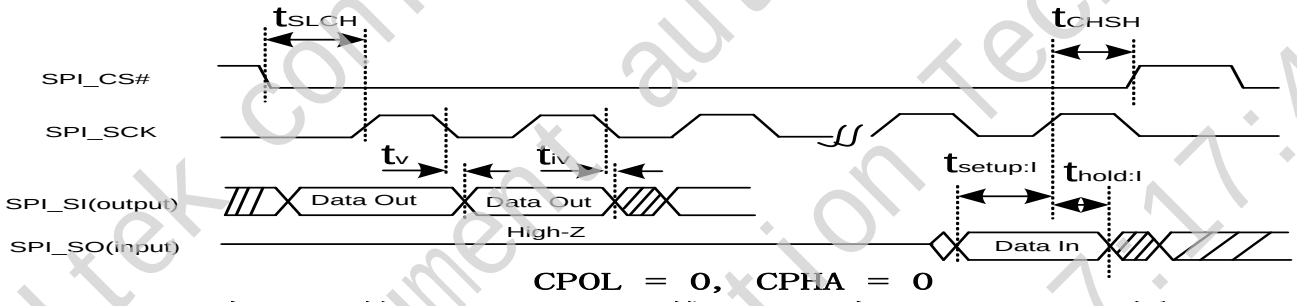


Figure 16. SPI Master Timing

Table 32. SPI Master Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
T	Clock period of the SPI_SCK	-	32	-	ns
Duty	Duty Cycle of the SPI_SCK	-	50	-	%
t_{SLCH}	CS# Active Setup Time	32	-	-	ns
t_{CHSH}	CS# Active Hold Time	32	-	-	ns
t_v	Data Output valid Time	-	-	4	ns
t_{iv}	Data Output invalid Time	-1.5	-	-	ns
$t_{setup:I}$	Data Input Setup Time	7	-	-	ns
$t_{hold:I}$	Data Input Hold Time	0	-	-	ns

9.3.15. EEPROM SMI Master Timing Characteristics

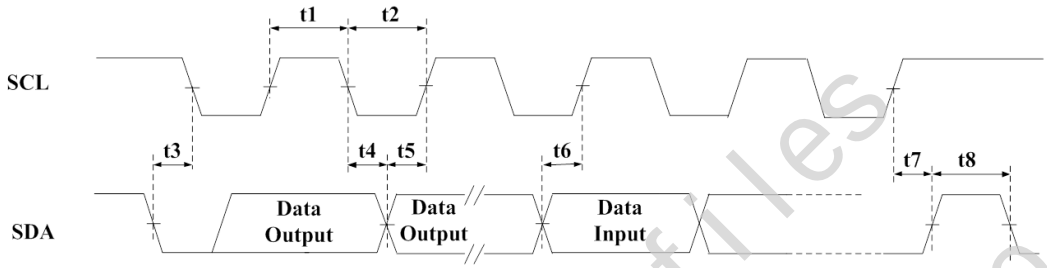


Figure 17. EEPROM SMI Master Timing

Table 33. EEPROM SMI Master Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
T	SCL period		20		us
t1	SCL high time		10		us
t2	SCL low time		10		us
t3	START condition hold time		9.9		us
t4	Data hold time		100		ns
t5	Data setup time		9.9		us
t6	Input Date setup time	0.007			us
t7	STOP condition setup time		10		us
t8	Bus free time between STOP and START	10			us

9.3.16. Power and Reset Characteristics

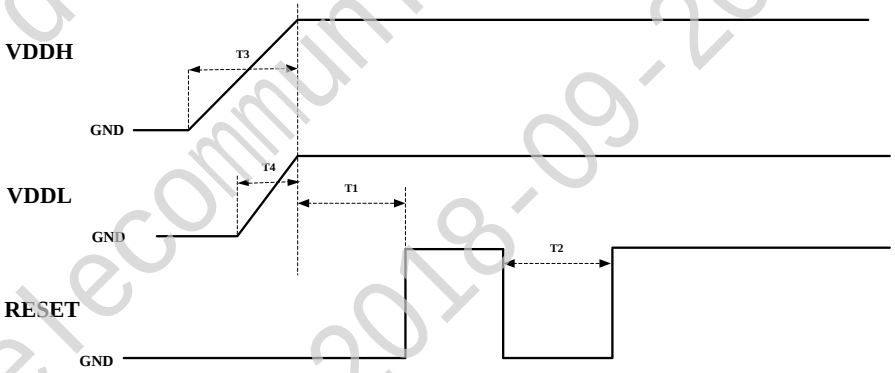


Figure 18. Power and Reset Timing

Table 34. Power and Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all of High Power and all of Low Power steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms
T3	All of High Power rising time	1	-	30	ms
T4	All of Low Power rising time	0.5	-	30	ms

10. Thermal Characteristics

10.1. Assembly Descriptions

Table 35. Assembly Descriptions

Package	Type	HFCBGA
	Ball counts	673
	Size	27 x 27 mm^2
Customized PCB	PCB dimensions	430 x 235 mm^2
	PCB thickness	1.6 mm
	Number of Layer-PCB	4-Layer
Heat Sink	Size	60 x 60 x 30 mm^3

10.2. Thermal Data

Table 36. Thermal Data

PCB Type	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W)
Customized 4L-PCB (with heat sink)	1.1	-	-	-
JEDEC 4L (without heat sink)	-	9.07	0.89	2.98
JEDEC 4L (with heat sink)	-	4.56	-	-

Note:

Ψ_{JT}: Junction-to-top-center thermal characterization parameter

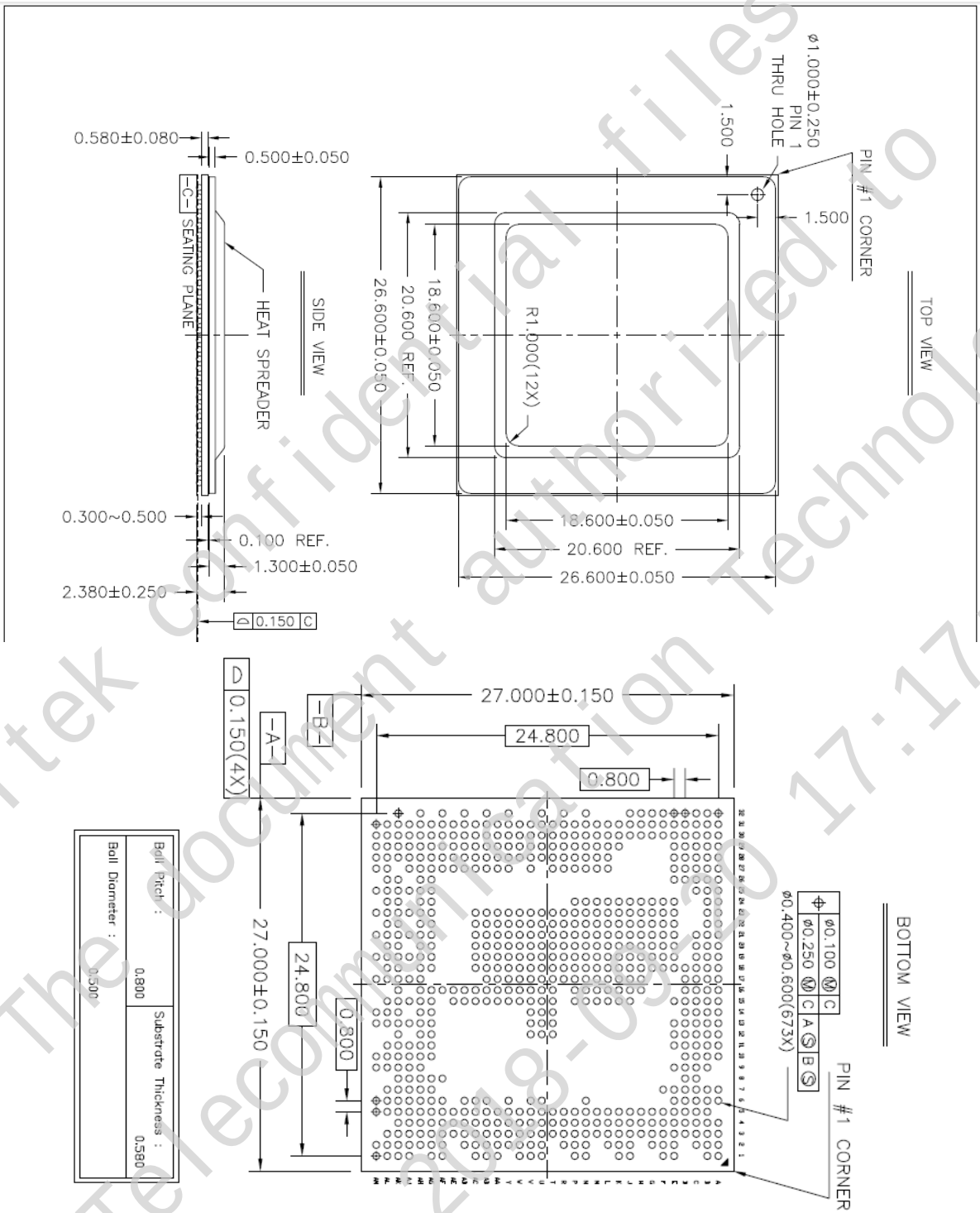
θ_{JC}: Junction-to-case thermal resistance

θ_{JB}: Junction-to-board thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

11. Package Information

*11.1. HFC FBGA673 (27*27)*



12. Ordering Information

Table 37. Ordering Information

Part Number	Package	Status
RTL9311R-CG	HFC FBGA673 (27mm*27mm)	

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