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SINGLE-CHIP 10/100/1000M SWITCH CONTROLLER

RTL8367RB/RTL8367MB
REGISTER TABLE

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek Gigabit Switch chip.

Though every effort has been made to ensure that this document is current and accurate， more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0.0	2010/12/10	First release

1. VLAN

1.1. Enable VLAN table Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x07a8	[0]	EN_VLAN	VLAN usage. 0b0:Disable 0b1:Enable	R/W	0x0
	[15:1]	RESERVED	Reserved		

1.2. VLAN Configuration Register

Address	Bit(s)	Name	Description	R/W	Default
0x0728	[7:0]	Member	VLAN member set of VLAN index 0.	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0729	[3:0]	FID/MSTI	FID/MSTI of VLAN index 0.	R/W	0x0
	[15:12]	RESERVED	Reserved	R/W	0x0
0x072a	[0]	VBPEN	VLAN based priority decision source of VLAN member configuration index 0 0b0:disable 0b1:enable	R/W	0x0
	[3:1]	VBPRI	VLAN based priority of VLAN member configuration index 0	R/W	0x0
	[4]	ENVLANPOL	VLAN based policing of VLAN member configuration index 0 0b0:disable 0b1:enable	R/W	
	[9:5]	METERIDX	Policing share meter index of VLAN member configuration index 0	R/W	
	[15:10]	RESERVED	Reserved		
0x072b	[12:0]	EVID	Enhanced VID of VLAN index 0.	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x072c~ 0x072f			VLAN member configuration index 1, the register definition is the same as index 0.	R/W	0
0x0730~ 0x0733			VLAN member configuration index 2, the register definition is the same as index 0.	R/W	0
0x0734~ 0x0737			VLAN member configuration index 3, the register definition is the same as index 0.	R/W	0
0x0738~ 0x073b			VLAN member configuration index 4, the register definition is the same as index 0.	R/W	0
0x073c~ 0x073f			VLAN member configuration index 5, the register definition is the same as index 0.	R/W	0
0x0740~ 0x0743			VLAN member configuration index 6, the register definition is the same as index 0.	R/W	0
0x0744~ 0x0747			VLAN member configuration index 7, the register definition is the same as index 0.	R/W	0

Address	Bit(s)	Name	Description	R/W	Default
0x0748~ 0x074b			VLAN member configuration index 8, the register definition is the same as index 0.	R/W	0
0x074c~ 0x074f			VLAN member configuration index 9, the register definition is the same as index 0.	R/W	0
0x0750~ 0x0753			VLAN member configuration index 10, the register definition is the same as index 0.	R/W	0
0x0754~ 0x0757			VLAN member configuration index 11, the register definition is the same as index 0.	R/W	0
0x0758~ 0x075b			VLAN member configuration index 12, the register definition is the same as index 0.	R/W	0
0x075c~ 0x075f			VLAN member configuration index 13, the register definition is the same as index 0.	R/W	0
0x0760~ 0x0763			VLAN member configuration index 14, the register definition is the same as index 0.	R/W	0
0x0764~ 0x0767			VLAN member configuration index 15, the register definition is the same as index 0.	R/W	0
0x0768~ 0x076b			VLAN member configuration index 16, the register definition is the same as index 0.	R/W	0
0x076c~ 0x076f			VLAN member configuration index 17, the register definition is the same as index 0.	R/W	0
0x0770~ 0x0773			VLAN member configuration index 18, the register definition is the same as index 0.	R/W	0
0x0774~ 0x0777			VLAN member configuration index 19, the register definition is the same as index 0.	R/W	0
0x0778~ 0x077b			VLAN member configuration index 20, the register definition is the same as index 0.	R/W	0
0x077c~ 0x077f			VLAN member configuration index 21, the register definition is the same as index 0.	R/W	0
0x0780~ 0x0783			VLAN member configuration index 22, the register definition is the same as index 0.	R/W	0
0x0784~ 0x0787			VLAN member configuration index 23, the register definition is the same as index 0.	R/W	0
0x0788~ 0x078b			VLAN member configuration index 24, the register definition is the same as index 0.	R/W	0
0x078c~ 0x078f			VLAN member configuration index 25, the register definition is the same as index 0.	R/W	0
0x0790~ 0x0793			VLAN member configuration index 26, the register definition is the same as index 0.	R/W	0
0x0794~ 0x0797			VLAN member configuration index 27, the register definition is the same as index 0.	R/W	0
0x0798~ 0x079b			VLAN member configuration index 28, the register definition is the same as index 0.	R/W	0
0x079c~ 0x079f			VLAN member configuration index 29, the register definition is the same as index 0.	R/W	0
0x07a0~ 0x07a3			VLAN member configuration index 30, the register definition is the same as index 0.	R/W	0
0x07a4~ 0x07a7			VLAN member configuration index 31, the register definition is the same as index 0.	R/W	0

1.3. Port-based VLAN Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0700	[4:0]	PVID	Port based CVLAN index to CVLAN member configuration of port 0	R/W	0x0
	[7:5]	RESERVED	Reserved		
	[12:8]	PVID	Port based CVLAN index to CVLAN member configuration of port 1	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x0701	[4:0]	PVID	Port based CVLAN index to CVLAN member configuration of port 2	R/W	0x0
	[7:5]	RESERVED	Reserved		
	[12:8]	PVID	Port based CVLAN index to CVLAN member configuration of port 3	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x0702	[4:0]	PVID	Port based CVLAN index to CVLAN member configuration of port 4	R/W	0x0
	[7:5]	RESERVED	Reserved		
	[12:8]	PVID	Port based CVLAN index to CVLAN member configuration of port 5	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x0703	[4:0]	PVID	Port based CVLAN index to CVLAN member configuration of port 6	R/W	0x0
	[7:5]	RESERVED	Reserved		
	[12:8]	PVID	Port based CVLAN index to CVLAN member configuration of port 7	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x0851	[2:0]	PORT0_PRIORITY	VLAN 1Q Port based priority assignment for PORT 0	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT1_PRIORITY	VLAN 1Q Port based priority assignment for PORT 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT2_PRIORITY	VLAN 1Q Port based priority assignment for PORT 2	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT3_PRIORITY	VLAN 1Q Port based priority assignment for PORT 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x0852	[2:0]	PORT4_PRIORITY	VLAN 1Q Port based priority assignment for PORT 4	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT5_PRIORITY	VLAN 1Q Port based priority assignment for PORT 5	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT6_PRIORITY	VLAN 1Q Port based priority assignment for PORT 6	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT7_PRIORITY	VLAN 1Q Port based priority assignment for PORT 7	R/W	0x0
	[15]	RESERVED	Reserved		

1.4. Port-based VLAN FID Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x07ac	[7:0]	PORT_PBFIDEN	Per port forced Port-based FID setting 0b0:disable, FID will be decided from 4K VLAN table or 32 VLAN member configuration 0b1:enable, forced using PORTn_PBFID for packets received from Port n	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x07ad	[3:0]	PORT0_PBFID	Port Based FID for PORT 0	R/W	0x0
	[15:4]	RESERVED	Reserved		
0x07ae	[3:0]	PORT1_PBFID	Port Based FID for PORT 1	R/W	0x0
	[15:4]	RESERVED	Reserved		
0x07af	[3:0]	PORT2_PBFID	Port Based FID for PORT 2	R/W	0x0
	[15:4]	RESERVED	Reserved		
0x07b0	[3:0]	PORT3_PBFID	Port Based FID for PORT 3	R/W	0x0
	[15:4]	RESERVED	Reserved		
0x07b1	[3:0]	PORT4_PBFID	Port Based FID for PORT 4	R/W	0x0
	[15:4]	RESERVED	Reserved		
0x07b2	[3:0]	PORT5_PBFID	Port Based FID for PORT 5	R/W	0x0
	[15:4]	RESERVED	Reserved		
0x07b3	[3:0]	PORT6_PBFID	Port Based FID for PORT 6	R/W	0x0
	[15:4]	RESERVED	Reserved		
0x07b4	[3:0]	PORT7_PBFID	Port Based FID for PORT 7	R/W	0x0
	[15:4]	RESERVED	Reserved		

1.5. Per-port VLAN Ingress Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x07a9	[0]	ADMIT_SMBROL_P0	Port 0 VLAN ingress check for source member VLAN 0b0:Disable VLAN ingress 0b1:Enable VLAN ingress	R/W	0x0
	[1]	ADMIT_SMBROL_P1	Port 1 VLAN ingress check for source member VLAN	R/W	0x0
	[2]	ADMIT_SMBROL_P2	Port 2 VLAN ingress check for source member VLAN	R/W	0x0
	[3]	ADMIT_SMBROL_P3	Port 3 VLAN ingress check for source member VLAN	R/W	0x0
	[4]	ADMIT_SMBROL_P4	Port 4 VLAN ingress check for source member VLAN	R/W	0x0
	[5]	ADMIT_SMBROL_P5	Port 5 VLAN ingress check for source member VLAN	R/W	0x0
	[6]	ADMIT_SMBROL_P6	Port 6 VLAN ingress check for source member VLAN	R/W	0x0
	[7]	ADMIT_SMBROL_P7	Port 7 VLAN ingress check for source member VLAN	R/W	0x0
	[15:8]	RESERVED	Reserved		

0x7aa	[1:0]	ADMIT_UNTAGOL_P0	Port 0 802.1Q acceptable frame types setting 0b00: Accept all frame type, 0b01: Accept tagged only. 0b10: Accept untagged only	R/W	0x0
	[3:2]	ADMIT_UNTAGOL_P1	Port 1 802.1Q acceptable frame types setting	R/W	0x0
	[5:4]	ADMIT_UNTAGOL_P2	Port 2 802.1Q acceptable frame types setting	R/W	0x0
	[7:6]	ADMIT_UNTAGOL_P3	Port 3 802.1Q acceptable frame types setting	R/W	0x0
	[9:8]	ADMIT_UNTAGOL_P4	Port 4 802.1Q acceptable frame types setting	R/W	0x0
	[11:10]	ADMIT_UNTAGOL_P5	Port 5 802.1Q acceptable frame types setting	R/W	0x0
	[13:12]	ADMIT_UNTAGOL_P6	Port 6 802.1Q acceptable frame types setting	R/W	0x0
	[15:14]	ADMIT_UNTAGOL_P7	Port 7 802.1Q acceptable frame types setting	R/W	0x0

1.6. Per-port VLAN Egress Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x000e	[3:0]	RESERVED	Reserved	R/W	
	[5:4]	VLAN_PORT0_EGRESS_MODE	Per-portVLAN tag egress format 0b00: Original mode. Output frame will follow VLAN untag setting. 0b01: Keep format mode. Output frame will keep VLAN original format. 0b10: Priority tag mode. Output frame will be priority tag. 0b11: Real keep mode. Output frame will keep CVID and C-tag format	R/W	0x3
	[9:6]	RESERVED	Reserved		
	[10]	INGRESSBW_PORT0_IFG	Bandwidth Control Include/exclude Preamble & IFG (20bytes) 0: exclude, 1: include	R/W	0x0
	[11]	INGRESSBW_PORT0_FLOWCRTL	Flow control setting while input rate is over input bandwidth 0: disable, drop packet 1: enable flow control	R/W	0x1
	[15:12]	RESERVED	Reserved		
0x002e		P1MISC	Same as 0x000e		
0x004e		P2MISC	Same as 0x000e		
0x006e		P3MISC	Same as 0x000e		
0x008e		P4MISC	Same as 0x000e		
0x00ae		P5MISC	Same as 0x000e		
0x00ce		P6MISC	Same as 0x000e		
0x00ee		P7MISC	Same as 0x000e		

1.7. Protocol and Port VLAN Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0708	[7:0]	PPB0_VALID	Valid port mask for protocol-and-port-based item 0	R/W	0x0
	[15:0]	RESERVED	Reserved		

0x0709	[4:0]	PPB0_PORT0_INDEX	Port 0 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[9:5]	PPB0_PORT1_INDEX	Port 1 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[14:10]	PPB0_PORT2_INDEX	Port 2 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x070a	[4:0]	PPB0_PORT3_INDEX	Port 3 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[9:5]	PPB0_PORT4_INDEX	Port 4 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[14:10]	PPB0_PORT5_INDEX	Port 5 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x070b	[4:0]	PPB0_PORT6_INDEX	Port 6 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[9:5]	PPB0_PORT7_INDEX	Port 7 CVLAN index to CVLAN member configuration of protocol and port based item 0	R/W	0x0
	[11:10]	PPB0_FRAME_TYPE	Frame format of protocol and port based item 0 0b00: Ethernet 0b01: LLC_Other 0b10: RFC1042 0b11:As usage disabled	R/W	0x0
	[15:12]	RESERVED	Reserved		
0x070f	[15:0]	PPB0_ETHERTYPR	EtherType or DSAP/SSAP of protocol and port based item 0	R/W	0x0
0x0710	[7:0]	PPB1_VALID	Valid port mask for protocol-and-port-based item 1	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0711	[4:0]	PPB1_PORT0_INDEX	Port 0 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[9:5]	PPB1_PORT1_INDEX	Port 1 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[14:10]	PPB1_PORT2_INDEX	Port 2 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x0712	[4:0]	PPB1_PORT3_INDEX	Port 3 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[9:5]	PPB1_PORT4_INDEX	Port 4 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[14:10]	PPB1_PORT5_INDEX	Port 5 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x0713	[4:0]	PPB1_PORT6_INDEX	Port 6 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[9:5]	PPB1_PORT7_INDEX	Port 7 CVLAN index to CVLAN member configuration of protocol and port based item 1	R/W	0x0
	[11:10]	PPB1_FRAME_TYPE	Frame format of protocol and port based item 1 0b00: Ethernet 0b01: LLC_Other 0b10: RFC1042 0b11:As usage disabled	R/W	0x0
	[15:12]	RESERVED	Reserved		
0x0717	[15:0]	PPB1_ETHERTYPR	EtherType or DSAP/SSAP of protocol and port based item 1	R/W	0x0

0x0718	[7:0]	PPB2_VALID	Valid port mask for protocol-and-port-based item 2	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0719	[4:0]	PPB2_PORT0_INDEX	Port 0 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[9:5]	PPB2_PORT1_INDEX	Port 1 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[14:10]	PPB2_PORT2_INDEX	Port 2 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x071a	[4:0]	PPB2_PORT3_INDEX	Port 3 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[9:5]	PPB2_PORT4_INDEX	Port 4 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[14:10]	PPB2_PORT5_INDEX	Port 5 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x071b	[4:0]	PPB2_PORT6_INDEX	Port 6 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[9:5]	PPB2_PORT7_INDEX	Port 7 CVLAN index to CVLAN member configuration of protocol and port based item 2	R/W	0x0
	[11:10]	PPB2_FRAME_TYPE	Frame format of protocol and port based item 2 0b00: Ethernet 0b01: LLC_Other 0b10: RFC1042 0b11:As usage disabled	R/W	0x0
	[15:12]	RESERVED	Reserved		
0x071f	[15:0]	PPB2_ETHERTYPR	EtherType or DSAP/SSAP of protocol and port based item 2	R/W	0x0
0x0720	[7:0]	PPB3_VALID	Valid port mask for protocol-and-port-based item 3	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0721	[4:0]	PPB3_PORT0_INDEX	Port 0 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[9:5]	PPB3_PORT1_INDEX	Port 1 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[14:10]	PPB3_PORT2_INDEX	Port 2 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x0722	[4:0]	PPB3_PORT3_INDEX	Port 3 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[9:5]	PPB3_PORT4_INDEX	Port 4 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[14:10]	PPB3_PORT5_INDEX	Port 5 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x0723	[4:0]	PPB3_PORT6_INDEX	Port 6 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[9:5]	PPB3_PORT7_INDEX	Port 7 CVLAN index to CVLAN member configuration of protocol and port based item 3	R/W	0x0
	[14:10]	PPB3_FRAME_TYPE	Frame format of protocol and port based item 3 0b00: Ethernet 0b01: LLC_Other 0b10: RFC1042 0b11:As usage disabled	R/W	0x0
	[15]	RESERVED	Reserved		

0x0727	[15:0]	PPB3_ETHERTYPR	EtherType or DSAP/SSAP of protocol and port based item 3	R/W	0x0
0x0855	[2:0]	PORT0_PRIORITY	VLAN 1Q priority assignmnet for PORT 0 of protocol and port based item 0	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT1_PRIORITY	VLAN 1Q priority assignmnet for PORT 1 of protocol and port based item 0	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT2_PRIORITY	VLAN 1Q priority assignmnet for PORT 2 of protocol and port based item 0	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT3_PRIORITY	VLAN 1Q priority assignmnet for PORT 3 of protocol and port based item 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x0856	[2:0]	PORT4_PRIORITY	VLAN 1Q priority assignmnet for PORT 4 of protocol and port based item 0	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT5_PRIORITY	VLAN 1Q priority assignmnet for PORT 5 of protocol and port based item 0	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT6_PRIORITY	VLAN 1Q priority assignmnet for PORT 6 of protocol and port based item 0	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT7_PRIORITY	VLAN 1Q priority assignmnet for PORT 7 of protocol and port based item 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x0859	[2:0]	PORT0_PRIORITY	VLAN 1Q priority assignmnet for PORT 0 of protocol and port based item 1	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT1_PRIORITY	VLAN 1Q priority assignmnet for PORT 1 of protocol and port based item 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT2_PRIORITY	VLAN 1Q priority assignmnet for PORT 2 of protocol and port based item 1	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT3_PRIORITY	VLAN 1Q priority assignmnet for PORT 3 of protocol and port based item 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x085a	[2:0]	PORT4_PRIORITY	VLAN 1Q priority assignmnet for PORT 4 of protocol and port based item 1	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT5_PRIORITY	VLAN 1Q priority assignmnet for PORT 5 of protocol and port based item 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT6_PRIORITY	VLAN 1Q priority assignmnet for PORT 6 of protocol and port based item 1	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT7_PRIORITY	VLAN 1Q priority assignmnet for PORT 7 of protocol and port based item 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x085d	[2:0]	PORT0_PRIORITY	VLAN 1Q priority assignmnet for PORT 0 of protocol and port based item 2	R/W	0x0
	[3]	RESERVED	Reserved		

	[6:4]	PORT1_PRIORITY	VLAN 1Q priority assignment for PORT 1 of protocol and port based item 2	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT2_PRIORITY	VLAN 1Q priority assignment for PORT 2 of protocol and port based item 2	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT3_PRIORITY	VLAN 1Q priority assignment for PORT 3 of protocol and port based item 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x085e	[2:0]	PORT4_PRIORITY	VLAN 1Q priority assignment for PORT 4 of protocol and port based item 2	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT5_PRIORITY	VLAN 1Q priority assignment for PORT 5 of protocol and port based item 2	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT6_PRIORITY	VLAN 1Q priority assignment for PORT 6 of protocol and port based item 2	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT7_PRIORITY	VLAN 1Q priority assignment for PORT 7 of protocol and port based item 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x0861	[2:0]	PORT0_PRIORITY	VLAN 1Q priority assignment for PORT 0 of protocol and port based item 3	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT1_PRIORITY	VLAN 1Q priority assignment for PORT 1 of protocol and port based item 3	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT2_PRIORITY	VLAN 1Q priority assignment for PORT 2 of protocol and port based item 3	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT3_PRIORITY	VLAN 1Q priority assignment for PORT 3 of protocol and port based item 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x0862	[2:0]	PORT4_PRIORITY	VLAN 1Q priority assignment for PORT 4 of protocol and port based item 3	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT5_PRIORITY	VLAN 1Q priority assignment for PORT 5 of protocol and port based item 3	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT6_PRIORITY	VLAN 1Q priority assignment for PORT 6 of protocol and port based item 3	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT7_PRIORITY	VLAN 1Q priority assignment for PORT 7 of protocol and port based item 3	R/W	0x0
	[15]	RESERVED	Reserved		

2. RMA

2.1. Reserved Multicast Address Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0800	[0]	PORTISO_LEAKY	Bypass port isolation function for aware RESERVED Multicast Address 01-80-C2-00-00-00	R/W	0x0
	[1]	VLAN_LEAKY	Bypass CVLAN egress filtering for aware RESERVED Multicast Address 01-80-C2-00-00-00	R/W	0x0
	[2]	KEEP_FORMAT	Keep packet C-tag format for aware RESERVED Multicast Address 01-80-C2-00-00-00 0x0: disable 0x1: enable	R/W	0x0
	[5:3]	TRAP_PRIORITY	Priority assignment for frames trapped to CPU for aware RESERVED Multicast Address 01-80-C2-00-00-00	R/W	0x0
	[6]	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware RESERVED Multicast Address 01-80-C2-00-00-00	R/W	0x0
	[8:7]	OPERATION	Operation setting for aware RESERVED Multicast Address 01-80-C2-00-00-00 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	R/W	0x0
	[15:9]	RESERVED	Reserved		
0x0801	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-01	R/W	0x0
0x0802	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-02	R/W	0x0
0x0803	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-03	R/W	0x0
0x0804	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-04 ~ 01-80-C2-00-00-07 & 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C & 01-80-C2-00-00-0F	R/W	0x0
0x0808	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-08	R/W	0x0
0x080d	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-0D	R/W	0x0
0x080e	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-0E	R/W	0x0
0x0810	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-10	R/W	0x0

Address	Bit(s)	Name	Description	R/W	Default
0x0811	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-11	R/W	0x0
0x0812	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-12	R/W	0x0
0x0813	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F	R/W	0x0
0x0818	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-18	R/W	0x0
0x081a	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-1A	R/W	0x0
0x0820	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-20	R/W	0x0
0x0821	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-21	R/W	0x0
0x0822	[15:0]		As same as register 0x0800 for RESERVED Multicast Address 01-80-C2-00-00-22 ~ 01-80-C2-00-00-2F	R/W	0x0

3. IGMP

3.1. IGMP Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1c00	[0]	GMP_MLD_EN	H/W IGMP_MLD_EN 0b0: disable 0b1: enable	R/W	0x0
	[2:1]	CKS_ERR_OP	Checksum error option 0b00: Drop (Default) 0b01: Trap to CPU 0b10: Forward (Treat as normal packet) 0b11: Reserved	R/W	0x0
	[3]	FAST_LEAVE_EN	Fast Leave 1: Enable Fast Leave 0: Disable Fast Leave	R/W	0x0
	[6:4]	LEAVE_TIMER	Leave timer, Used as aging value, ASIC minus 1 every [Query Interval]	R/W	0x2
	[7]	REPORT_SUPPRESSION	Report Suppression 1: Enable 0: Disable	R/W	0x0
	[8]	LEAVE_SUPPRESSION	Learve Suppression 1: Enable 0: Disable	R/W	0x0
	[11:9]	ROBURSTNESS_VAR	Roburstness Variable, Used as aging value, ASIC minus 1 every [Query Interval]	R/W	0x3
	[12]	REPORT_FORWARD	control bit for IGMPv1/v2 and MLDv1 Report forwarding behavior 0:forward to router ports only 1:forward to all ports	R/W	0x0
	[13]	IGMP_MLD_DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for IGMP/MLD packets 1: Discard strom counting 0: Enable Strom counting	R/W	0x0
	[14]	IGMP_MLD_VLAN_LEAKY	VLAN leaky for IGMP/MLD packets 1: Enable Leaky 0: Disable Leaky	R/W	0x0
	[15]	IGMP_MLD_PORTISO_LEAKY	Port isolation leaky for IGMP/MLD packets 1: Enable Leaky 0: Disable Leaky	R/W	0x0
0x1c01	[1:0]	TABLE_FULL_OP	Table full option 0b00: Froward to Router port 0b01: Drop 0b10: Trap to CPU 0b11: Reserved	R/W	0x0
	[2]	DROP_LEAVE_ZERO	Discard Leave Packet with Group address = 0.0.0.0 1: Drop 0: Bypass	R/W	0x0
	[15:3]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
0x1c02	[15:0]	QUERY_INTERVAL	Query Interval	R/W	0x7D
0x1c03	[2:0]	D_ROUTER_PORT_TMR_1	1st dynamic router port timer	RO	0x0
	[6:3]	D_ROUTER_PORT_1	1st dynamic router port	RO	0xF
	[7]	RESERVED	Reserved		
	[10:8]	D_ROUTER_PORT_TMR_2	2nd dynamic router port timer	RO	0x0
	[14:11]	D_ROUTER_PORT_2	2nd dynamic router port	RO	0xF
	[15]	RESERVED	Reserved		
0x1c04	[7:0]	S_ROUTER_PORTMASK	Static router port mask	R/W	0x0
	[15:8]	RESERVED	Reserved		0x0
0x1c05	[1:0]	IGMPV1_OP	IGMPv1 operation control for Port 0 0b00: ASIC process 0b01: Flooding 0b10: Trap to CPU 0b11: Drop	R/W	0x0
	[3:2]	IGMPV2_OP	IGMPv2 operation control for Port 0 0b00: ASIC process 0b01: Flooding 0b10: Trap to CPU 0b11: Drop	R/W	0x0
	[5:4]	IGMPV3_OP	IGMPv3 operation control for Port 0 0b00: ASIC process 0b01: Flooding 0b10: Trap to CPU 0b11: Drop	R/W	0x0
	[7:6]	MLDV1_OP	MLDv1 operation control for Port 0 0b00: ASIC process 0b01: Flooding 0b10: Trap to CPU 0b11: Drop	R/W	0x0
	[9:8]	MLDV2_OP	MLDv2 operation control for Port 0 0b00: ASIC process 0b01: Flooding 0b10: Trap to CPU 0b11: Drop	R/W	0x0
	[10]	ALLOW_MC_DATA	Allow Multicast data packet 1: Allow 0: Drop		0x1
	[11]	ALLOW_MRP	Allow Multicast Routing protocol packet 1: Allow 0: Drop		0x1
	[12]	ALLOW_LEAVE	Allow to receive Leave packet 1: Allow 0: Drop		0x1

Address	Bit(s)	Name	Description	R/W	Default
	[13]	ALLOW_REPORT	Allow to receive Report packet 1: Allow 0: Drop		0x1
	[14]	ALLOW_QUERY	Allow to receive Query packet 1: Allow 0: Drop		0x1
	[15]	RESERVED	Reserved		
0x1c06	[15:0]		As same as register 0x1c05 for port 1		
0x1c07	[15:0]		As same as register 0x1c05 for port 2		
0x1c08	[15:0]		As same as register 0x1c05 for port 3		
0x1c09	[15:0]		As same as register 0x1c05 for port 4		
0x1c0a	[15:0]		As same as register 0x1c05 for port 5		
0x1c0b	[15:0]		As same as register 0x1c05 for port 6		
0x1c0c	[15:0]		As same as register 0x1c05 for port 7		

4. Ethernet AV

4.1. Ethernet AV Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0939	[0]	EAV_TRAP_8051	Trap 802.1AS packet to 8051	R/W	0x0
	[1]	EAV_TRAP_CPU	Trap 802.1AS packet to CPU	R/W	0x0
	[15:2]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
0x001d	[15:0]	EGRESS_TS_512NS	Egress timestamp of port 0 in 512 nanosecond[15:0]	RO	0x0
0x001e	[4:0]	EGRESS_TS_512NS	Egress timestamp of port 0 in 512 nanosecond[20:16]	RO	0x0
	[5]	EGRESS_TS_VALID	If EGRESS_TS_VALID is 1， it is read-clear。 0: Invalid 1: Valid	RC	0x0
	[6]	TIME_SYNC_TX_TS_FILL_EN	Will automatically fill previous TX timestamp in follow message 0: Disable 1: Enable	R/W	0x0
	[7]	TIME_SYNC_EN	Time Sync enable (support 802.1AS and IEEE 1588v2) 0: Disable 1: Enable	R/W	0x0
	[15:8]	TIME_TS_SECOND	Egress timestamp of this port in second 8-bits LSB	RO	0x0
0x003d	[15:0]		As same as register 0x001d for port 1		
0x003e	[15:0]		As same as register 0x001e for port 1		
0x005d	[15:0]		As same as register 0x001d for port 2		
0x005e	[15:0]		As same as register 0x001e for port 2		
0x007d	[15:0]		As same as register 0x001d for port 3		
0x007e	[15:0]		As same as register 0x001e for port 3		
0x009d	[15:0]		As same as register 0x001d for port 4		
0x009e	[15:0]		As same as register 0x001e for port 4		
0x00ad	[15:0]		As same as register 0x001d for port 5		
0x00ae	[15:0]		As same as register 0x001e for port 5		
0x00cd	[15:0]		As same as register 0x001d for port 6		
0x00ce	[15:0]		As same as register 0x001e for port 6		
0x00ed	[15:0]		As same as register 0x001d for port 7		
0x00ee	[15:0]		As same as register 0x001e for port 7		

5. LED

5.1. LED Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1b00	[1:0]	LED_SELECT	configuration system led mode 00:scan mode 0 01:scan mode 1 10:parallel mode 11:mdx mode (connect to s2p led ic) -- deault for 76s mode	R/W	0x3
	[2]	SEL_SERIAL_LED	0:mdx mode (scan mode) 1:serial mode	R/W	0
	[3]	LED_IO_DISABLE	configuration turn off the led I/O (I/O output enable) 0: normal 1: turn off the led I/O (I/O output enable)	R/W	0
	[4]	LED_POWERON_0	configuration led0 light when power-on light period 0: led0 off when power-on light period 1: led0 on when power-on light period	R/W	0x1
	[5]	LED_POWERON_1	configuration led1 light when power-on light period 0: led1 off when power-on light period 1: led1 on when power-on light period	R/W	0x1
	[6]	LED_POWERON_2	configuration led2 light when power-on light period 0: led2 off when power-on light period 1: led2 on when power-on light period	R/W	0x1
	[7]	SERI_LED_ACT_LOW	configuration if serial led active low 0: serial led active high 1: serial led active low	R/W	1
	[15:8]	RESERVED	Reserved		
0x1b02	[0]	RESERVED	Reserved		
	[3:1]	SEL_LEDRATE	select led blink rate 000 = 32 ms 001 = 64 ms 010 = 128 ms 011 = 256 ms 100 = 512 ms 101 = 1024 ms 110 = 48 ms 111 = 96 ms	R/W	0x1

Address	Bit(s)	Name	Description	R/W	Default
	[5:4]	FORCE_RATE	select led blink rate when cpu force blink 00 = 512 ms 01 = 1024 ms 10 = 2048 ms 11 = the same with cfg_led_blink_rate	R/W	0x3
	[7:6]	LOOP_DETECT_RATE	select led blink rate for loop detect 00 = 512 ms 01 = 1024 ms 10 = 1536 ms 11 = 2048 ms	R/W	0x0
	[8]	RESERVED	Reserved		
	[10:9]	SEL_PWRON_TIME	select power on led light continue time 00: Power on light time is 800ms (0.8s) 01: Power on light time is 1200ms (1.2s) 10: Power on light time is 1600ms (1.6s) 11: Power on light time is 2000ms (2s)	R/W	0x0
	[11]	LOOP_DETECT_MODE	select loop detection mode 0:mode 0 1:mode 1	R/W	0x0
	[13:12]	BUZZER_RATE	select buzzer rate for loop detect 00 = 1k 01 = 2k 10 = 4k 11 = 8kHz	R/W	0x1
	[14]	LED_BUZZ_DUTY	select buzzer duty for loop detect 0: duty 50% high 1: duty 75% high	R/W	0x1
	[15]	RESERVED	Reserved	R/W	0x0
0x1b03	[3:0]	LED0_CFG	LED Control Register 1	R/W	0x2
	[7:4]	LED1_CFG		R/W	0x3
	[11:8]	LED2_CFG		R/W	0x4
	[15:12]	RESERVED	Reserved		
0x1b08	[1:0]	Force_PORT0_LED0	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[3:2]	Force_PORT1_LED0	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[5:4]	Force_PORT2_LED0	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0

Address	Bit(s)	Name	Description	R/W	Default
	[7:6]	Force_PORT3_LED0	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[9:8]	Force_PORT4_LED0	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[15:10]	RESERVED	Reserved		
0x1b0a	[1:0]	Force_PORT0_LED1	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[3:2]	Force_PORT1_LED1	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[5:4]	Force_PORT2_LED1	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[7:6]	Force_PORT3_LED1	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[9:8]	Force_PORT4_LED1	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[15:10]	RESERVED	Reserved		
0x1b0c	[1:0]	Force_PORT0_LED2	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[3:2]	Force_PORT1_LED2	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[5:4]	Force_PORT2_LED2	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[7:6]	Force_PORT3_LED2	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0

Address	Bit(s)	Name	Description	R/W	Default
	[9:8]	Force_PORT4_LED2	00: normal mode (not force) 01: cpu force led to blink (cfg_led_force_rate) 10: cpu force led to 0 11: cpu force led to 1	R/W	0x0
	[15:10]	RESERVED	Reserved		
0x1b24	[7:0]	LED0_PARA_P07_00	Led group 0 parameter p07-p00	R/W	0xFF
	[15:8]	LED1_PARA_P07_00	Led group 1 parameter p07-p00	R/W	0xFF
0x1b25	[7:0]	LED1_PARA_P07_00	Led group 2 parameter p07-p00	R/W	0xFF
	[15:8]	RESERVED	Reserved	R/W	0xFF
0x1b26	[0]	LED_SERI_CLK_EN	led_seri_clk_en	R/W	0x1
	[1]	LED_SERI_DATA_EN	led_seri_data_en	R/W	0x1
	[2]	LED_LOOP_DET_BUZZER_EN	led_loop_det_buzzer_en	R/W	0x1
	15:3]	RESERVED	Reserved		

5.2. LEDx_CFG Definition

Definition	LED Statuses	Description
0000	LED_Off	LED pin Tri-State.
0001	Dup/Col	Collision, Full duplex Indicator. Blinking every 43ms when collision happens. Low for full duplex, and high for half duplex mode.
0010	Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinks every 43ms when the corresponding port is transmitting or receiving.
0011	Spd1000	1000Mb/s Speed Indicator. Low for 1000Mb/s.
0100	Spd100	100Mb/s Speed Indicator. Low for 100Mb/s.
0101	Spd10	10Mb/s Speed Indicator. Low for 10Mb/s.
0110	Spd1000/Act	1000Mb/s Speed/Activity Indicator. Low for 1000Mb/s. Blinks every 43ms when the corresponding port is transmitting or receiving.
0111	Spd100/Act	100Mb/s Speed/Activity Indicator. Low for 100Mb/s. Blinks every 43ms when the corresponding port is transmitting or receiving.
1000	Spd10/Act	10Mb/s Speed/Activity Indicator. Low for 10Mb/s. Blinks every 43ms when the corresponding port is transmitting or receiving.
1001	Spd100 (10)/Act	10/100Mb/s Speed/Activity Indicator. Low for 10/100Mb/s. Blinks every 43ms when the corresponding port is transmitting or receiving.
1010	LoopDetect	Loop detection indicator
1011	eee_cap/eee_lpi	EEE capability indicator. Blinking when port enters into LPI state.
1100	Spd1000(100)/Act	1000/100 Mb/s Speed/Activity Indicator. Low for 1000/100 Mb/s. Blinks every 43ms when the corresponding port is transmitting or receiving.
1101	Spd1000(10)/Act	1000/10 Mb/s Speed/Activity Indicator. Low for 1000/10 Mb/s. Blinks every 43ms when the corresponding port is transmitting or receiving.
1110	Master	Link on Master Indicator. Low for link Master established.
1111	1'b0/Act	Blinking when corresponding port is transmitting or receiving.

6. CPU Port

6.1. CPU Port Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1219	[7:0]	CPU_PORT_MASK	CPU tag aware port mask	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x121a	[0]	CPU_EN	Enable CPU tag function	R/W	0x0
	[2:1]	CPU_INSERTMODE	Egress packet CPU tag inserting mode 0b00: Insert CPU tag to all packets 0b01: Insert CPU tag to trapping frames only. The trapping reason must be not 0. 0b10: Not insert CPU tag to egressing packets 0b11:reserved	R/W	0x1
	[5:3]	CPU_TRAP_PORT	Port number to transmiting out trapping frame	R/W	0x0
	[6]	CPU_TAG_POSITION	The CPU tag position in packet 0b0: After MAC_SA 0b1: After entire packet(before CRC field)	R/W	0x0
	[7]	CPU_TAG_RXBYTECOUNT	CPU tag frame receiving byte count length include cpu-tag (default 1) 0b0:disable, normal CPU tag frame should be 72(64+8) bytes 0b1:enable, accept cpu-tag frame in 64 bytes only	R/W	0x1
	[15:8]	RESERVED	Reserved		

7. Mirror

7.1. Port Mirror Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x121c	[3:0]	SOURCE_PORT	Select the source port to be mirrored.	R/W	0x0
	[7:4]	MINITOR_PORT	Select the monitor port.	R/W	0x0
	[8]	RESERVED	Reserved		
	[9]	MIRROR_RX	Enable the mirror function on RX of the source port. 0b0: Disable 0b1: Enable	R/W	0
	[10]	MIRROR_TX	Enable the mirror function on TX of the source port.	R/W	0
	[11]	MIRROR_ISO	Enable isolation of TX traffic on the monitor port. 0: Normal operation 0b1: The monitor port will accept only packets from the source port. Other packets destined to the monitor port will be dropped.	R/W	0
	[15:12]	RESERVED	Reserved		
0x12fb	[7:0]	MIRROR_SRC_PMSK	Mirror Source Port Mask	R/W	0
	[15:8]	RESERVED	Reserved		

8. Storm Filtering

8.1. Storm Filtering Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0a40	[7:0]	BC_STORM_EN	Per port broadcasting storm filtering setting	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a41	[7:0]	MC_STORM_EN	Per port multicasting storm filtering setting	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a42	[7:0]	UNDA_STORM_EN	Per port unkown unicasting storm filtering setting	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a43	[7:0]	UNMC_STORM_EN	Per port unkown multicasting storm filtering setting	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a44	[7:0]	PORT0_METERIDX	Port 0 broadcast storm meter index	R/W	0x0
	[15:8]	PORT1_METERIDX	Port 1 broadcast storm meter index	R/W	0x0
0x0a45	[7:0]	PORT2_METERIDX	Port 2 broadcast storm meter index	R/W	0x0
	[15:8]	PORT3_METERIDX	Port 3 broadcast storm meter index	R/W	0x0
0x0a46	[7:0]	PORT4_METERIDX	Port 4 broadcast storm meter index	R/W	0x0
	[15:8]	PORT5_METERIDX	Port 5 broadcast storm meter index	R/W	0x0
0x0a47	[7:0]	PORT6_METERIDX	Port 6 broadcast storm meter index	R/W	0x0
	[15:8]	PORT7_METERIDX	Port 7 broadcast storm meter index	R/W	0x0
0x0a4c	[7:0]	PORT0_METERIDX	Port 0 multicast storm meter index	R/W	0x0
	[15:8]	PORT1_METERIDX	Port 1 multicast storm meter index	R/W	0x0
0x0a4d	[7:0]	PORT2_METERIDX	Port 2 multicast storm meter index	R/W	0x0
	[15:8]	PORT3_METERIDX	Port 3 multicast storm meter index	R/W	0x0
0x0a4e	[7:0]	PORT4_METERIDX	Port 4 multicast storm meter index	R/W	0x0
	[15:8]	PORT5_METERIDX	Port 5 multicast storm meter index	R/W	0x0
0x0a4f	[7:0]	PORT6_METERIDX	Port 6 multicast storm meter index	R/W	0x0
	[15:8]	PORT7_METERIDX	Port 7 multicast storm meter index	R/W	0x0
0x0a54	[7:0]	PORT0_METERIDX	Port 0 unknown unicast storm meter index	R/W	0x0
	[15:8]	PORT1_METERIDX	Port 1 unknown unicast storm meter index	R/W	0x0
0x0a55	[7:0]	PORT2_METERIDX	Port 2 unknown unicast storm meter index	R/W	0x0
	[15:8]	PORT3_METERIDX	Port 3 unknown unicast storm meter index	R/W	0x0
0x0a56	[7:0]	PORT4_METERIDX	Port 4 unknown unicast storm meter index	R/W	0x0
	[15:8]	PORT5_METERIDX	Port 5 unknown unicast storm meter index	R/W	0x0
0x0a57	[7:0]	PORT6_METERIDX	Port 6 unknown unicast storm meter index	R/W	0x0
	[15:8]	PORT7_METERIDX	Port 7 unknown unicast storm meter index	R/W	0x0
0x0a5c	[7:0]	PORT0_METERIDX	Port 0 unknown multicast storm meter index	R/W	0x0
	[15:8]	PORT1_METERIDX	Port 1 unknown multicast storm meter index	R/W	0x0
0x0a5d	[7:0]	PORT2_METERIDX	Port 2 unknown multicast storm meter index	R/W	0x0
	[15:8]	PORT3_METERIDX	Port 3 unknown multicast storm meter index	R/W	0x0

Address	Bit(s)	Name	Description	R/W	Default
0x0a5e	[7:0]	PORT4_METERIDX	Port 4 unknown multicast storm meter index	R/W	0x0
	[15:8]	PORT5_METERIDX	Port 5 unknown multicast storm meter index	R/W	0x0
0x0a5f	[7:0]	PORT6_METERIDX	Port 6 unknown multicast storm meter index	R/W	0x0
	[15:8]	PORT7_METERIDX	Port 7 unknown multicast storm meter index	R/W	0x0

9. Interrupt

9.1. Interrupt Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1100	[0]	Interrupt Polarity	Pull low or pull high interrupt pin 0b0: pull high 0b1: pull low	R/W	0x0
	[15:1]	RESERVED	Reserved		
0x1101	[0]	Link change	Enable port linking change interrupt 0b0: Disable 0b1: Enable	R/W	0x0
	[1]	METER_EXCEEDED	IMR for meter exceed	R/W	0x0
	[2]	LEARN_OVER	IMR for L2 learn over	R/W	0x0
	[3]	SPEED_CHANGE	IMR for speed change	R/W	0x0
	[4]	SPECIAL_CONGEST	IMR for TX special congest	R/W	0x0
	[5]	GREEN_TIMER	IMR for update ingress page rate	R/W	0x0
	[6]	LOOP_DETECTION	IMR for have loop detected or loop recoved situation happen	R/W	0x0
	[7]	INTERRUPT_8051	IMR for Interrupt from 8051	R/W	0x0
	[8]	CABLE_DIAG_FIN	IMR for Cable Diag finish	R/W	0x0
	[9]	ACL_ACTION	IMR for ACL interrupt	R/W	0x0
	[10]	UPS_EVENT	IMR for UPS state trigger	R/W	0x0
	[11]	SLIENT_START	IMR for Slient Start	R/W	0x0
	[15:12]	RESERVED	Reserved		
0x1102	[0]	Link change	IMS for link change,write 1 to clear	R/O	0x0
	[1]	METER_EXCEEDED	IMS for meter exceed,write 1 to clear	R/O	0x0
	[2]	LEARN_OVER	IMS for L2 learn over,write 1 to clear	R/O	0x0
	[3]	SPEED_CHANGE	IMS for speed change,write 1 to clear	R/O	0x0
	[4]	SPECIAL_CONGEST	IMS for TX special congest,write 1 to clear	R/O	0x0
	[5]	GREEN_TIMER	IMS for update ingress page rate,write 1 to clear	R/O	0x0
	[6]	LOOP_DETECTION	IMS for have loop detected or loop recoved situation happen,write 1 to clear	R/O	0x0
	[7]	INTERRUPT_8051	IMS for Interrupt from 8051,write 1 to clear	R/O	0x0
	[8]	CABLE_DIAG_FIN	IMS for Cable Diag finish,write 1 to clear	R/O	0x0
	[9]	ACL_ACTION	IMS for ACL interrupt,write 1 to clear	R/O	0x0
	[10]	UPS_EVENT	IMS for UPS state trigger,write 1 to clear	R/O	0x0
	[11]	SLIENT_START	IMS for Slient Start,write 1 to clear	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1103	[7:0]	LEARN_OVER	L2 learn over ever occurs,write 1 to clear	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1104	[7:0]	SPEED_CHANGE	speed changer ever occurs,write 1 to clear	R/O	0x0

	[15:8]	RESERVED	Reserved		
0x1105	[7:0]	SPECIAL_CONGEST	TX special congest ever occurs,write 1 to clear	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1106	[7:0]	PORT_LINKDOWN	Per port had been link down state,write 1 to clear	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1107	[7:0]	PORT_LINKUP	Per port had been link up state,write 1 to clear	R/O	0x0
	[15:8]	RESERVED	Reserved		

10. QoS

10.1. Per-Port Input Bandwidth Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x000e	[3:0]	RESERVED	Reserved	R/W	
	[5:4]	VLAN_PORT0_EGRESS_MODE	Per-portVLAN tag egress format 0b00: Original mode. Output frame will follow VLAN untag setting. 0b01: Keep format mode. Output frame will keep VLAN original format. 0b10: Priority tag mode. Output frame will be priority tag. 0b11: Real keep mode. Output frame will keep CVID and C-tag format	R/W	
	[6]	MAC_LOOPBACK	enable loopback from Tx to Rx in MAC 0b1:enable mac loop-back function	R/W	0
	[7]	RESERVED	Reserved		
	[8]	CRC_SKIP	skip L2CRC check 0b0:disable 0b1:enable	R/W	0
	[9]	RX_SPC	enable received special packet which packet length is smaller than 64 bytes, or received packet is not byte alignment and L2 CRC errored packet 0b0:disable 0b1:enable	R/W	0
	[10]	INGRESSBW_PORT0_IFG	Bandwidth Control Include/exclude Preamble & IFG (20bytes) 0: exclude, 1: include	R/W	0
	[11]	INGRESSBW_PORT0_FLOWCRTL	Flow control setting while input rate is over input bandwidth 0: disable, drop packet 1: enable flow control	R/W	1
	[15:12]	RESERVED	Reserved		
0x000f	[15:0]	INGRESSBW_PORT0_RATE15_0	Ingress Bandwidth Control, unit: 8Kbps (K=1024) 17'h1ffff : BW= full rate (line rate) N : BW=N*8Kbps	R/W	0xFFFF
0x0010	[0]	INGRESSBW_PORT0_RATE16	MSB bit[16] of Ingress Bandwidth Control N : BW=N*8Kbps	R/W	1
	[15:1]	RESERVED	Reserved		
0x002e		P1MISC	Same as 0x000e		
0x002f		P1INBWRATE_L	Same as 0x000f		
0x0030		P1INBWRATE_L	Same as 0x0010		
0x004e		P2MISC	Same as 0x000e		
0x004f		P2INBWRATE_L	Same as 0x000f		
0x0050		P2INBWRATE_L	Same as 0x0010		

0x006e		P3MISC	Same as 0x000e		
0x006f		P3INBWRATE_L	Same as 0x000f		
0x0070		P3INBWRATE_L	Same as 0x0010		
0x008e		P4MISC	Same as 0x000e		
0x008f		P4INBWRATE_L	Same as 0x000f		
0x0090		P4INBWRATE_L	Same as 0x0010		
0x00ae		P5MISC	Same as 0x000e		
0x00af		P5INBWRATE_L	Same as 0x000f		
0x00b0		P5INBWRATE_L	Same as 0x0010		
0x00ce		P6MISC	Same as 0x000e		
0x00cf		P6INBWRATE_L	Same as 0x000f		
0x00d0		P6INBWRATE_L	Same as 0x0010		
0x00ee		P7MISC	Same as 0x000e		
0x00ef		P7INBWRATE_L	Same as 0x000f		
0x00f0		P7INBWRATE_L	Same as 0x0010		

10.2. Per-Port Output Bandwidth Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0300	[0]	WFQ_IFG	Rate calculation include IFG(Inter Frame Gap) setting in WFQ leaky bucket 0b0:exclude IPG 0b1:inculde IPG	R/W	1
	[15:2]	RESERVED	Reserved		
0x038c	[15:0]	P00_RATE_L	Egress rate LSB of port 0	R/W	0xFFFF
0x038d	[0]	P00_RATE_H	Egress rate MSB[15] of port 0	R/W	1
	[15:1]	RESERVED	Reserved		
0x038e		P01_RATE_L	Same as 0x038c		
0x038f		P01_RATE_H	Same as 0x038d		
0x0390		P02_RATE_L	Same as 0x038c		
0x0391		P02_RATE_H	Same as 0x038d		
0x0392		P03_RATE_L	Same as 0x038c		
0x0393		P03_RATE_H	Same as 0x038d		
0x0394		P04_RATE_L	Same as 0x038c		
0x0395		P04_RATE_H	Same as 0x038d		
0x0396		P05_RATE_L	Same as 0x038c		
0x0397		P05_RATE_H	Same as 0x038d		
0x0398		P06_RATE_L	Same as 0x038c		
0x0399		P06_RATE_H	Same as 0x038d		
0x039a		P07_RATE_L	Same as 0x038c		
0x039b		P07_RATE_H	Same as 0x038d		

10.3. Remarking Register

10.3.1. Remarking Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x120C	[7:0]	RESERVED	Reserved		
	[8]	REMARKING_DSCP_ENABLE	DSCP remarking enale setting 0b0:disable 0b1:enable	R/W	0x0
	[15:9]	RESERVED	Reserved		
0x000e	[11:0]	RESERVED	Reserved		
	[12]	DOT1Q_REMARK_ENABLE	1Q remarking enable setting of Port 0 0b0:disable 0b1:enable	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x002e	[15:0]		As same as register 0x000e for Port 1	R/W	0x0
0x004e	[15:0]		As same as register 0x000e for Port 2	R/W	0x0
0x006e	[15:0]		As same as register 0x000e for Port 3	R/W	0x0
0x008e	[15:0]		As same as register 0x000e for Port 4	R/W	0x0
0x00ae	[15:0]		As same as register 0x000e for Port 5	R/W	0x0
0x00ce	[15:0]		As same as register 0x000e for Port 6	R/W	0x0
0x00ee	[15:0]		As same as register 0x000e for Port 7	R/W	0x0

10.3.2. 802.1p Remarking Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1211	[2:0]	INTPRI0_PRI	8021.Q remarking value for internal priority 0	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	INTPRI1_PRI	8021.Q remarking value for internal priority 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	INTPRI2_PRI	8021.Q remarking value for internal priority 2	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	INTPRI3_PRI	8021.Q remarking value for internal priority 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x1212	[2:0]	INTPRI4_PRI	8021.Q remarking value for internal priority 4	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	INTPRI5_PRI	8021.Q remarking value for internal priority 5	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	INTPRI6_PRI	8021.Q remarking value for internal priority 6	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	INTPRI7_PRI	8021.Q remarking value for internal priority 7	R/W	0x0
	[15]	RESERVED	Reserved		

10.3.3. DSCP Remarking Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x120d	[5:0]	INTPRI0_DSCP	DSCP remarking value for internal priority 0	R/W	0x0
	[7:6]	RESERVED	Reserved		
	[13:8]	INTPRI1_DSCP	DSCP remarking value for internal priority 1	R/W	0x0
	[15:14]	RESERVED	Reserved		
0x120e	[5:0]	INTPRI2_DSCP	DSCP remarking value for internal priority 2	R/W	0x0

	[7:6]	RESERVED	Reserved		
	[13:8]	INTPRI3_DSCP	DSCP remarking value for internal priority 3	R/W	0x0
	[15:14]	RESERVED	Reserved		
0x120f	[5:0]	INTPRI4_DSCP	DSCP remarking value for internal priority 4	R/W	0x0
	[7:6]	RESERVED	Reserved		
	[13:8]	INTPRI5_DSCP	DSCP remarking value for internal priority 5	R/W	0x0
	[15:14]	RESERVED	Reserved		
0x1210	[5:0]	INTPRI6_DSCP	DSCP remarking value for internal priority 6	R/W	0x0
	[7:6]	RESERVED	Reserved		
	[13:8]	INTPRI7_DSCP	DSCP remarking value for internal priority 7	R/W	0x0
	[15:14]	RESERVED	Reserved		

10.4. Port-based Priority Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0877	[2:0]	PBP0PRI	Port-based Priority assign for port 0.	R/W	0x0
	[5:3]	PBP1PRI	Port-based Priority assign for port 1.	R/W	0x0
	[8:6]	PBP2PRI	Port-based Priority assign for port 2.	R/W	0x0
	[11:9]	PBP3PRI	Port-based Priority assign for port 3.	R/W	0x0
	[15:12]	RESERVED	Reserved		
0x0878	[2:0]	PBP4PRI	Port-based Priority assign for port 4	R/W	0x0
	[5:3]	PBP5PRI	Port-based Priority assign for port 5	R/W	0x0
	[8:6]	PBP6PRI	Port-based Priority assign for port 6	R/W	0x0
	[11:9]	PBP7PRI	Port-based Priority assign for port 7	R/W	0x0
	[15:12]	RESERVED	Reserved		

10.5. DSCP-based Priority Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0867	[2:0]	DSCP0_PRIORITY	DSCP to internal priority for DSCP 0	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP1_PRIORITY	DSCP to internal priority for DSCP 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP2_PRIORITY	DSCP to internal priority for DSCP 2	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP3_PRIORITY	DSCP to internal priority for DSCP 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x0868	[2:0]	DSCP4_PRIORITY	DSCP to internal priority for DSCP 4	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP5_PRIORITY	DSCP to internal priority for DSCP 5	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP6_PRIORITY	DSCP to internal priority for DSCP 6	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP7_PRIORITY	DSCP to internal priority for DSCP 7	R/W	0x0
	[15]	RESERVED	Reserved		
0x0869	[2:0]	DSCP8_PRIORITY	DSCP to internal priority for DSCP 8	R/W	0x0
	[3]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
	[6:4]	DSCP9_PRIORITY	DSCP to internal priority for DSCP 9	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP10_PRIORITY	DSCP to internal priority for DSCP 10	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP11_PRIORITY	DSCP to internal priority for DSCP 11	R/W	0x0
	[15]	RESERVED	Reserved		
0x086a	[2:0]	DSCP12_PRIORITY	DSCP to internal priority for DSCP 12	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP13_PRIORITY	DSCP to internal priority for DSCP 13	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP14_PRIORITY	DSCP to internal priority for DSCP 14	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP15_PRIORITY	DSCP to internal priority for DSCP 15	R/W	0x0
	[15]	RESERVED	Reserved		
0x086b	[2:0]	DSCP16_PRIORITY	DSCP to internal priority for DSCP 16	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP17_PRIORITY	DSCP to internal priority for DSCP 17	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP18_PRIORITY	DSCP to internal priority for DSCP 18	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP19_PRIORITY	DSCP to internal priority for DSCP 19	R/W	0x0
	[15]	RESERVED	Reserved		
0x086c	[2:0]	DSCP20_PRIORITY	DSCP to internal priority for DSCP 20	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP21_PRIORITY	DSCP to internal priority for DSCP 21	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP22_PRIORITY	DSCP to internal priority for DSCP 22	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP23_PRIORITY	DSCP to internal priority for DSCP 23	R/W	0x0
	[15]	RESERVED	Reserved		
0x086d	[2:0]	DSCP24_PRIORITY	DSCP to internal priority for DSCP 24	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP25_PRIORITY	DSCP to internal priority for DSCP 25	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP26_PRIORITY	DSCP to internal priority for DSCP 26	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP27_PRIORITY	DSCP to internal priority for DSCP 27	R/W	0x0
	[15]	RESERVED	Reserved		
0x086e	[2:0]	DSCP28_PRIORITY	DSCP to internal priority for DSCP 28	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP29_PRIORITY	DSCP to internal priority for DSCP 29	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP30_PRIORITY	DSCP to internal priority for DSCP 30	R/W	0x0
	[11]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
	[14:12]	DSCP31_PRIORITY	DSCP to internal priority for DSCP 31	R/W	0x0
	[15]	RESERVED	Reserved		
0x086f	[2:0]	DSCP32_PRIORITY	DSCP to internal priority for DSCP 32	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP33_PRIORITY	DSCP to internal priority for DSCP 33	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP34_PRIORITY	DSCP to internal priority for DSCP 34	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP35_PRIORITY	DSCP to internal priority for DSCP 35	R/W	0x0
	[15]	RESERVED	Reserved		
0x0870	[2:0]	DSCP36_PRIORITY	DSCP to internal priority for DSCP 36	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP37_PRIORITY	DSCP to internal priority for DSCP 37	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP38_PRIORITY	DSCP to internal priority for DSCP 38	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP39_PRIORITY	DSCP to internal priority for DSCP 39	R/W	0x0
	[15]	RESERVED	Reserved		
0x0871	[2:0]	DSCP40_PRIORITY	DSCP to internal priority for DSCP 40	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP41_PRIORITY	DSCP to internal priority for DSCP 41	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP42_PRIORITY	DSCP to internal priority for DSCP 42	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP43_PRIORITY	DSCP to internal priority for DSCP 43	R/W	0x0
	[15]	RESERVED	Reserved		
0x0872	[2:0]	DSCP44_PRIORITY	DSCP to internal priority for DSCP 44	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP45_PRIORITY	DSCP to internal priority for DSCP 45	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP46_PRIORITY	DSCP to internal priority for DSCP 46	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP47_PRIORITY	DSCP to internal priority for DSCP 47	R/W	0x0
	[15]	RESERVED	Reserved		
0x0873	[2:0]	DSCP48_PRIORITY	DSCP to internal priority for DSCP 48	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP49_PRIORITY	DSCP to internal priority for DSCP 49	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP50_PRIORITY	DSCP to internal priority for DSCP 50	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP51_PRIORITY	DSCP to internal priority for DSCP 51	R/W	0x0
	[15]	RESERVED	Reserved		
0x0874	[2:0]	DSCP52_PRIORITY	DSCP to internal priority for DSCP 52	R/W	0x0
	[3]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
	[6:4]	DSCP53_PRIORITY	DSCP to internal priority for DSCP 53	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP54_PRIORITY	DSCP to internal priority for DSCP 54	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP55_PRIORITY	DSCP to internal priority for DSCP 55	R/W	0x0
	[15]	RESERVED	Reserved		
0x0875	[2:0]	DSCP56_PRIORITY	DSCP to internal priority for DSCP 56	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP57_PRIORITY	DSCP to internal priority for DSCP 57	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP58_PRIORITY	DSCP to internal priority for DSCP 58	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP59_PRIORITY	DSCP to internal priority for DSCP 59	R/W	0x0
	[15]	RESERVED	Reserved		
0x0876	[2:0]	DSCP60_PRIORITY	DSCP to internal priority for DSCP 56	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	DSCP61_PRIORITY	DSCP to internal priority for DSCP 57	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	DSCP62_PRIORITY	DSCP to internal priority for DSCP 58	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	DSCP63_PRIORITY	DSCP to internal priority for DSCP 59	R/W	0x0
	[15]	RESERVED	Reserved		

10.6. 802.1Q-based Mapping Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0865	[2:0]	1QPRI0MAP	1Q priority 0 mapping to Internal Priority	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	1QPRI1MAP	1Q priority 1 mapping to Internal Priority	R/W	0x1
	[7]	RESERVED	Reserved		
	[10:8]	1QPRI2MAP	1Q priority 2 mapping to Internal Priority	R/W	0x2
	[11]	RESERVED	Reserved		
	[14:12]	1QPRI3MAP	1Q priority 3 mapping to Internal Priority	R/W	0x3
	[15]	RESERVED	Reserved		
0x0866	[2:0]	1QPRI4MAP	1Q priority 4 mapping to Internal Priority	R/W	0x4
	[3]	RESERVED	Reserved		
	[6:4]	1QPRI5MAP	1Q priority 5 mapping to Internal Priority	R/W	0x5
	[7]	RESERVED	Reserved		
	[10:8]	1QPRI6MAP	1Q priority 6 mapping to Internal Priority	R/W	0x6
	[11]	RESERVED	Reserved		
	[14:12]	1QPRI7MAP	1Q priority 7 mapping to Internal Priority	R/W	0x7
	[15]	RESERVED	Reserved		

10.7. Priority Decision Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x087b	[7:0]	QOS_PORT_WEIGHT	Internal priority decision weight configuration of port based priority source	R/W	0x0
	[15:8]	QOS_ACL_WEIGHT	Internal priority decision weight configuration of ACL priority source	R/W	0x0
0x087c	[7:0]	QOS_DSCP_WEIGHT	Internal priority decision weight configuration of DSCP based priority source	R/W	0x0
	[15:8]	QOS_DOT1Q_WEIGHT	Internal priority decision weight configuration of 802.1Q based priority source	R/W	0x0
0x087d	[7:0]	QOS_SVLAN_WEIGHT	Internal priority decision weight configuration of SVLAN based priority source	R/W	0x0
	[15:8]	QOS_CVLAN_WEIGHT	Internal priority decision weight configuration of CVLAN based priority source	R/W	0x0
0x087e	[7:0]	QOS_DA_WEIGHT	Internal priority decision weight configuration of destination MAC based priority source	R/W	0x0
	[15:8]	QOS_SA_WEIGHT	Internal priority decision weight configuration of source MAC based priority source	R/W	0x0

10.8. Output Queue Number Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0900	[2:0]	PORT0_NUMBER	Queue number assignment for PORT 0	R/W	0x1
	[3]	RESERVED	Reserved		
	[6:4]	PORT1_NUMBER	Queue number assignment for PORT 1	R/W	0x1
	[7]	RESERVED	Reserved		
	[10:8]	PORT2_NUMBER	Queue number assignment for PORT 2	R/W	0x1
	[11]	RESERVED	Reserved		
	[14:12]	PORT3_NUMBER	Queue number assignment for PORT 3	R/W	0x1
	[15]	RESERVED	Reserved		
0x0901	[2:0]	PORT4_NUMBER	Queue number assignment for PORT 4	R/W	0x1
	[3]	RESERVED	Reserved		
	[6:4]	PORT5_NUMBER	Queue number assignment for PORT 5	R/W	0x1
	[7]	RESERVED	Reserved		
	[10:8]	PORT6_NUMBER	Queue number assignment for PORT 6	R/W	0x1
	[11]	RESERVED	Reserved		
	[14:12]	PORT7_NUMBER	Queue number assignment for PORT 7	R/W	0x1
	[15]	RESERVED	Reserved		

10.9. QNUM and Priority to QID Mapping Register

Address	Bit(s)	Name	Description	R/W	Default
0x0904	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 1st queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 1st queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 1st queue mapping table	R/W	0x0
	[11]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 1st queue mapping table	R/W	0x0
	[15]	RESERVED	Reserved		
0x0905	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 1st queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 1st queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 1st queue mapping table	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 1st queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		
0x0906	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 2Pnd queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 2Pnd queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 2Pnd queue mapping table	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 2Pnd queue mapping table	R/W	0x0
	[15]	RESERVED	Reserved		
0x0907	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 2Pnd queue mapping table	R/W	0x7
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 2Pnd queue mapping table	R/W	0x7
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 2Pnd queue mapping table	R/W	0x7
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 2Pnd queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		
0x0908	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 3Prd queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 3Prd queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 3Prd queue mapping table	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 3Prd queue mapping table	R/W	0x0
	[15]	RESERVED	Reserved		
0x0909	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 3Prd queue mapping table	R/W	0x1
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 3Prd queue mapping table	R/W	0x1
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 3Prd queue mapping table	R/W	0x7
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 3Prd queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		
0x090a	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 4Pth queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 4Pth queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 4Pth queue mapping table	R/W	0x1
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 4Pth queue mapping table	R/W	0x1
	[15]	RESERVED	Reserved		
0x090b	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 4Pth queue mapping table	R/W	0x2

Address	Bit(s)	Name	Description	R/W	Default
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 4Pth queue mapping table	R/W	0x2
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 4Pth queue mapping table	R/W	0x7
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 4Pth queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		
0x090c	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 5Pth queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 5Pth queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 5Pth queue mapping table	R/W	0x1
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 5Pth queue mapping table	R/W	0x1
	[15]	RESERVED	Reserved		
0x090d	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 5Pth queue mapping table	R/W	0x2
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 5Pth queue mapping table	R/W	0x3
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 5Pth queue mapping table	R/W	0x7
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 5Pth queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		
0x090e	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 6Pth queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 6Pth queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 6Pth queue mapping table	R/W	0x1
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 6Pth queue mapping table	R/W	0x2
	[15]	RESERVED	Reserved		
0x090f	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 6Pth queue mapping table	R/W	0x3
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 6Pth queue mapping table	R/W	0x4
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 6Pth queue mapping table	R/W	0x7
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 6Pth queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		
0x0910	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 7Pth queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 7Pth queue mapping table	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 7Pth queue mapping table	R/W	0x1
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 7Pth queue mapping table	R/W	0x2
	[15]	RESERVED	Reserved		
0x0911	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 7Pth queue mapping table	R/W	0x3
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 7Pth queue mapping table	R/W	0x4
	[7]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 7Pth queue mapping table	R/W	0x5
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 7Pth queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		
0x0912	[2:0]	PRIORITY0_TO_QID	Priority 0 to queue id in 8Pth queue mapping table	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY1_TO_QID	Priority 1 to queue id in 8Pth queue mapping table	R/W	0x1
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY2_TO_QID	Priority 2 to queue id in 8Pth queue mapping table	R/W	0x2
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY3_TO_QID	Priority 3 to queue id in 8Pth queue mapping table	R/W	0x3
	[15]	RESERVED	Reserved		
0x0913	[2:0]	PRIORITY4_TO_QID	Priority 4 to queue id in 8Pth queue mapping table	R/W	0x4
	[3]	RESERVED	Reserved		
	[6:4]	PRIORITY5_TO_QID	Priority 5 to queue id in 8Pth queue mapping table	R/W	0x5
	[7]	RESERVED	Reserved		
	[10:8]	PRIORITY6_TO_QID	Priority 6 to queue id in 8Pth queue mapping table	R/W	0x6
	[11]	RESERVED	Reserved		
	[14:12]	PRIORITY7_TO_QID	Priority 7 to queue id in 8Pth queue mapping table	R/W	0x7
	[15]	RESERVED	Reserved		

10.10. Scheduler Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0302	[0]	PORT0_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 0 0b0:strict queue type 0b1:WFQ queue type	R/W	0x0
	[1]	PORT0_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 0	R/W	0x0
	[2]	PORT0_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 0	R/W	0x0
	[3]	PORT0_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 0	R/W	0x0
	[4]	PORT0_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 0	R/W	0x0
	[5]	PORT0_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 0	R/W	0x0
	[6]	PORT0_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 0	R/W	0x0
	[7]	PORT0_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 0	R/W	0x0
	[8]	PORT1_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 1	R/W	0x0
	[9]	PORT1_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 1	R/W	0x0
	[10]	PORT1_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 1	R/W	0x0
	[11]	PORT1_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 1	R/W	0x0
	[12]	PORT1_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 1	R/W	0x0
	[13]	PORT1_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 1	R/W	0x0
	[14]	PORT1_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 1	R/W	0x0
	[15]	PORT1_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 1	R/W	0x0
0x0303	[0]	PORT2_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 2	R/W	0x0
	[1]	PORT2_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 2	R/W	0x0
	[2]	PORT2_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 2	R/W	0x0
	[3]	PORT2_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 2	R/W	0x0
	[4]	PORT2_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 2	R/W	0x0

Address	Bit(s)	Name	Description	R/W	Default
	[5]	PORT2_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 2	R/W	0x0
	[6]	PORT2_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 2	R/W	0x0
	[7]	PORT2_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 2	R/W	0x0
	[8]	PORT3_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 3	R/W	0x0
	[9]	PORT3_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 3	R/W	0x0
	[10]	PORT3_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 3	R/W	0x0
	[11]	PORT3_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 3	R/W	0x0
	[12]	PORT3_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 3	R/W	0x0
	[13]	PORT3_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 3	R/W	0x0
	[14]	PORT3_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 3	R/W	0x0
	[15]	PORT3_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 3	R/W	0x0
0x0304	[0]	PORT4_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 4	R/W	0x0
	[1]	PORT4_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 4	R/W	0x0
	[2]	PORT4_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 4	R/W	0x0
	[3]	PORT4_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 4	R/W	0x0
	[4]	PORT4_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 4	R/W	0x0
	[5]	PORT4_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 4	R/W	0x0
	[6]	PORT4_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 4	R/W	0x0
	[7]	PORT4_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 4	R/W	0x0
	[8]	PORT5_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 5	R/W	0x0
	[9]	PORT5_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 5	R/W	0x0
	[10]	PORT5_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 5	R/W	0x0
	[11]	PORT5_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 5	R/W	0x0
	[12]	PORT5_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 5	R/W	0x0
	[13]	PORT5_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 5	R/W	0x0
	[14]	PORT5_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 5	R/W	0x0
	[15]	PORT5_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 5	R/W	0x0
0x0305	[0]	PORT6_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 6	R/W	0x0
	[1]	PORT6_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 6	R/W	0x0
	[2]	PORT6_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 6	R/W	0x0
	[3]	PORT6_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 6	R/W	0x0
	[4]	PORT6_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 6	R/W	0x0
	[5]	PORT6_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 6	R/W	0x0
	[6]	PORT6_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 6	R/W	0x0
	[7]	PORT6_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 6	R/W	0x0
	[8]	PORT7_QUEUE0_TYPE	WFQ or strict queue type in queue 0 of port 7	R/W	0x0
	[9]	PORT7_QUEUE1_TYPE	WFQ or strict queue type in queue 1 of port 7	R/W	0x0
	[10]	PORT7_QUEUE2_TYPE	WFQ or strict queue type in queue 2 of port 7	R/W	0x0
	[11]	PORT7_QUEUE3_TYPE	WFQ or strict queue type in queue 3 of port 7	R/W	0x0
	[12]	PORT7_QUEUE4_TYPE	WFQ or strict queue type in queue 4 of port 7	R/W	0x0
	[13]	PORT7_QUEUE5_TYPE	WFQ or strict queue type in queue 5 of port 7	R/W	0x0
	[14]	PORT7_QUEUE6_TYPE	WFQ or strict queue type in queue 6 of port 7	R/W	0x0
	[15]	PORT7_QUEUE7_TYPE	WFQ or strict queue type in queue 7 of port 7	R/W	0x0

10.11. Weight Fair Queue Parameter Register

Address	Bit(s)	Name	Description	R/W	Default
0x030c	[15:0]	P0_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 0	R/W	0x1
0x030d	[6:0]	P0_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 0	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x030e	[6:0]	P0_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 0	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x030f	[6:0]	P0_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 0	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0310	[6:0]	P0_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 0	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0311	[6:0]	P0_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 0	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0312	[6:0]	P0_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 0	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0313	[6:0]	P0_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 0	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0314	[15:0]	P1_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 1	R/W	0x1
0x0315	[6:0]	P1_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 1	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0316	[6:0]	P1_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 1	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0317	[6:0]	P1_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 1	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0318	[6:0]	P1_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 1	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0319	[6:0]	P1_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 1	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x031a	[6:0]	P1_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 1	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x031b	[6:0]	P1_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 1	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x031c	[15:0]	P2_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 2	R/W	0x1
0x031d	[6:0]	P2_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 2	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x031e	[6:0]	P2_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 2	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x031f	[6:0]	P2_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 2	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0320	[6:0]	P2_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 2	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0321	[6:0]	P2_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 2	R/W	0x1
	[15:7]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
0x0322	[6:0]	P2_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 2	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0323	[6:0]	P2_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 2	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0324	[15:0]	P3_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 3	R/W	0x1
0x0325	[6:0]	P3_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 3	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0326	[6:0]	P3_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 3	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0327	[6:0]	P3_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 3	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0328	[6:0]	P3_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 3	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0329	[6:0]	P3_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 3	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x032a	[6:0]	P3_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 3	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x032b	[6:0]	P3_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 3	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x032c	[15:0]	P4_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 4	R/W	0x1
0x032d	[6:0]	P4_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 4	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x032e	[6:0]	P4_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 4	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x032f	[6:0]	P4_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 4	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0330	[6:0]	P4_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 4	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0331	[6:0]	P4_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 4	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0332	[6:0]	P4_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 4	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0333	[6:0]	P4_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 4	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0334	[15:0]	P5_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 5	R/W	0x1
0x0335	[6:0]	P5_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 5	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0336	[6:0]	P5_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 5	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0337	[6:0]	P5_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 5	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0338	[6:0]	P5_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 5	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0339	[6:0]	P5_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 5	R/W	0x1

Address	Bit(s)	Name	Description	R/W	Default
	[15:7]	RESERVED	Reserved		
0x033a	[6:0]	P5_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 5	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x033b	[6:0]	P5_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 5	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x033c	[15:0]	P6_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 6	R/W	0x1
0x033d	[6:0]	P6_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 6	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x033e	[6:0]	P6_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 6	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x033f	[6:0]	P6_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 6	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0340	[6:0]	P6_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 6	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0341	[6:0]	P6_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 6	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0342	[6:0]	P6_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 6	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0343	[6:0]	P6_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 6	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0344	[15:0]	P7_QUEUE0_WEIGHT	Weight of WFQ in queue 0 port 7	R/W	0x1
0x0345	[6:0]	P7_QUEUE1_WEIGHT	Weight of WFQ in queue 1 port 7	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0346	[6:0]	P7_QUEUE2_WEIGHT	Weight of WFQ in queue 2 port 7	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0347	[6:0]	P7_QUEUE3_WEIGHT	Weight of WFQ in queue 3 port 7	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0348	[6:0]	P7_QUEUE4_WEIGHT	Weight of WFQ in queue 4 port 7	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x0349	[6:0]	P7_QUEUE5_WEIGHT	Weight of WFQ in queue 5 port 7	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x034a	[6:0]	P7_QUEUE6_WEIGHT	Weight of WFQ in queue 6 port 7	R/W	0x1
	[15:7]	RESERVED	Reserved		
0x034b	[6:0]	P7_QUEUE7_WEIGHT	Weight of WFQ in queue 7 port 7	R/W	0x1
	[15:7]	RESERVED	Reserved		

10.12. APR Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x030a	[0]	PORT0_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0

	[1]	PORT1_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0
	[2]	PORT2_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0
	[3]	PORT3_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0
	[4]	PORT4_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0
	[5]	PORT5_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0
	[6]	PORT6_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0
	[7]	PORT7_APR_ENABLE	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	R/W	0
	[15:8]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
0x03ac	[2:0]	PORT0_QUEUE0_APR_METER	APR meter index of PORT 0 Queue 0.The shared meter index (16*n+PORTn_QUEUEm_APR_METER) will be used for this leaky bucket	R/W	0
	[5:3]	PORT0_QUEUE1_APR_METER	APR meter index of PORT 0 Queue 1	R/W	0
	[8:6]	PORT0_QUEUE2_APR_METER	APR meter index of PORT 0 Queue 2	R/W	0
	[11:9]	PORT0_QUEUE3_APR_METER	APR meter index of PORT 0 Queue 3	R/W	0
	[14:12]	PORT0_QUEUE4_APR_METER	APR meter index of PORT 0 Queue 4	R/W	0
	[15]	RESERVED	Reserved		
0x03ad	[2:0]	PORT0_QUEUE5_APR_METER	APR meter index of PORT 0 Queue 5	R/W	0
	[5:3]	PORT0_QUEUE6_APR_METER	APR meter index of PORT 0 Queue 6	R/W	0
	[8:6]	PORT0_QUEUE7_APR_METER	APR meter index of PORT 0 Queue 7	R/W	0
	[15:9]	RESERVED	Reserved		
0x03b0		P1_APR_METER0	Same as 0x03ac		
0x03b1		P1_APR_METER1	Same as 0x03ad		
0x03b4		P2_APR_METER0	Same as 0x03ac		
0x03b5		P2_APR_METER1	Same as 0x03ad		
0x03b8		P3_APR_METER0	Same as 0x03ac		
0x03b9		P3_APR_METER1	Same as 0x03ad		
0x03bc		P4_APR_METER0	Same as 0x03ac		
0x03bd		P4_APR_METER1	Same as 0x03ad		
0x03c0		P5_APR_METER0	Same as 0x03ac		

0x03c1		P5_APR_METER1	Same as 0x03ad		
0x03c4		P6_APR_METER0	Same as 0x03ac		
0x03c5		P6_APR_METER1	Same as 0x03ad		
0x03c8		P7_APR_METER0	Same as 0x03ac		
0x03c9		P7_APR_METER1	Same as 0x03ad		

11. PHY

11.1. PHY Access Control Registers

Reg.	Bits	Name	Description	R/W	Default
0x1f00	[0]	PHYCMD	PHY registers access command	R/W	0
	[1]	RW	0b0:Read command 0b1:Write command	R/W	0
	[15:2]	RESERVED	Reserved		
0x1f01	[1:0]	RESERVED	Reserved		
	[2]	PHY_BUSY	Access to internal PHY is under running.	R/O	0x0
	[15:3]	RESERVED	Reserved		
0x1f02	[15:0]	ADDRESS	Indirect access address.	R/W	0x0
0x1f03	[15:0]	PHYWDATA	PHY register write access data	R/W	0x0
0x1f04	[15:0]	PHYRDATA	PHY register read access data	R/W	0x0

11.2. PHY Registers

Reg.	Bits	Name	Description	R/W	Default
0x2020	[15:0]	PHY0REG0	PHY Control	R/W	0
0x2021	[15:0]	PHY0REG1	PHY Status	R/W	0
0x2022	[15:0]	PHY0REG2	PHY Identifier 1	R/W	0
0x2023	[15:0]	PHY0REG3	PHY Identifier 2	R/W	0
0x2024	[15:0]	PHY0REG4	Auto-Negotiation Advertisement	R/W	0
0x2025	[15:0]	PHY0REG5	Auto-Negotiation Link Partner Ability	R/W	0
0x2026	[15:0]	PHY0REG6	Auto-Negotiation Expansion	R/W	0
0x2027	[15:0]	PHY0REG7	Auto-Negotiation Page Transmit Register	R/W	0
0x2028	[15:0]	PHY0REG8	Auto-Negotiation Link Partner Next Page Register	R/W	0
0x2029	[15:0]	PHY0REG9	1000Base-T Control Register	R/W	0
0x202a	[15:0]	PHY0REG10	1000Base-T Status Register	R/W	0
0x2040 0x204a		PHY1REG0 ~ PHY1REG10	Same as PHY0 registers		
0x2080 0x208a		PHY2REG0 ~ PHY2REG10	Same as PHY0 registers		
0x2100 0x210a		PHY3REG0 ~ PHY3REG10	Same as PHY0 registers		
0x2200 0x220a		PHY4REG0 ~ PHY4REG10	Same as PHY0 registers		
0x2400 0x240a		PHY5REG0 ~ PHY5REG10	Same as PHY0 registers		
0x2800 0x280a		PHY6REG0 ~ PHY6REG10	Same as PHY0 registers		

0x3000 0x300a		PHY7REG0 ~ PHY7REG10	Same as PHY0 registers		

12. MIB

12.1. MIB Control Register

Address.	Bit(s)	Name	Description	R/W	Default
0x1000	[15:0]	MIB_COUNTER0	SRAM data[15:0]	R/O	0x0
0x1001	[15:0]	MIB_COUNTER1	SRAM data[31:16]	R/O	0x0
0x1002	[15:0]	MIB_COUNTER2	SRAM data[47:32]	R/O	0x0
0x1003	[15:0]	MIB_COUNTER3	SRAM data[63:48]	R/O	0x0
0x1004	[8:0]	MIB_ADDRESS	SRAM address for watching MIB data	WO	0x0
	[15:9]	RESERVED	Reserved		
0x1005	[0]	BUSY_FLAG	ASIC is accessing MIB	R/O	0x0
	[1]	RESET_FLAG	ASIC is resetting MIB	R/O	0x0
	[2]	PORT0_RESET	Port 0 MIB reset	R/W	0x0
	[3]	PORT1_RESET	Port 1 MIB reset	R/W	0x0
	[4]	PORT2_RESET	Port 2 MIB reset	R/W	0x0
	[5]	PORT3_RESET	Port 3 MIB reset	R/W	0x0
	[6]	PORT4_RESET	Port 4 MIB reset	R/W	0x0
	[7]	PORT5_RESET	Port 5 MIB reset	R/W	0x0
	[8]	PORT6_RESET	Port 6 MIB reset	R/W	0x0
	[9]	PORT7_RESET	Port 7 MIB reset	R/W	0x0
	[10]	QM_RESET	enable resetting outq MIB counters 0b0:disable 0b1:enable output queue related MIB resetting	R/W	0x0
	[11]	GLOBAL_RESET	enable resetting Global MIB counters 0b0:disable 0b1:enable all MIB resetting	R/W	0x0
	[15:12]	RESERVED	Reserved		

12.2. MIB Data Register

Address	Name	Bits
0	P0_ifInOctets	[63:0]
1	P0_dot3StatsFCSErrors	[31:0]
1	P0_dot3StatsSymbolErrors	[63:32]
2	P0_dot3InPauseFrames	[31:0]
2	P0_dot3ControlInUnknownOpcodes	[63:32]
3	P0_etherFregament	[31:0]
3	P0_etherStatsJabbers	[63:32]
4	P0_ifInUcastPkts	[31:0]
4	P0_etherStatsDropEvents	[63:32]
5	P0_ ifInMulticastPkts	[31:0]

5	P0_ifInBroadcastPkts	[63:32]
6	P0_InMldChecksumError	[31:0]
6	P0_InIgmpChecksumError	[63:32]
7	P0_InMldSpecificQuery	[31:0]
7	P0_InMldGeneralQuery	[63:32]
8	P0_InIgmpSpecificQuery	[31:0]
8	P0_InIgmpGeneralQuery	[63:32]
9	P0_InMldLeaves	[31:0]
9	P0_InIgmpInterfaceLeaves	[63:32]
10	P0_etherStatsOctets	[63:0]
11	P0_etherStatsUnderSizePkts	[31:0]
11	P0_etherOversizeStats	[63:32]
12	P0_etherStatsPkts64Octets	[31:0]
12	P0_etherStatsPkts65to127Octets	[63:32]
13	P0_etherStatsPkts128to255Octets	[31:0]
13	P0_etherStatsPkts256to511Octets	[63:32]
14	P0_etherStatsPkts512to1023Octets	[31:0]
14	P0_etherStatsPkts1024to1518Octets	[63:32]
15	P0_ifOutOctets	[63:0]
16	P0_dot3StatsSingleCollisionFrames	[31:0]
16	P0_dot3StatMultipleCollisionFrames	[63:32]
17	P0_dot3sDeferredTransmissions	[31:0]
17	P0_dot3StatsLateCollisions	[63:32]
18	P0_etherStatsCollisions	[31:0]
18	P0_Dot3StatsExcessiveCollisions	[63:32]
19	P0_dot3OutPauseFrames	[31:0]
19	P0_ifOutDiscards	[63:32]
20	P0_dot1dTpPortInDiscards	[31:0]
20	P0_ifOutUcastPkts	[63:32]
21	P0_ifOutMulticastPkts	[31:0]
21	P0_ifOutBroadcastPkts	[63:32]
22	P0_OutOampduPkts	[31:0]
22	P0_InOampduPkts	[63:32]
23	P0_InIgmpJoinsSuccess	[31:0]
23	P0_InIgmpJoinsFail	[63:32]
24	P0_InMldJoinsSuccess	[31:0]
24	P0_InMldJoinsFail	[63:32]
25	P0_InReportSuppressionDrop	[31:0]
25	P0_InLeaveSuppressionDrop	[63:32]
26	P0_OutIgmpReports	[31:0]
26	P0_OutIgmpLeaves	[63:32]
27	P0_OutIgmpGeneralQuery	[31:0]
27	P0_OutIgmpSpecificQuery	[63:32]
28	P0_OutMldReports	[31:0]
28	P0_OutMldLeaves	[63:32]

29	P0_OutMldGeneralQuery	[31:0]
29	P0_OutMldSpecificQuery	[63:32]
30	P0_InKnownMulticastPkts	[31:0]
30	N/A	[63:32]
31 ~ 60	Same MIBs data in Port 1 as port 0	
61 ~ 90	Same MIBs data in Port 2 as port 0	
91 ~ 120	Same MIBs data in Port 3 as port 0	
121 ~ 150	Same MIBs data in Port 4 as port 0	
151 ~ 180	Same MIBs data in Port 5 as port 0	
181 ~ 210	Same MIBs data in Port 6 as port 0	
211 ~ 240	Same MIBs data in Port 7 as port 0	

13. LUT

13.1. LUT Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0a30	[2:0]	AGE_TIMER	Lookup table aging timer for auto-learning entry. ASIC will set AGE field of auto-learning by this register.	R/W	0x6
	[3]	RESERVED	Reserved		
	[4]	IPMCAST_LOOKUP	Hash algorithm for incoming IP multicast packet to lookup forwarding decision 0b0:using {DMAC,FID} hash algorithm 0b1:using {DIP,SIP} hash algorithm	R/W	0
	[5]	LINKDOWN_AGEOUT	Link down port aging out setting 0b0:enable force aging out all L2 lookup entries belong to link down ports 0b1:disable aging out	R/W	0
	[6]	BCAM_DISABLE	Binary CAM usage setting 0b0:enable 0b1:disable	R/W	0
	[7]	RESERVED	Reserved		
	[9:8]	AGE_SPEED	L2 lookup table aging speed/period for each 8K entries 0x0: 14.3 second 0x1: 28.6 second 0x2: 57.2 second 0x3: 1.9 minute	R/W	0x2
	[15:10]	RESERVED	Reserved		
0x0a31	[7:0]	LUT_AGEOUT_CRTL	per port aging out enable/disable setting 0b0:enable aging out 0b1:disable aging out	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a36	[7:0]	FORCE_FLUSH	Per-port L2 entries flush portmask, ASIC will clear it atfer finish flushing	R/W	0x0
	[15:8]	BUSY_STATUS	L2 Flush state 0b1:Busy 0b0:Normal	RO	

13.2. LUT Learn Limit Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x08c8	[1:0]	UNKNOW_SA_BEHAVE	Drop/Trap packet if SA is unknown 0b00: normal 0b01: drop packet & disable learning 0b10: trap to CPU 0b11: copy to 8051	R/W	0x0

	[3:2]	UNMATCHED_SA_BEHAVE	Drop/Trap packet if SA is not from the same source port as L2 SPA 0b00: normal 0b01: drop packet & disable learning 0b10: trap to CPU 0b11: copy to 8051	R/W	0x0
	[5:4]	LUT_LEARN_OVER_ACT	Auto leaning number exceed behavior 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: reserved	R/W	0x0
	[7:6]	UNKNOWN_UNICAST_DA_BEHAVE	Drop/Trap packet if unicast DA is unknown 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: reserved	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a20	[11:0]	PORT0_LEARN_LIMITNO	Port 0 L2 learning limitation entry number. ASIC supports 8K LUT entries and L2 learning limitation is for auto-learning L2 entry number. Set register to value 0x3FFF for non-limitation.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a21	[11:0]	PORT1_LEARN_LIMITNO	Port 1 L2 learning limitation entry number.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a22	[11:0]	PORT2_LEARN_LIMITNO	Port 2 L2 learning limitation entry number.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a23	[11:0]	PORT3_LEARN_LIMITNO	Port 3 L2 learning limitation entry number.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a24	[11:0]	PORT4_LEARN_LIMITNO	Port 4 L2 learning limitation entry number.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a25	[11:0]	PORT5_LEARN_LIMITNO	Port 5 L2 learning limitation entry number.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a26	[11:0]	PORT6_LEARN_LIMITNO	Port 6 L2 learning limitation entry number.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a27	[11:0]	PORT7_LEARN_LIMITNO	Port 7 L2 learning limitation entry number.	R/W	0x0840
	[15:12]	RESERVED	Reserved		
0x0a87	[11:0]	L2_PORT0_LRN_CNT	Number of SA learned on Port 0	R/O	0x0
	[15:12]	RESERVED	Reserved		
0x0a88	[11:0]	L2_PORT1_LRN_CNT	Number of SA learned on Port 1	R/O	0x0
	[15:12]	RESERVED	Reserved		
0x0a89	[11:0]	L2_PORT2_LRN_CNT	Number of SA learned on Port 2	R/O	0x0
	[15:12]	RESERVED	Reserved		
0x0a8a	[11:0]	L2_PORT3_LRN_CNT	Number of SA learned on Port 3	R/O	0x0
	[15:12]	RESERVED	Reserved		
0x0a8b	[11:0]	L2_PORT4_LRN_CNT	Number of SA learned on Port 4	R/O	0x0
	[15:12]	RESERVED	Reserved		
0x0a8c	[11:0]	L2_PORT5_LRN_CNT	Number of SA learned on Port 5	R/O	0x0
	[15:12]	RESERVED	Reserved		

0x0a8d	[11:0]	L2_PORT6_LRN_CNT	Number of SA learned on Port 6	R/O	0x0
	[15:12]	RESERVED	Reserved		
0x0a8e	[11:0]	L2_PORT7_LRN_CNT	Number of SA learned on Port 7	R/O	0x0
	[15:12]	RESERVED	Reserved		

14. Port Isolation

14.1. Port Isolation Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x08a2	[7:0]	PORT0_MASK	Port0 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08a3	[7:0]	PORT1_MASK	Port1 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08a4	[7:0]	PORT2_MASK	Port2 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08a5	[7:0]	PORT3_MASK	Port3 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08a6	[7:0]	PORT4_MASK	Port4 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08a7	[7:0]	PORT5_MASK	Port5 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08a8	[7:0]	PORT6_MASK	Port6 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08a9	[7:0]	PORT7_MASK	Port7 L2 Force portmask Control Register	R/W	0xFF
	[15:8]	RESERVED	Reserved		

14.2. Enhance FID Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0a32	[2:0]	PORT0_EFID	Enhanced filtering database ID for PORT 0	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT1_EFID	Enhanced filtering database ID for PORT 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT2_EFID	Enhanced filtering database ID for PORT 2	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT3_EFID	Enhanced filtering database ID for PORT 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x0a33	[2:0]	PORT4_EFID	Enhanced filtering database ID for PORT 4	R/W	0x0
	[3]	RESERVED	Reserved		
	[6:4]	PORT5_EFID	Enhanced filtering database ID for PORT 5	R/W	0x0
	[7]	RESERVED	Reserved		
	[10:8]	PORT6_EFID	Enhanced filtering database ID for PORT 6	R/W	0x0
	[11]	RESERVED	Reserved		
	[14:12]	PORT7_EFID	Enhanced filtering database ID for PORT 7	R/W	0x0
	[15]	RESERVED	Reserved		

15. SVLAN

15.1. SVLAN Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0e80	[1:0]	VS_SPRISEL	S-priority assignment of upstream packet setting 0b00: use internal priority 0b01: use 1Q tag priority 0b10: use VS_SPRI as S-Priority 0b11: using port based priority	R/W	0x0
	[3:2]	VS_UNTAG	un-stagged packet with trap to CPU action 0b00:drop 0b01: trap to CPU 0b10: assign ingress SVID as VS_UNTAG_SVIDX 0b11: reserved	R/W	0x0
	[5:4]	VS_UNMAT	Unmatched SVID packet with trap to CPU action 0b00:drop 0b01: trap to CPU 0b10: assign ingress SVID as VS_UNMAT_SVIDX 0b11: assign ingress SVID as VS_UNMAT_SVIDX and keep original SVLAN format	R/W	0x0
	[6]	VS_UIFSEG	Uplink stream frame without egressing SVID assignment trapping to CPU action 0b0: using default egress SVLAN configuration in VS_CPSVIDX 0b1: Trap to CPU	R/W	0x0
	[7]	VS_PORT0_DMACVIDSEL	Per egress port 0 Dmac CVID decision	R/W	0x0
	[8]	VS_PORT1_DMACVIDSEL	Per egress port 1 Dmac CVID decision	R/W	0x0
	[9]	VS_PORT2_DMACVIDSEL	Per egress port 2 Dmac CVID decision	R/W	0x0
	[10]	VS_PORT3_DMACVIDSEL	Per egress port 3 Dmac CVID decision	R/W	0x0
	[11]	VS_PORT4_DMACVIDSEL	Per egress port 4 Dmac CVID decision	R/W	0x0
	[12]	VS_PORT5_DMACVIDSEL	Per egress port 5 Dmac CVID decision	R/W	0x0
	[13]	VS_PORT6_DMACVIDSEL	Per egress port 6 Dmac CVID decision	R/W	0x0
	[14]	VS_PORT7_DMACVIDSEL	Per egress port 7 Dmac CVID decision	R/W	0x0
	[15]	RESERVED	Reserved	R/W	
0x1202	[15:0]	VS_TPID	SVLAN TPID configuration	R/W	0x88A8
0x1218	[7:0]	SVLAN_UPLINK_PORTMASK	SVLAN uplink port mask	R/W	0x0
	[15:8]	RESERVED	Reserved		

15.2. SVLAN Member Configuration Register

Address	Bit(s)	Name	Description	R/W	Default
0x0c01	[7:0]	VS_UNTAGSET	SVLAN untag set	R/W	0x0
	[15:8]	VS_SMBR	Port member of received S-tag packet which SVID is the same as this configuration entry 0	R/W	0x0
0x0c02	[3:0]	VS_FID_MSTI	Filtering Database/ Multiple Spanning Tree Instance for accepted S-VID	R/W	0x0
	[6:4]	VS_SPRI	SVLAN priroity assignment of received S-tag packet which SVID is the same as this configuration entry 0	R/W	0x0
	[7]	VS_FIDEN	Force FID from SVLAN	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0c03	[11:0]	VS_SVID	SVID of received S-tag packet which SVID is the same as this configuration entry 0	R/W	0x0
	[12]	VS_EFIDEN	Usage EFID setting of received S-tag packet which SVID is the same as this configuration entry 0 0b0:disable 0b1:enable	R/W	0x0
	[15:13]	VS_EFID	EFID of received S-tag packet which SVID is the same as this configuration entry 0	R/W	0x0
0x0c04~ 0x0c06			SVLAN member configuration entry 1, the register definition is the same as entry 0.	R/W	0x0
0x0c07~ 0x0c09			SVLAN member configuration entry 2, the register definition is the same as entry 0.	R/W	0x0
0x0c0a~ 0x0c0c			SVLAN member configuration entry 3, the register definition is the same as entry 0.	R/W	0x0
0x0c0d~ 0x0c0f			SVLAN member configuration entry 4, the register definition is the same as entry 0.	R/W	0x0
0x0c10~ 0x0c12			SVLAN member configuration entry 5, the register definition is the same as entry 0.	R/W	0x0
0x0c13~ 0x0c15			SVLAN member configuration entry 6, the register definition is the same as entry 0.	R/W	0x0
0x0c16~ 0x0c18			SVLAN member configuration entry 7, the register definition is the same as entry 0.	R/W	0x0
0x0c19~ 0x0c1b			SVLAN member configuration entry 8, the register definition is the same as entry 0.	R/W	0x0
0x0c1c~ 0x0c1e			SVLAN member configuration entry 9, the register definition is the same as entry 0.	R/W	0x0
0x0c1f~ 0x0c21			SVLAN member configuration entry 10, the register definition is the same as entry 0.	R/W	0x0
0x0c22~ 0x0c24			SVLAN member configuration entry 11, the register definition is the same as entry 0.	R/W	0x0
0x0c25~ 0x0c27			SVLAN member configuration entry 12, the register definition is the same as entry 0.	R/W	0x0
0x0c28~ 0x0c2a			SVLAN member configuration entry 13, the register definition is the same as entry 0.	R/W	0x0
0x0c2b~ 0x0c2d			SVLAN member configuration entry 14, the register definition is the same as entry 0.	R/W	0x0

0x0c2e~ 0x0c30			SVLAN member configuration entry 15, the register definition is the same as entry 0.	R/W	0x0
0x0c31~ 0x0c33			SVLAN member configuration entry 16, the register definition is the same as entry 0.	R/W	0x0
0x0c34~ 0x0c36			SVLAN member configuration entry 17, the register definition is the same as entry 0.	R/W	0x0
0x0c37~ 0x0c39			SVLAN member configuration entry 18, the register definition is the same as entry 0.	R/W	0x0
0x0c3a~ 0x0c3c			SVLAN member configuration entry 19, the register definition is the same as entry 0.	R/W	0x0
0x0c3d~ 0x0c3f			SVLAN member configuration entry 20, the register definition is the same as entry 0.	R/W	0x0
0x0c40~ 0x0c42			SVLAN member configuration entry 21, the register definition is the same as entry 0.	R/W	0x0
0x0c43~ 0x0c45			SVLAN member configuration entry 22, the register definition is the same as entry 0.	R/W	0x0
0x0c46~ 0x0c48			SVLAN member configuration entry 23, the register definition is the same as entry 0.	R/W	0x0
0x0c49~ 0x0c4b			SVLAN member configuration entry 24, the register definition is the same as entry 0.	R/W	0x0
0x0c4c~ 0x0c4e			SVLAN member configuration entry 25, the register definition is the same as entry 0.	R/W	0x0
0x0c4f~ 0x0c51			SVLAN member configuration entry 26, the register definition is the same as entry 0.	R/W	0x0
0x0c52~ 0x0c54			SVLAN member configuration entry 27, the register definition is the same as entry 0.	R/W	0x0
0x0c55~ 0x0c57			SVLAN member configuration entry 28, the register definition is the same as entry 0.	R/W	0x0
0x0c58~ 0x0c5a			SVLAN member configuration entry 29, the register definition is the same as entry 0.	R/W	0x0
0x0c5b~ 0x0c5d			SVLAN member configuration entry 30, the register definition is the same as entry 0.	R/W	0x0
0x0c5e~ 0x0c60			SVLAN member configuration entry 31, the register definition is the same as entry 0.	R/W	0x0
0x0c61~ 0x0c63			SVLAN member configuration entry 32, the register definition is the same as entry 0.	R/W	0x0
0x0c64~ 0x0c66			SVLAN member configuration entry 33, the register definition is the same as entry 0.	R/W	0x0
0x0c67~ 0x0c69			SVLAN member configuration entry 34, the register definition is the same as entry 0.	R/W	0x0
0x0c6a~ 0x0c6c			SVLAN member configuration entry 35, the register definition is the same as entry 0.	R/W	0x0
0x0c6d~ 0x0c6f			SVLAN member configuration entry 36, the register definition is the same as entry 0.	R/W	0x0
0x0c70~ 0x0c72			SVLAN member configuration entry 37, the register definition is the same as entry 0.	R/W	0x0
0x0c73~ 0x0c75			SVLAN member configuration entry 38, the register definition is the same as entry 0.	R/W	0x0

0x0c76~ 0x0c78			SVLAN member configuration entry 39, the register definition is the same as entry 0.	R/W	0x0
0x0c79~ 0x0c7b			SVLAN member configuration entry 40, the register definition is the same as entry 0.	R/W	0x0
0x0c7c~ 0x0c7e			SVLAN member configuration entry 41, the register definition is the same as entry 0.	R/W	0x0
0x0c7f~ 0x0c81			SVLAN member configuration entry 42, the register definition is the same as entry 0.	R/W	0x0
0x0c82~ 0x0c84			SVLAN member configuration entry 43, the register definition is the same as entry 0.	R/W	0x0
0x0c85~ 0x0c87			SVLAN member configuration entry 44, the register definition is the same as entry 0.	R/W	0x0
0x0c88~ 0x0c8a			SVLAN member configuration entry 45, the register definition is the same as entry 0.	R/W	0x0
0x0c8b~ 0x0c8d			SVLAN member configuration entry 46, the register definition is the same as entry 0.	R/W	0x0
0x0c8e~ 0x0c90			SVLAN member configuration entry 47, the register definition is the same as entry 0.	R/W	0x0
0x0c91~ 0x0c93			SVLAN member configuration entry 48, the register definition is the same as entry 0.	R/W	0x0
0x0c94~ 0x0c96			SVLAN member configuration entry 49, the register definition is the same as entry 0.	R/W	0x0
0x0c97~ 0x0c99			SVLAN member configuration entry 50, the register definition is the same as entry 0.	R/W	0x0
0x0c9a~ 0x0c9c			SVLAN member configuration entry 51, the register definition is the same as entry 0.	R/W	0x0
0x0c9d~ 0x0c9f			SVLAN member configuration entry 52, the register definition is the same as entry 0.	R/W	0x0
0x0ca0~ 0x0ca2			SVLAN member configuration entry 53, the register definition is the same as entry 0.	R/W	0x0
0x0ca3~ 0x0ca5			SVLAN member configuration entry 54, the register definition is the same as entry 0.	R/W	0x0
0x0ca6~ 0x0ca8			SVLAN member configuration entry 55, the register definition is the same as entry 0.	R/W	0x0
0x0ca9~ 0x0cab			SVLAN member configuration entry 56, the register definition is the same as entry 0.	R/W	0x0
0x0cac~ 0x0cae			SVLAN member configuration entry 57, the register definition is the same as entry 0.	R/W	0x0
0x0caf~ 0x0cb1			SVLAN member configuration entry 58, the register definition is the same as entry 0.	R/W	0x0
0x0cb2~ 0x0cb4			SVLAN member configuration entry 59, the register definition is the same as entry 0.	R/W	0x0
0x0cb5~ 0x0cb7			SVLAN member configuration entry 60, the register definition is the same as entry 0.	R/W	0x0
0x0cb8~ 0x0cba			SVLAN member configuration entry 61, the register definition is the same as entry 0.	R/W	0x0
0x0cbb~ 0x0cbd			SVLAN member configuration entry 62, the register definition is the same as entry 0.	R/W	0x0

0x0cbe~ 0x0cc0			SVLAN member configuration entry 63, the register definition is the same as entry 0.	R/W	0x0

15.3. SVLAN C2S Configuration Register

Address	Bit(s)	Name	Description	R/W	Default
0x0d00	[5:0]	SVIDX	SVLAN member configuration index of uplink port egressing packts which ingress Enhanced VID is matched to C2S configuration entry 0	R/W	0x0
	[15:6]	RESERVED	Reserved		
0x0d01	[7:0]	C2SENPMSK	Port member to assign egress SVID which packet ingressing Enhanced VID is matched to C2S configuration entry 0	R/W	0x0
	[15:0]	RESERVED	Reserved		
0x0d02	[12:0]	EVID	Ingressing Enhanced VID of C2S configuration entry 0	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x0d03~ 0x0d05			SVLAN C2S configuration entry 1, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d06~ 0x0d08			SVLAN C2S configuration entry 2, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d09~ 0x0d0b			SVLAN C2S configuration entry 3, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d0c~ 0x0d0e			SVLAN C2S configuration entry 4, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d0F~ 0x0d11			SVLAN C2S configuration entry 5, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d12~ 0x0d14			SVLAN C2S configuration entry 6, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d15~ 0x0d17			SVLAN C2S configuration entry 7, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d18~ 0x0d1a			SVLAN C2S configuration entry 8, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d1b~ 0x0d1d			SVLAN C2S configuration entry 9, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d1e~ 0x0d20			SVLAN C2S configuration entry 10, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d21~ 0x0d23			SVLAN C2S configuration entry 11, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d24~ 0x0d26			SVLAN C2S configuration entry 12, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d27~ 0x0d29			SVLAN C2S configuration entry 13, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d2a~ 0x0d2c			SVLAN C2S configuration entry 14, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d2d~ 0x0d2f			SVLAN C2S configuration entry 15, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0

0x0d30~ 0x0d32			SVLAN C2S configuration entry 16, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d33~ 0x0d35			SVLAN C2S configuration entry 17, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d36~ 0x0d38			SVLAN C2S configuration entry 18, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d39~ 0x0d3b			SVLAN C2S configuration entry 19, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d3c~ 0x0d3e			SVLAN C2S configuration entry 20, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d3f~ 0x0d41			SVLAN C2S configuration entry 21, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d42~ 0x0d44			SVLAN C2S configuration entry 22, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d45~ 0x0d47			SVLAN C2S configuration entry 23, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d48~ 0x0d4a			SVLAN C2S configuration entry 24, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d4b~ 0x0d4d			SVLAN C2S configuration entry 25, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d4e~ 0x0d50			SVLAN C2S configuration entry 26, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d51~ 0x0d53			SVLAN C2S configuration entry 27, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d54~ 0x0d56			SVLAN C2S configuration entry 28, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d57~ 0x0d59			SVLAN C2S configuration entry 29, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d5a~ 0x0d5c			SVLAN C2S configuration entry 30, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d5d~ 0x0d5f			SVLAN C2S configuration entry 31, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d60~ 0x0d62			SVLAN C2S configuration entry 32, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d63~ 0x0d65			SVLAN C2S configuration entry 33, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d66~ 0x0d68			SVLAN C2S configuration entry 34, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d69~ 0x0d6b			SVLAN C2S configuration entry 35, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d6c~ 0x0d6e			SVLAN C2S configuration entry 36, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d6f~ 0x0d71			SVLAN C2S configuration entry 37, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d72~ 0x0d74			SVLAN C2S configuration entry 38, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d75~ 0x0d77			SVLAN C2S configuration entry 39, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0

0x0d78~ 0x0d7a			SVLAN C2S configuration entry 40, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d7b~ 0x0d7d			SVLAN C2S configuration entry 41, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d7e~ 0x0d80			SVLAN C2S configuration entry 42, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d81~ 0x0d83			SVLAN C2S configuration entry 43, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d84~ 0x0d86			SVLAN C2S configuration entry 44, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d87~ 0x0d89			SVLAN C2S configuration entry 45, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d8a~ 0x0d8c			SVLAN C2S configuration entry 46, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d8d~ 0x0d8f			SVLAN C2S configuration entry 47, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d90~ 0x0d92			SVLAN C2S configuration entry 48, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d93~ 0x0d95			SVLAN C2S configuration entry 49, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d96~ 0x0d98			SVLAN C2S configuration entry 50, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d99~ 0x0d9b			SVLAN C2S configuration entry 51, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d9c~ 0x0d9e			SVLAN C2S configuration entry 52, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0d9f~ 0x0da1			SVLAN C2S configuration entry 53, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0da2~ 0x0da4			SVLAN C2S configuration entry 54, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0da5~ 0x0da7			SVLAN C2S configuration entry 55, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0da8~ 0x0daa			SVLAN C2S configuration entry 56, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dab~ 0x0dad			SVLAN C2S configuration entry 57, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dae~ 0x0db0			SVLAN C2S configuration entry 58, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0db1~ 0x0db3			SVLAN C2S configuration entry 59, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0db4~ 0x0db6			SVLAN C2S configuration entry 60, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0db7~ 0x0db9			SVLAN C2S configuration entry 61, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dba~ 0x0dbc			SVLAN C2S configuration entry 62, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dbd~ 0x0dbf			SVLAN C2S configuration entry 63, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0

0x0dc0~ 0x0dc2			SVLAN C2S configuration entry 64, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dc3~ 0x0dc5			SVLAN C2S configuration entry 65, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dc6~ 0x0dc8			SVLAN C2S configuration entry 66, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dc9~ 0x0dcb			SVLAN C2S configuration entry 67, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dcc~ 0x0dce			SVLAN C2S configuration entry 68, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dcf~ 0x0dd1			SVLAN C2S configuration entry 69, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dd2~ 0x0dd4			SVLAN C2S configuration entry 70, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dd5~ 0x0dd7			SVLAN C2S configuration entry 71, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dd8~ 0x0dda			SVLAN C2S configuration entry 72, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0ddb~ 0x0ddd			SVLAN C2S configuration entry 73, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dde~ 0x0de0			SVLAN C2S configuration entry 74, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0de1~ 0x0de3			SVLAN C2S configuration entry 75, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0de4~ 0x0de6			SVLAN C2S configuration entry 76, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0de7~ 0x0de9			SVLAN C2S configuration entry 77, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dea~ 0x0dec			SVLAN C2S configuration entry 78, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0ded~ 0x0def			SVLAN C2S configuration entry 79, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0df0~ 0x0df2			SVLAN C2S configuration entry 80, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0df3~ 0x0df5			SVLAN C2S configuration entry 81, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0df6~ 0x0df8			SVLAN C2S configuration entry 82, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0df9~ 0x0dfb			SVLAN C2S configuration entry 83, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dfc~ 0x0dfe			SVLAN C2S configuration entry 84, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0dff~ 0x0e01			SVLAN C2S configuration entry 85, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e02~ 0x0e04			SVLAN C2S configuration entry 86, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e05~ 0x0e07			SVLAN C2S configuration entry 87, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0

0x0e08~ 0x0e0a			SVLAN C2S configuration entry 88, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e0b~ 0x0e0d			SVLAN C2S configuration entry 89, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e0e~ 0x0e10			SVLAN C2S configuration entry 90, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e11~ 0x0e13			SVLAN C2S configuration entry 91, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e14~ 0x0e16			SVLAN C2S configuration entry 92, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e17~ 0x0e19			SVLAN C2S configuration entry 93, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e1a~ 0x0e1c			SVLAN C2S configuration entry 94, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e1d~ 0x0e1f			SVLAN C2S configuration entry 95, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e20~ 0x0e22			SVLAN C2S configuration entry 96, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e23~ 0x0e25			SVLAN C2S configuration entry 97, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e26~ 0x0e28			SVLAN C2S configuration entry 98, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e29~ 0x0e2b			SVLAN C2S configuration entry 99, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e2c~ 0x0e2e			SVLAN C2S configuration entry 100, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e2f~ 0x0e31			SVLAN C2S configuration entry 101, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e32~ 0x0e34			SVLAN C2S configuration entry 102, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e35~ 0x0e37			SVLAN C2S configuration entry 103, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e38~ 0x0e3a			SVLAN C2S configuration entry 104, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e3b~ 0x0e3d			SVLAN C2S configuration entry 105, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e3e~ 0x0e40			SVLAN C2S configuration entry 106, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e41~ 0x0e43			SVLAN C2S configuration entry 107, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e44~ 0x0e46			SVLAN C2S configuration entry 108, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e47~ 0x0e49			SVLAN C2S configuration entry 109, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e4a~ 0x0e4c			SVLAN C2S configuration entry 110, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e4d~ 0x0e4f			SVLAN C2S configuration entry 111, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0

0x0e50~ 0x0e52			SVLAN C2S configuration entry 112, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e53~ 0x0e55			SVLAN C2S configuration entry 113, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e56~ 0x0e58			SVLAN C2S configuration entry 114, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e59~ 0x0e5b			SVLAN C2S configuration entry 115, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e5c~ 0x0e5e			SVLAN C2S configuration entry 116, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e5f~ 0x0e61			SVLAN C2S configuration entry 117, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e62~ 0x0e64			SVLAN C2S configuration entry 118, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e65~ 0x0e67			SVLAN C2S configuration entry 119, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e68~ 0x0e6a			SVLAN C2S configuration entry 120, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e6b~ 0x0e6d			SVLAN C2S configuration entry 121, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e6e~ 0x0e70			SVLAN C2S configuration entry 122, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e71~ 0x0e73			SVLAN C2S configuration entry 123, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e74~ 0x0e76			SVLAN C2S configuration entry 124, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e77~ 0x0e79			SVLAN C2S configuration entry 125, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e7a~ 0x0e7c			SVLAN C2S configuration entry 126, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0
0x0e7d~ 0x0e7f			SVLAN C2S configuration entry 127, the definition of registers is the same as SVLAN C2S entry 0	R/W	0x0

15.4. SVLAN MC2S Configuration Register

Address	Bit(s)	Name	Description	R/W	Default
0x0b00	[5:0]	SVIDX	SVLAN member configuration index of uplink port egressing packt which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0	R/W	0x0
	[6]	FORMAT	Compare data format of uplink port egressing packt which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0 0b0: compare data is DMAC[31:0] 0b1: compare data is IPv4 DIP	R/W	0x0
	[7]	VALID	Valid setting of MC2S configuration entry 0 0b0:not vaild 0b1:valid	R/W	0x0

	[15:8]	RESERVED	Reserved		
0x0b01	[15:0]	MASK_0	Compare destination mac/IP address mask[15:0] of uplink port egressing packt which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0	R/W	0x0
0x0b02	[15:0]	MASK_1	Compare destination mac/IP address mask[31:16] of uplink port egressing packt which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0	R/W	0x0
0x0b03	[15:0]	DATA_0	Compare destination mac[15:0]/IP[15:0] address of uplink port egressing packt which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0	R/W	0x0
0x0b04	[15:0]	DATA_1	Compare destination mac[31:16]/IP[31:16] address of uplink port egressing packt which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0	R/W	0x0
0x0b05~ 0x0b09			SVLAN MC2S configuration entry 1, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b0a~ 0x0b0e			SVLAN MC2S configuration entry 2, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b0f~ 0x0b13			SVLAN MC2S configuration entry 3, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b14~ 0x0b18			SVLAN MC2S configuration entry 4, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b19~ 0x0b1d			SVLAN MC2S configuration entry 5, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b1e~ 0x0b22			SVLAN MC2S configuration entry 6, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b23~ 0x0b27			SVLAN MC2S configuration entry 7, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b28~ 0x0b2c			SVLAN MC2S configuration entry 8, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b2d~ 0x0b31			SVLAN MC2S configuration entry 9, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b32~ 0x0b36			SVLAN MC2S configuration entry 10, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b37~ 0x0b3b			SVLAN MC2S configuration entry 11, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b3c~ 0x0b40			SVLAN MC2S configuration entry 12, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b41~ 0x0b45			SVLAN MC2S configuration entry 13, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b46~ 0x0b4a			SVLAN MC2S configuration entry 14, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b4b~ 0x0b4f			SVLAN MC2S configuration entry 15, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b50~ 0x0b54			SVLAN MC2S configuration entry 16, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0

0x0b55~ 0x0b59			SVLAN MC2S configuration entry 17, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b5a~ 0x0b5e			SVLAN MC2S configuration entry 18, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b5f~ 0x0b63			SVLAN MC2S configuration entry 19, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b64~ 0x0b68			SVLAN MC2S configuration entry 20, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b69~ 0x0b6d			SVLAN MC2S configuration entry 21, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b6e~ 0x0b72			SVLAN MC2S configuration entry 22, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b73~ 0x0b77			SVLAN MC2S configuration entry 23, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b78~ 0x0b7C			SVLAN MC2S configuration entry 24, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b7d~ 0x0b81			SVLAN MC2S configuration entry 25, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b82~ 0x0b86			SVLAN MC2S configuration entry 26, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b87~ 0x0b8b			SVLAN MC2S configuration entry 27, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b8c~ 0x0b90			SVLAN MC2S configuration entry 28, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b91~ 0x0b95			SVLAN MC2S configuration entry 29, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b96~ 0x0b9a			SVLAN MC2S configuration entry 30, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0
0x0b9b~ 0x0b9f			SVLAN MC2S configuration entry 31, the definition of registers is the same as SVLAN MC2S entry 0	R/W	0x0

15.5. SVLAN SP2C Configuration Register

Address	Bit(s)	Name	Description	R/W	Default
0x0f00	[2:0]	DST_PORT	Egressing customer port number of s-tag packet from uplink ports in S2C configuration entry 0	R/W	0x0
	[8:3]	SVIDX	SVID of ingress s-tag packet from uplink ports in S2C configuration entry 0	R/W	0x0
	[15:9]	RESERVED	Reserved		
0x0f01	[11:0]	VID	Egressing CVID of s-tag packet from uplink ports that SVID and egress port number are the same as S2C configuration entry 0	R/W	0x0
	[12]	VALID	vaid bit	R/W	0x0
	[15:13]	RESERVED	Reserved		
0x0f02~ 0x0f03			SVLAN S2C configuration entry 1, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f04~ 0x0f05			SVLAN S2C configuration entry 2, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0

0x0f06~ 0x0f07			SVLAN S2C configuration entry 3, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f08~ 0x0f09			SVLAN S2C configuration entry 4, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f0a~ 0x0f0b			SVLAN S2C configuration entry 5, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f0c~ 0x0f0d			SVLAN S2C configuration entry 6, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f0e~ 0x0f0f			SVLAN S2C configuration entry 7, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f10~ 0x0f11			SVLAN S2C configuration entry 8, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f12~ 0x0f13			SVLAN S2C configuration entry 9, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f14~ 0x0f15			SVLAN S2C configuration entry 10, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f16~ 0x0f17			SVLAN S2C configuration entry 11, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f18~ 0x0f19			SVLAN S2C configuration entry 12, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f1a~ 0x0f1b			SVLAN S2C configuration entry 13, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f1c~ 0x0f1d			SVLAN S2C configuration entry 14, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f1e~ 0x0f1f			SVLAN S2C configuration entry 15, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f20~ 0x0f21			SVLAN S2C configuration entry 16, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f22~ 0x0f23			SVLAN S2C configuration entry 17, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f24~ 0x0f25			SVLAN S2C configuration entry 18, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f26~ 0x0f27			SVLAN S2C configuration entry 19, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f28~ 0x0f29			SVLAN S2C configuration entry 20, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f2a~ 0x0f2b			SVLAN S2C configuration entry 21, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f2c~ 0x0f2d			SVLAN S2C configuration entry 22, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f2e~ 0x0f2f			SVLAN S2C configuration entry 23, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f30~ 0x0f31			SVLAN S2C configuration entry 24, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f32~ 0x0f33			SVLAN S2C configuration entry 25, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f34~ 0x0f35			SVLAN S2C configuration entry 26, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0

0x0f36~ 0x0f37			SVLAN S2C configuration entry 27, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f38~ 0x0f39			SVLAN S2C configuration entry 28, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f3a~ 0x0f3b			SVLAN S2C configuration entry 29, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f3c~ 0x0f3d			SVLAN S2C configuration entry 30, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f3e~ 0x0f3f			SVLAN S2C configuration entry 31, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f40~ 0x0f41			SVLAN S2C configuration entry 32, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f42~ 0x0f43			SVLAN S2C configuration entry 33, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f44~ 0x0f45			SVLAN S2C configuration entry 34, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f46~ 0x0f47			SVLAN S2C configuration entry 35, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f48~ 0x0f49			SVLAN S2C configuration entry 36, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f4a~ 0x0f4b			SVLAN S2C configuration entry 37, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f4c~ 0x0f4d			SVLAN S2C configuration entry 38, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f4e~ 0x0f4f			SVLAN S2C configuration entry 39, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f50~ 0x0f51			SVLAN S2C configuration entry 40, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f52~ 0x0f53			SVLAN S2C configuration entry 41, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f54~ 0x0f55			SVLAN S2C configuration entry 42, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f56~ 0x0f57			SVLAN S2C configuration entry 43, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f58~ 0x0f59			SVLAN S2C configuration entry 44, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f5a~ 0x0f5b			SVLAN S2C configuration entry 45, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f5c~ 0x0f5d			SVLAN S2C configuration entry 46, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f5e~ 0x0f5f			SVLAN S2C configuration entry 47, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f60~ 0x0f61			SVLAN S2C configuration entry 48, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f62~ 0x0f63			SVLAN S2C configuration entry 49, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f64~ 0x0f65			SVLAN S2C configuration entry 50, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0

0x0f66~ 0x0f67			SVLAN S2C configuration entry 51, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f68~ 0x0f69			SVLAN S2C configuration entry 52, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f6a~ 0x0f6b			SVLAN S2C configuration entry 53, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f6c~ 0x0f6d			SVLAN S2C configuration entry 54, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f6e~ 0x0f6f			SVLAN S2C configuration entry 55, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f70~ 0x0f71			SVLAN S2C configuration entry 56, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f72~ 0x0f73			SVLAN S2C configuration entry 57, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f74~ 0x0f75			SVLAN S2C configuration entry 58, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f76~ 0x0f77			SVLAN S2C configuration entry 59, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f78~ 0x0f79			SVLAN S2C configuration entry 60, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f7a~ 0x0f7b			SVLAN S2C configuration entry 61, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f7c~ 0x0f7d			SVLAN S2C configuration entry 62, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f7e~ 0x0f7f			SVLAN S2C configuration entry 63, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f80~ 0x0f81			SVLAN S2C configuration entry 64, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f82~ 0x0f83			SVLAN S2C configuration entry 65, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f84~ 0x0f85			SVLAN S2C configuration entry 66, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f86~ 0x0f87			SVLAN S2C configuration entry 67, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f88~ 0x0f89			SVLAN S2C configuration entry 68, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f8a~ 0x0f8b			SVLAN S2C configuration entry 69, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f8c~ 0x0f8d			SVLAN S2C configuration entry 70, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f8e~ 0x0f8f			SVLAN S2C configuration entry 71, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f90~ 0x0f91			SVLAN S2C configuration entry 72, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f92~ 0x0f93			SVLAN S2C configuration entry 73, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f94~ 0x0f95			SVLAN S2C configuration entry 74, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0

0x0f96~ 0x0f97			SVLAN S2C configuration entry 75, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f98~ 0x0f99			SVLAN S2C configuration entry 76, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f9a~ 0x0f9b			SVLAN S2C configuration entry 77, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f9c~ 0x0f9d			SVLAN S2C configuration entry 78, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0f9e~ 0x0f9f			SVLAN S2C configuration entry 79, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fa0~ 0x0fa1			SVLAN S2C configuration entry 80, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fa2~ 0x0fa3			SVLAN S2C configuration entry 81, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fa4~ 0x0fa5			SVLAN S2C configuration entry 82, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fa6~ 0x0fa7			SVLAN S2C configuration entry 83, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fa8~ 0x0fa9			SVLAN S2C configuration entry 84, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0faa~ 0x0fab			SVLAN S2C configuration entry 85, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fac~ 0x0fad			SVLAN S2C configuration entry 86, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fae~ 0x0faf			SVLAN S2C configuration entry 87, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fb0~ 0x0fb1			SVLAN S2C configuration entry 88, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fb2~ 0x0fb3			SVLAN S2C configuration entry 89, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fb4~ 0x0fb5			SVLAN S2C configuration entry 90, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fb6~ 0x0fb7			SVLAN S2C configuration entry 91, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fb8~ 0x0fb9			SVLAN S2C configuration entry 92, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fba~ 0x0fbb			SVLAN S2C configuration entry 93, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fbc~ 0x0fbd			SVLAN S2C configuration entry 94, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fbe~ 0x0fbf			SVLAN S2C configuration entry 95, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fc0~ 0x0fc1			SVLAN S2C configuration entry 96, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fc2~ 0x0fc3			SVLAN S2C configuration entry 97, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fc4~ 0x0fc5			SVLAN S2C configuration entry 98, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0

0x0fc6~ 0x0fc7			SVLAN S2C configuration entry 99, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fc8~ 0x0fc9			SVLAN S2C configuration entry 100, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fca~ 0x0fcb			SVLAN S2C configuration entry 101, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fcc~ 0x0fcd			SVLAN S2C configuration entry 102, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fce~ 0x0fcf			SVLAN S2C configuration entry 103, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fd0~ 0x0fd1			SVLAN S2C configuration entry 104, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fd2~ 0x0fd3			SVLAN S2C configuration entry 105, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fd4~ 0x0fd5			SVLAN S2C configuration entry 106, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fd6~ 0x0fd7			SVLAN S2C configuration entry 107, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fd8~ 0x0fd9			SVLAN S2C configuration entry 108, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fda~ 0x0fdb			SVLAN S2C configuration entry 109, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fdc~ 0x0fdd			SVLAN S2C configuration entry 110, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fde~ 0x0fdf			SVLAN S2C configuration entry 111, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fe0~ 0x0fe1			SVLAN S2C configuration entry 112, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fe2~ 0x0fe3			SVLAN S2C configuration entry 113, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fe4~ 0x0fe5			SVLAN S2C configuration entry 114, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fe6~ 0x0fe7			SVLAN S2C configuration entry 115, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fe8~ 0x0fe9			SVLAN S2C configuration entry 116, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fea~ 0x0feb			SVLAN S2C configuration entry 117, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fec~ 0x0fed			SVLAN S2C configuration entry 118, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0fee~ 0x0fef			SVLAN S2C configuration entry 119, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0ff0~ 0x0ff1			SVLAN S2C configuration entry 120, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0ff2~ 0x0ff3			SVLAN S2C configuration entry 121, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0ff4~ 0x0ff5			SVLAN S2C configuration entry 122, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0

0x0ff6~ 0x0ff7			SVLAN S2C configuration entry 123, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0ff8~ 0x0ff9			SVLAN S2C configuration entry 124, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0ffa~ 0x0ffb			SVLAN S2C configuration entry 125, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0ffc~ 0x0ffd			SVLAN S2C configuration entry 126, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0
0x0ffe~ 0x0fff			SVLAN S2C configuration entry 127, the definition of registers is the same as SVLAN S2C entry 0	R/W	0x0

16. Port

16.1. Port Ability Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1310	[11:0]	EXT_0_FORCE	ext0 force ability [1:0]:Speed [2]:Duplex [3]:reserved [4]:LINK [5]:RXPAUSE [6]:TXPAUSE [7]:NWAY [8]:MST_MOD [9]:MST_FAULT [10]:100_LPI	R/W	0x0
	[12]	EXT_0_FORCE	force mode for ext0	R/W	0x0
	[15:13]	RESERVED	Reserved	R/W	0x0
0x1311		CFG_EXT1_FORCE	Same as 0x1310	R/W	0x0
0x13c4		CFG_EXT2_FORCE	Same as 0x1310	R/W	0x0
0x1312		CFG_PHY0_FORCE	Same as 0x1310	R/W	0x0
0x1313		CFG_PHY1_FORCE	Same as 0x1310	R/W	0x0
0x1314		CFG_PHY2_FORCE	Same as 0x1310	R/W	0x0
0x1315		CFG_PHY3_FORCE	Same as 0x1310	R/W	0x0
0x1316		CFG_PHY4_FORCE	Same as 0x1310	R/W	0x0

16.2. Port Status Register

Address	Bit(s)	Name	Description	R/W	Default
0x1352	[1:0]	LINK_SPEED	link speed . 00=10M 01=100M 10=1000M 11=Reserved; should never occur	R/O	0
	[2]	FULL_DUPLUX_CAP	full duplex capable 0=half duplex 1=full duplex	R/O	0
	[3]	RESERVED	Reserved	R/O	0
	[4]	LINK_STATE	link status : 0=link status is not okay 1=link status is okay	R/O	0
	[5]	RX_FLOWCTRL_CAP	receive flow control capable 0:not flow control capable 1:flow control capable		0
	[6]	TX_FLOWCTRL_CAP	transmit flow control 0:not flow control capable 1:flow control capable	R/O	0

	[7]	NWAY_CAP	Auto-Negotiation Ability 1=Auto-negotiation capable. 0=Without Auto-negotiation capability.	R/O	0
	[8]	LINK_ON_MASTER	link on in master mode	R/O	0
	[9]	NWAY_FAULT	N-way fault	R/O	0
	[10]	EN_100_LPI	en_100_lpi	R/O	0
	[11]	EN_1000_LPI	en_1000_lpi	R/O	0
	[15:12]	RESERVED	Reserved	R/O	0
0x1353		PORT1_STATUS	Same as 0x1352		
0x1354		PORT2_STATUS	Same as 0x1352		
0x1355		PORT3_STATUS	Same as 0x1352		
0x1356		PORT4_STATUS	Same as 0x1352		
0x1357		PORT5_STATUS	Same as 0x1352		
0x1358		PORT6_STATUS	Same as 0x1352		
0x1359		PORT7_STATUS	Same as 0x1352		

16.3. External Interface Mode Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1305	[3:0]	SELECT_RGMII_0	0000:Disable 0001:port 5 MAC with RGMII 0010:port 5 MAC with MII MAC mode 0011:port 5 MAC with MII PHY mode 0100:port 5 MAC with TMII MAC mode 0101:port 5 MAC with TMII PHY mode 0110:port 5 MAC with GMII 0111:port 5 MAC with RMII MAC mode 1000:port 5 MAC with RMII PHY mode	R/W	0x0
	[7:4]	SELECT_RGMII_1	0000:Disable 0001:port 6 MAC with RGMII 0010:port 6 MAC with MII MAC mode 0011:port 6 MAC with MII PHY mode 0100:port 6 MAC with TMII MAC mode 0101:port 6 MAC with TMII PHY mode 0110:port 6 MAC with GMII 0111:port 6 MAC with RMII MAC mode 1000:port 6 MAC with RMII PHY mode	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x13c3	[3:0]	SELECT_RGMII_2	0000:Disable 0001:port 7 MAC with RGMII 0010:port 7 MAC with MII MAC mode 0011:port 7 MAC with MII PHY mode 0100:port 7 MAC with TMII MAC mode 0101:port 7 MAC with TMII PHY mode 0110:port 7 MAC with GMII 0111:port 7 MAC with RMII MAC mode 1000:port 7 MAC with RMII PHY mode	R/W	0x0

	[15:4	RESERVED	Reserved		
0x1306	[4:0]	EXT0_RGMXF	ext0 RGMXF configuration 4: select RTBI, 3: TXC delay 2ns, 2:0: delay cell used in rgmrxc	R/W	0x0
	[15:5]	RESERVED	Reserved		
0x1307	[4:0]	EXT1_RGMXF	Ext1 RGMXF configuration 4: select RTBI, 3: TXC delay 2ns, 2:0: delay cell used in rgmrxc	R/W	0x0
	[15:5]	RESERVED	Reserved		
0x13c5	[4:0]	EXT2_RGMXF	Ext1 RGMXF configuration 4: select RTBI, 3: TXC delay 2ns, 2:0: delay cell used in rgmrxc	R/W	0x0
	[15:5]	RESERVED	Reserved		

16.4. Port Security Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0890	[7:0]	UNUCAST_FLOADING_PMSK	Egress port mask for unknown unicast flooding packets	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x0891	[7:0]	UNMCAST_FLOADING_PMSK	Egress port mask for unknown multicast flooding packets	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x0892	[7:0]	BCAST_FLOADING_PMSK	Egress port mask for broadcast(ff-ff-ff-ff-ff-ff) flooding packets	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x08c5	[7:0]	SOURCE_PORT_BLOCK	per port block packet forwarding which receiving from the same port 0b0:normal forward 0b1:enable block	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x08c6	[7:0]	IPMCAST_VLAN_LEAKY	VLAN leaky for IPv4/IPv6 multicast packets 0b0:diable 0b1:enable	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x08c7	[7:0]	IPMCAST_PORTISO_LEAKY	Port isolation leaky for for IPv4/IPv6 multicast packets 0b0:diable 0b1:enable	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x08c8	[1:0]	UNKNOW_SA_BEHAVE	Drop/Trap packet if SA is unknown 0b00: normal 0b01: drop packet & disable learning 0b10: trap to CPU 0b11: copy to 8051	R/W	0x0

	[3:2]	UNMATCHED_SA_BEHAVE	Drop/Trap packet if SA is not from the same source port as L2 SPA 0b00: normal 0b01: drop packet & disable learning 0b10: trap to CPU 0b11: copy to 8051	R/W	0x0
	[5:4]	LUT_LEARN_OVER_ACT	Auto leaning number exceed behavior 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: reserved	R/W	0x0
	[7:6]	UNKNOWN_UNICAST_DA_BEHAVE	Drop/Trap packet if unicast DA is unknown 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: reserved	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x08c9	[1:0]	PORT0_UNKNOWN_IP4_MCAST	Port 0 unknow IPv4 multicast frame behavior 0b00: normal flooding 0b01: drop packet, exclude IP 224.0.0.x and IGMP packets 0b10: trap to CPU, exclude IP 224.0.0.x and IGMP packets 0b11: flooding to router port only	R/W	0x0
	[3:2]	PORT1_UNKNOWN_IP4_MCAST	Port 1 unknow IPv4 multicast frame behavior	R/W	0x0
	[5:4]	PORT2_UNKNOWN_IP4_MCAST	Port 2 unknow IPv4 multicast frame behavior	R/W	0x0
	[7:6]	PORT3_UNKNOWN_IP4_MCAST	Port 3 unknow IPv4 multicast frame behavior	R/W	0x0
	[9:8]	PORT4_UNKNOWN_IP4_MCAST	Port 4 unknow IPv4 multicast frame behavior	R/W	0x0
	[11:10]	PORT5_UNKNOWN_IP4_MCAST	Port 5 unknow IPv4 multicast frame behavior	R/W	0x0
	[13:12]	PORT6_UNKNOWN_IP4_MCAST	Port 6 unknow IPv4 multicast frame behavior	R/W	0x0
	[15:14]	PORT7_UNKNOWN_IP4_MCAST	Port 7 unknow IPv4 multicast frame behavior	R/W	0x0
0x08cb	[1:0]	PORT0_UNKNOWN_IP6_MCAST	Port 0 unknow IPv6 multicast frame behavior 0b00: normal flooding 0b01: drop packet, exclude MLD packets 0b10: trap to CPU, exclude MLD packets 0b11: flooding to router port only	R/W	0x0
	[3:2]	PORT1_UNKNOWN_IP6_MCAST	Port 1 unknow IPv6 multicast frame behavior	R/W	0x0
	[5:4]	PORT2_UNKNOWN_IP6_MCAST	Port 2 unknow IPv6 multicast frame behavior	R/W	0x0
	[7:6]	PORT3_UNKNOWN_IP6_MCAST	Port 3 unknow IPv6 multicast frame behavior	R/W	0x0
	[9:8]	PORT4_UNKNOWN_IP6_MCAST	Port 4 unknow IPv6 multicast frame behavior	R/W	0x0
	[11:10]	PORT5_UNKNOWN_IP6_MCAST	Port 5 unknow IPv6 multicast frame behavior	R/W	0x0
	[13:12]	PORT6_UNKNOWN_IP6_MCAST	Port 6 unknow IPv6 multicast frame behavior	R/W	0x0
	[15:14]	PORT7_UNKNOWN_IP6_MCAST	Port 7 unknow IPv6 multicast frame behavior	R/W	0x0
0x08cd	[1:0]	PORT0_UNKNOWN_IP4_MCAST	Port 0 unknow L2 multicast frame behavior 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: drop packet exclude RMA	R/W	0x0
	[3:2]	PORT1_UNKNOWN_IP4_MCAST	Port 1 unknow L2 multicast frame behavior	R/W	0x0
	[5:4]	PORT2_UNKNOWN_IP4_MCAST	Port 2 unknow L2multicast frame behavior	R/W	0x0
	[7:6]	PORT3_UNKNOWN_IP4_MCAST	Port 3 unknow L2multicast frame behavior	R/W	0x0

	[9:8]	PORT4_UNKNOWN_IP4_MCAST	Port 4 unknow L2multicast frame behavior	R/W	0x0
	[11:10]	PORT5_UNKNOWN_IP4_MCAST	Port 5 unknow L2multicast frame behavior	R/W	0x0
	[13:12]	PORT6_UNKNOWN_IP4_MCAST	Port 6 unknow L2multicast frame behavior	R/W	0x0
	[15:14]	PORT7_UNKNOWN_IP4_MCAST	Port 7 unknow L2multicast frame behavior	R/W	0x0

16.5. EEE Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0018	[9:0]	RESERVED	Reserved		
	[10]	EEE_GIGA	mac enable eee in giga	R/W	0x0
	[11]	EEE_100M	mac enable eee in 100M	R/W	0x0
	[15:12]	RESERVED	Reserved		
0x0038		P1EEECFG	Same as 0x0018		
0x0058		P2EEECFG	Same as 0x0018		
0x0078		P3EEECFG	Same as 0x0018		
0x0098		P4EEECFG	Same as 0x0018		
0x00b8		P5EEECFG	Same as 0x0018		
0x00d8		P6EEECFG	Same as 0x0018		
0x00f8		P7EEECFG	Same as 0x0018		

16.6. Misc

Address	Bit(s)	Name	Description	R/W	Default
0x1200	[12:0]	RESERVED	Reserved		
	[14:13]	MAX_LENTH_CTRL	Max. bc ctrl(0:1522, 1:1536, 2:1552, 3:16k)	R/W	0x0
	[15]	RESERVED	Reserved		
0x1207	[3:1]	RESERVED	Reserved		
	[4]	EN_BACLPRESSURE	Enable backpressure 0: disable 1:enable	R/W	0x1
	[15:5]	RESERVED	Reserved		
0x130f	[4:0]	RESERVED	Reserved		
	[5]	PDNPHY	0: Enable all PHY (Default) 1: Power Down All PHY Reverse strapping option pin (EN_PHY)	R/W	0x0
	[6]	GREEN_ON	0: Disable green ethernet 1: Enable green ethernet (default)	R/W	0x1
	[15:7]	RESERVED	Reserved		

17. Spanning Tree

17.1. MSPT Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0a00	[15:14]	MSTI0_CTRL0_PORT7_STATE	Port 07 status of multiple spanning tree 00	R/W	0x3
	[13:12]	MSTI0_CTRL0_PORT6_STATE	Port 06 status of multiple spanning tree 00	R/W	0x3
	[11:10]	MSTI0_CTRL0_PORT5_STATE	Port 05 status of multiple spanning tree 00	R/W	0x3
	[9:8]	MSTI0_CTRL0_PORT4_STATE	Port 04 status of multiple spanning tree 00	R/W	0x3
	[7:6]	MSTI0_CTRL0_PORT3_STATE	Port 03 status of multiple spanning tree 00	R/W	0x3
	[5:4]	MSTI0_CTRL0_PORT2_STATE	Port 02 status of multiple spanning tree 00	R/W	0x3
	[3:2]	MSTI0_CTRL0_PORT1_STATE	Port 01 status of multiple spanning tree 00	R/W	0x3
	[1:0]	MSTI0_CTRL0_PORT0_STATE	Port 00 status of multiple spanning tree 00	R/W	0x3
0x0a02	[15:0]	MSTI1_CTRL0	Port 0~Port 7 status of multiple spanning tree 01	R/W	0xFFFF
0x0a04	[15:0]	MSTI2_CTRL0	Port 0~Port 7 status of multiple spanning tree 02	R/W	0xFFFF
0x0a06	[15:0]	MSTI3_CTRL0	Port 0~Port 7 status of multiple spanning tree 03	R/W	0xFFFF
0x0a08	[15:0]	MSTI4_CTRL0	Port 0~Port 7 status of multiple spanning tree 04	R/W	0xFFFF
0x0a0a	[15:0]	MSTI5_CTRL0	Port 0~Port 7 status of multiple spanning tree 05	R/W	0xFFFF
0x0a0c	[15:0]	MSTI6_CTRL0	Port 0~Port 7 status of multiple spanning tree 06	R/W	0xFFFF
0x0a0e	[15:0]	MSTI7_CTRL0	Port 0~Port 7 status of multiple spanning tree 07	R/W	0xFFFF
0x0a10	[15:0]	MSTI8_CTRL0	Port 0~Port 7 status of multiple spanning tree 08	R/W	0xFFFF
0x0a12	[15:0]	MSTI9_CTRL0	Port 0~Port 7 status of multiple spanning tree 09	R/W	0xFFFF
0x0a14	[15:0]	MSTI10_CTRL0	Port 0~Port 7 status of multiple spanning tree 10	R/W	0xFFFF
0x0a16	[15:0]	MSTI11_CTRL0	Port 0~Port 7 status of multiple spanning tree 11	R/W	0xFFFF
0x0a18	[15:0]	MSTI12_CTRL0	Port 0~Port 7 status of multiple spanning tree 12	R/W	0xFFFF
0x0a1a	[15:0]	MSTI13_CTRL0	Port 0~Port 7 status of multiple spanning tree 13	R/W	0xFFFF
0x0a1c	[15:0]	MSTI14_CTRL0	Port 0~Port 7 status of multiple spanning tree 14	R/W	0xFFFF
0x0a1e	[15:0]	MSTI15_CTRL0	Port 0~Port 7 status of multiple spanning tree 15	R/W	0xFFFF

18. Share Meter

18.1. Share Meter Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x1400	[15:0]	METER0_RATE_0	Rate configuration bits[15:0] of shared meter entry 0, unit btes	R/W	0x0
0x1401	[0]	METER0_RATE_1	Rate configuration bit[16] of shared meter entry 0	R/W	0
	[15:1]	RESERVED	Reserved		
0x1402		METER1_RATE_0	Same as 0x1400		
0x1403		METER1_RATE_1	Same as 0x1401		
0x1404		METER2_RATE_0	Same as 0x1400		
0x1405		METER2_RATE_1	Same as 0x1401		
0x1406		METER3_RATE_0	Same as 0x1400		
0x1407		METER3_RATE_1	Same as 0x1401		
0x1408		METER4_RATE_0	Same as 0x1400		
0x1409		METER4_RATE_1	Same as 0x1401		
0x140a		METER5_RATE_0	Same as 0x1400		
0x140b		METER5_RATE_1	Same as 0x1401		
0x140c		METER6_RATE_0	Same as 0x1400		
0x140d		METER6_RATE_1	Same as 0x1401		
0x140e		METER7_RATE_0	Same as 0x1400		
0x140f		METER7_RATE_1	Same as 0x1401		
0x1410		METER8_RATE_0	Same as 0x1400		
0x1411		METER8_RATE_1	Same as 0x1401		
0x1412		METER9_RATE_0	Same as 0x1400		
0x1413		METER9_RATE_1	Same as 0x1401		
0x1414		METER10_RATE_0	Same as 0x1400		
0x1415		METER10_RATE_1	Same as 0x1401		
0x1416		METER11_RATE_0	Same as 0x1400		
0x1417		METER11_RATE_1	Same as 0x1401		
0x1418		METER12_RATE_0	Same as 0x1400		
0x1419		METER12_RATE_1	Same as 0x1401		
0x141a		METER13_RATE_0	Same as 0x1400		
0x141b		METER13_RATE_1	Same as 0x1401		
0x141c		METER14_RATE_0	Same as 0x1400		
0x141d		METER14_RATE_1	Same as 0x1401		
0x141e		METER15_RATE_0	Same as 0x1400		
0x141f		METER15_RATE_1	Same as 0x1401		
0x1420		METER16_RATE_0	Same as 0x1400		
0x1421		METER16_RATE_1	Same as 0x1401		
0x1422		METER17_RATE_0	Same as 0x1400		
0x1423		METER17_RATE_1	Same as 0x1401		
0x1424		METER18_RATE_0	Same as 0x1400		
0x1425		METER18_RATE_1	Same as 0x1401		

0x1426		METER19_RATE_0	Same as 0x1400		
0x1427		METER19_RATE_1	Same as 0x1401		
0x1428		METER20_RATE_0	Same as 0x1400		
0x1429		METER20_RATE_1	Same as 0x1401		
0x142a		METER21_RATE_0	Same as 0x1400		
0x142b		METER21_RATE_1	Same as 0x1401		
0x142c		METER22_RATE_0	Same as 0x1400		
0x142d		METER22_RATE_1	Same as 0x1401		
0x142e		METER23_RATE_0	Same as 0x1400		
0x142f		METER23_RATE_1	Same as 0x1401		
0x1430		METER24_RATE_0	Same as 0x1400		
0x1431		METER24_RATE_1	Same as 0x1401		
0x1432		METER25_RATE_0	Same as 0x1400		
0x1433		METER25_RATE_1	Same as 0x1401		
0x1434		METER26_RATE_0	Same as 0x1400		
0x1435		METER26_RATE_1	Same as 0x1401		
0x1436		METER27_RATE_0	Same as 0x1400		
0x1437		METER27_RATE_1	Same as 0x1401		
0x1438		METER28_RATE_0	Same as 0x1400		
0x1439		METER28_RATE_1	Same as 0x1401		
0x143a		METER29_RATE_0	Same as 0x1400		
0x143b		METER29_RATE_1	Same as 0x1401		
0x143c		METER30_RATE_0	Same as 0x1400		
0x143d		METER30_RATE_1	Same as 0x1401		
0x143e		METER31_RATE_0	Same as 0x1400		
0x143f		METER31_RATE_1	Same as 0x1401		
0x1430		METER32_RATE_0	Same as 0x1400		
0x1441		METER32_RATE_1	Same as 0x1401		
0x1442		METER33_RATE_0	Same as 0x1400		
0x1443		METER33_RATE_1	Same as 0x1401		
0x1444		METER34_RATE_0	Same as 0x1400		
0x1445		METER34_RATE_1	Same as 0x1401		
0x1446		METER35_RATE_0	Same as 0x1400		
0x1447		METER35_RATE_1	Same as 0x1401		
0x1448		METER36_RATE_0	Same as 0x1400		
0x1449		METER36_RATE_1	Same as 0x1401		
0x144a		METER37_RATE_0	Same as 0x1400		
0x144b		METER37_RATE_1	Same as 0x1401		
0x144c		METER38_RATE_0	Same as 0x1400		
0x144d		METER38_RATE_1	Same as 0x1401		
0x144e		METER39_RATE_0	Same as 0x1400		
0x144f		METER39_RATE_1	Same as 0x1401		
0x1450		METER40_RATE_0	Same as 0x1400		
0x1451		METER40_RATE_1	Same as 0x1401		
0x1452		METER41_RATE_0	Same as 0x1400		

0x1453		METER41_RATE_1	Same as 0x1401		
0x1454		METER42_RATE_0	Same as 0x1400		
0x1455		METER42_RATE_1	Same as 0x1401		
0x1456		METER43_RATE_0	Same as 0x1400		
0x1457		METER43_RATE_1	Same as 0x1401		
0x1458		METER44_RATE_0	Same as 0x1400		
0x1459		METER44_RATE_1	Same as 0x1401		
0x145a		METER45_RATE_0	Same as 0x1400		
0x145b		METER45_RATE_1	Same as 0x1401		
0x145c		METER46_RATE_0	Same as 0x1400		
0x145d		METER46_RATE_1	Same as 0x1401		
0x145e		METER47_RATE_0	Same as 0x1400		
0x145f		METER47_RATE_1	Same as 0x1401		
0x1460		METER48_RATE_0	Same as 0x1400		
0x1461		METER48_RATE_1	Same as 0x1401		
0x1462		METER49_RATE_0	Same as 0x1400		
0x1463		METER49_RATE_1	Same as 0x1401		
0x1464		METER50_RATE_0	Same as 0x1400		
0x1465		METER50_RATE_1	Same as 0x1401		
0x1466		METER51_RATE_0	Same as 0x1400		
0x1467		METER51_RATE_1	Same as 0x1401		
0x1468		METER52_RATE_0	Same as 0x1400		
0x1469		METER52_RATE_1	Same as 0x1401		
0x146a		METER53_RATE_0	Same as 0x1400		
0x146b		METER53_RATE_1	Same as 0x1401		
0x146c		METER54_RATE_0	Same as 0x1400		
0x146d		METER54_RATE_1	Same as 0x1401		
0x146e		METER55_RATE_0	Same as 0x1400		
0x146f		METER55_RATE_1	Same as 0x1401		
0x1470		METER56_RATE_0	Same as 0x1400		
0x1471		METER56_RATE_1	Same as 0x1401		
0x1472		METER57_RATE_0	Same as 0x1400		
0x1473		METER57_RATE_1	Same as 0x1401		
0x1474		METER58_RATE_0	Same as 0x1400		
0x1475		METER58_RATE_1	Same as 0x1401		
0x1476		METER59_RATE_0	Same as 0x1400		
0x1477		METER59_RATE_1	Same as 0x1401		
0x1478		METER60_RATE_0	Same as 0x1400		
0x1479		METER60_RATE_1	Same as 0x1401		
0x147a		METER61_RATE_0	Same as 0x1400		
0x147b		METER61_RATE_1	Same as 0x1401		
0x147c		METER62_RATE_0	Same as 0x1400		
0x147d		METER62_RATE_1	Same as 0x1401		
0x147e		METER63_RATE_0	Same as 0x1400		
0x147f		METER63_RATE_1	Same as 0x1401		

0x1712	[0]	METER0_IFG	Share meter rate calculation with 20 bytes IPG of shared meter entry 0-15 0b0:exclude IPG 0b1:Include IPG each bit as one meter	R/W	0
	[1]	METER1_IFG		R/W	0
	[2]	METER2_IFG		R/W	0
	[3]	METER3_IFG		R/W	0
	[4]	METER4_IFG		R/W	0
	[5]	METER5_IFG		R/W	0
	[6]	METER6_IFG		R/W	0
	[7]	METER7_IFG		R/W	0
	[8]	METER8_IFG		R/W	0
	[9]	METER9_IFG		R/W	0
	[10]	METER10_IFG		R/W	0
	[11]	METER11_IFG		R/W	0
	[12]	METER12_IFG		R/W	0
	[13]	METER13_IFG		R/W	0
	[14]	METER14_IFG		R/W	0
	[15]	METER15_IFG		R/W	0
0x1713	[0]	METER16_IFG	Share meter rate calculation with 20 bytes IPG of shared meter entry 16-31 0b0:exclude IPG 0b1:Include IPG each bit as one meter	R/W	0
	[1]	METER17_IFG		R/W	0
	[2]	METER18_IFG		R/W	0
	[3]	METER19_IFG		R/W	0
	[4]	METER20_IFG		R/W	0
	[5]	METER21_IFG		R/W	0
	[6]	METER22_IFG		R/W	0
	[7]	METER23_IFG		R/W	0
	[8]	METER24_IFG		R/W	0
	[9]	METER25_IFG		R/W	0
	[10]	METER26_IFG		R/W	0
	[11]	METER27_IFG		R/W	0
	[12]	METER28_IFG		R/W	0
	[13]	METER29_IFG		R/W	0
	[14]	METER30_IFG		R/W	0
	[15]	METER31_IFG		R/W	0

19. Trunk

19.1. Trunk Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x08cf	[0]	SPA_HASH	Port trunking hash algorithm selection with SPA (source port)	R/W	0x0
	[1]	SMAC_HASH	Port trunking hash algorithm selection with SMAC	R/W	0x0
	[2]	DMAC_HASH	Port trunking hash algorithm selection with DMAC	R/W	0x0
	[3]	SIP_HASH	Port trunking hash algorithm selection with SIP	R/W	0x0
	[4]	DIP_HASH	Port trunking hash algorithm selection with DIP	R/W	0x0
	[5]	SPORT_HASH	Port trunking hash algorithm selection with SPORT	R/W	0x0
	[6]	DPORT_HASH	Port trunking hash algorithm selection with DPORT	R/W	0x0
	[7]	PORT_TRUNK_FLOOD	Enable directly forwading unknown (L2 lookup miss) packets to aggregation logic 1st port and normal forward other packets to other available trunking ports.	R/W	0x0
	[8]	PORT_TRUNK_DUMB	0: not dumb mode, 1: dumb mode	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x08d0	[3:0]	PORT_TRUNK_GROUP0_MASK	Port trunking aggregation logic port mask for group 0 ports' mask. This trunking group function will be enabled while there are more than 2 trunking ports are aggregated in the mask.	R/W	0x0
	[7:4]	PORT_TRUNK_GROUP1_MASK	Port trunking aggregation logic port mask for group 1 ports' mask	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x022d	[7:0]	PORT_QEMPTY	Egress port mask which output ports' queue FIFO is empty.	R/O	0x0
	[15:8]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
0x08d2	[15:14]	HASH7	Port number mapping to hash value 7	R/W	0x3
	[13:12]	HASH6	Port number mapping to hash value 6	R/W	0x3
	[11:10]	HASH5	Port number mapping to hash value 5	R/W	0x3
	[9:8]	HASH4	Port number mapping to hash value 4	R/W	0x3
	[7:6]	HASH3	Port number mapping to hash value 3	R/W	0x3
	[5:4]	HASH2	Port number mapping to hash value 2	R/W	0x3
	[3:2]	HASH1	Port number mapping to hash value 1	R/W	0x3
	[1:0]	HASH0	Port number mapping to hash value 0	R/W	0x3
0x08d2	[15:14]	HASH15	Port number mapping to hash value 15	R/W	0x3
	[13:12]	HASH14	Port number mapping to hash value 14	R/W	0x3
	[11:10]	HASH13	Port number mapping to hash value 13	R/W	0x3
	[9:8]	HASH12	Port number mapping to hash value 12	R/W	0x3
	[7:6]	HASH11	Port number mapping to hash value 11	R/W	0x3
	[5:4]	HASH10	Port number mapping to hash value 10	R/W	0x3

	[3:2]	HASH9	Port number mapping to hash value 9	R/W	0x3
	[1:0]	HASH8	Port number mapping to hash value 8	R/W	0x3

20. 802.1X

20.1. 802.1X Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0a80	[7:0]	DOT1X_PORT_ENABLE	Per port 802.1X port-based function enable/disable setting. 0b0:disable 0b1:enable	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a81	[7:0]	DOT1X_MAC_ENABLE	Per port 802.1X MAC-based function enable/disable setting. 0b0:disable 0b1:enable	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a82	[7:0]	DOT1X_PORT_AUTH	Per port 802.1X port-based authorication setting. 0b0:unauthorized 0b1:authorized	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a83	[7:0]	DOT1X_PORT_OPDIR	Per port 802.1X port-based operation direction setting while port-based authorication setting is unthorized 0b0:BOTH, unauthorized port can not TX/RX. 0b1:IN , unauthorized port can TX only.	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x0a84	[1:0]	DOT1X_PORT0_UNAUTHBH	Port 0~7 unauthorized behavior for both Port and MAC Access Control 0b00: Drop unauthorized frames 0b01: Trap unauthorized frames to CPU 0b10: Guest VLAN 0b11: Reserved	R/W	0x0
	[3:2]	DOT1X_PORT1_UNAUTHBH		R/W	0x0
	[5:4]	DOT1X_PORT2_UNAUTHBH		R/W	0x0
	[7:6]	DOT1X_PORT3_UNAUTHBH		R/W	0x0
	[9:8]	DOT1X_PORT4_UNAUTHBH		R/W	0x0
	[11:10]	DOT1X_PORT5_UNAUTHBH		R/W	0x0
	[13:12]	DOT1X_PORT6_UNAUTHBH		R/W	0x0
	[15:14]	DOT1X_PORT7_UNAUTHBH		R/W	0x0
0x0a86	[4:0]	DOT1X_GVIDX	Guest VLAN member index for unauthorized packets	R/W	0x0
	[5]	DOT1X_MAC_OPDIR	802.1X Mac-based operation direction setting 0b0:BOTH, don't RX unauthorized SA frame and don't TX unauthorized DA frame 0b1:IN , don't RX unauthorized SA frame only.	R/W	0x0
	[6]	DOT1X_GVOPDIR	Operation direction setting for unauthorized packet belong to guest VLAN 0: SA belongs to Guest VLAN is disallowed to talk to authorized DA 1: SA belongs to Guest VLAN is allowed to talk to authorized DA	R/W	0x0
	[15:7]	RESERVED	Reserved		

21. ACL

21.1. ACL Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x0600	[6:0]	ACL_TEMPLATE0_FIELD0	Type of field 0 in ACL user defined rule template 0	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE0_FIELD1	Type of field 1 in ACL user defined rule template 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x0601	[6:0]	ACL_TEMPLATE0_FIELD2	Type of field 2 in ACL user defined rule template 0	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE0_FIELD3	Type of field 3 in ACL user defined rule template 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x0602	[6:0]	ACL_TEMPLATE0_FIELD4	Type of field 4 in ACL user defined rule template 0	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE0_FIELD5	Type of field 5 in ACL user defined rule template 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x0603	[6:0]	ACL_TEMPLATE0_FIELD6	Type of field 6 in ACL user defined rule template 0	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE0_FIELD7	Type of field 7 in ACL user defined rule template 0	R/W	0x0
	[15]	RESERVED	Reserved		
0x0604	[6:0]	ACL_TEMPLATE1_FIELD0	Type of field 0 in ACL user defined rule template 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE1_FIELD1	Type of field 1 in ACL user defined rule template 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x0605	[6:0]	ACL_TEMPLATE1_FIELD2	Type of field 2 in ACL user defined rule template 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE1_FIELD3	Type of field 3 in ACL user defined rule template 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x0606	[6:0]	ACL_TEMPLATE1_FIELD4	Type of field 4 in ACL user defined rule template 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE1_FIELD5	Type of field 5 in ACL user defined rule template 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x0607	[6:0]	ACL_TEMPLATE1_FIELD6	Type of field 6 in ACL user defined rule template 1	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE1_FIELD7	Type of field 7 in ACL user defined rule template 1	R/W	0x0
	[15]	RESERVED	Reserved		
0x0608	[6:0]	ACL_TEMPLATE2_FIELD0	Type of field 0 in ACL user defined rule template 2	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE2_FIELD1	Type of field 1 in ACL user defined rule template 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x0609	[6:0]	ACL_TEMPLATE2_FIELD2	Type of field 2 in ACL user defined rule template 2	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE2_FIELD3	Type of field 3 in ACL user defined rule template 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x060a	[6:0]	ACL_TEMPLATE2_FIELD4	Type of field 4 in ACL user defined rule template 2	R/W	0x0
	[7]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
	[14:8]	ACL_TEMPLATE2_FIELD5	Type of field 5 in ACL user defined rule template 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x060b	[6:0]	ACL_TEMPLATE2_FIELD6	Type of field 6 in ACL user defined rule template 2	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE2_FIELD7	Type of field 7 in ACL user defined rule template 2	R/W	0x0
	[15]	RESERVED	Reserved		
0x060c	[6:0]	ACL_TEMPLATE3_FIELD0	Type of field 0 in ACL user defined rule template 3	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE3_FIELD1	Type of field 1 in ACL user defined rule template 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x060d	[6:0]	ACL_TEMPLATE3_FIELD2	Type of field 2 in ACL user defined rule template 3	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE3_FIELD3	Type of field 3 in ACL user defined rule template 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x060e	[6:0]	ACL_TEMPLATE3_FIELD4	Type of field 4 in ACL user defined rule template 3	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE3_FIELD5	Type of field 5 in ACL user defined rule template 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x060f	[6:0]	ACL_TEMPLATE3_FIELD6	Type of field 6 in ACL user defined rule template 3	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE3_FIELD7	Type of field 7 in ACL user defined rule template 3	R/W	0x0
	[15]	RESERVED	Reserved		
0x0610	[6:0]	ACL_TEMPLATE4_FIELD0	Type of field 0 in ACL user defined rule template 4	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE4_FIELD1	Type of field 1 in ACL user defined rule template 4	R/W	0x0
	[15]	RESERVED	Reserved		
0x0611	[6:0]	ACL_TEMPLATE4_FIELD2	Type of field 2 in ACL user defined rule template 4	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE4_FIELD3	Type of field 3 in ACL user defined rule template 4	R/W	0x0
	[15]	RESERVED	Reserved		
0x0612	[6:0]	ACL_TEMPLATE4_FIELD4	Type of field 4 in ACL user defined rule template 4	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE4_FIELD5	Type of field 5 in ACL user defined rule template 4	R/W	0x0
	[15]	RESERVED	Reserved		
0x0613	[6:0]	ACL_TEMPLATE4_FIELD6	Type of field 6 in ACL user defined rule template 4	R/W	0x0
	[7]	RESERVED	Reserved		
	[14:8]	ACL_TEMPLATE4_FIELD7	Type of field 7 in ACL user defined rule template 4	R/W	0x0
0x0614	[0]	ACL_ACT0_CVID	CVID action of ACL rule 0 0b0: disable 0b0: enable	R/W	1
	[1]	ACL_ACT0_SVID	SVID action of ACL rule 0 0b0: disable 0b0: enable	R/W	1
	[2]	ACL_ACT0_PRIORITY	Priority action of ACL rule 0 0b0: disable 0b1: enable	R/W	1

Address	Bit(s)	Name	Description	R/W	Default
	[3]	ACL_ACT0_POLICING	Policing action of ACL rule 0 0b0: disable 0b0: enable	R/W	1
	[4]	ACL_ACT0_FORWARD	Forwarding action of ACL rule 0 0b0: disable 0b1: enable	R/W	1
	[5]	ACL_OP0_NOT	NOT operation of ACL rule 0 0b0: disable 0b1: enable, ACL will do action to rule unmatchd packets	R/W	0
	[7:6]	RESERVED	Reserved		
	[8]	ACL_ACT1_CVID	Action of ACL rule 1	R/W	1
	[9]	ACL_ACT1_SVID		R/W	1
	[10]	ACL_ACT1_PRIORITY		R/W	1
	[11]	ACL_ACT1_POLICING		R/W	1
	[12]	ACL_ACT1_FORWARD		R/W	1
	[13]	ACL_OP1_NOT		R/W	0
	[15:14]	RESERVED	Reserved		
0x0615		ACT_RULE_3_2	Action of ACL Rule 2&3, same as 0x0614		
0x0616		ACT_RULE_5_4	Action of ACL Rule 4&5, same as 0x0614		
0x0617		ACT_RULE_7_6	Action of ACL Rule 6&7, same as 0x0614		
0x0618		ACT_RULE_9_8	Action of ACL Rule 8&9, same as 0x0614		
0x0619		ACT_RULE_11_10	Action of ACL Rule 10&11, same as 0x0614		
0x061a		ACT_RULE_13_12	Action of ACL Rule 12&13, same as 0x0614		
0x061b		ACT_RULE_15_14	Action of ACL Rule 15&14, same as 0x0614		
0x061c		ACT_RULE_17_16	Action of ACL Rule 17&16, same as 0x0614		
0x061d		ACT_RULE_19_18	Action of ACL Rule 19&18, same as 0x0614		
0x061e		ACT_RULE_21_20	Action of ACL Rule 21&20, same as 0x0614		
0x061f		ACT_RULE_23_22	Action of ACL Rule 23&22, same as 0x0614		
0x0620		ACT_RULE_25_24	Action of ACL Rule 25&24, same as 0x0614		
0x0621		ACT_RULE_27_26	Action of ACL Rule 27&26, same as 0x0614		
0x0622		ACT_RULE_29_28	Action of ACL Rule 29&28, same as 0x0614		
0x0623		ACT_RULE_31_30	Action of ACL Rule 31&30, same as 0x0614		
0x0624		ACT_RULE_33_32	Action of ACL Rule 33&32, same as 0x0614		
0x0625		ACT_RULE_35_34	Action of ACL Rule 35&34, same as 0x0614		
0x0626		ACT_RULE_37_36	Action of ACL Rule 37&36, same as 0x0614		
0x0627		ACT_RULE_39_38	Action of ACL Rule 39&38, same as 0x0614		
0x0628		ACT_RULE_41_40	Action of ACL Rule 41&40, same as 0x0614		
0x0629		ACT_RULE_43_42	Action of ACL Rule 43&42, same as 0x0614		
0x062a		ACT_RULE_45_44	Action of ACL Rule 45&44, same as 0x0614		
0x062b		ACT_RULE_47_46	Action of ACL Rule 47&46, same as 0x0614		
0x062c		ACT_RULE_49_48	Action of ACL Rule 49&48, same as 0x0614		
0x062d		ACT_RULE_51_50	Action of ACL Rule 51&50, same as 0x0614		
0x062e		ACT_RULE_53_52	Action of ACL Rule 53&52, same as 0x0614		
0x062f		ACT_RULE_55_54	Action of ACL Rule 55&54, same as 0x0614		
0x0630		ACT_RULE_57_56	Action of ACL Rule 57&56, same as 0x0614		

Address	Bit(s)	Name	Description	R/W	Default
0x0631		ACT_RULE_59_58	Action of ACL Rule 59&58, same as 0x0614		
0x0632		ACT_RULE_61_60	Action of ACL Rule 61&60, same as 0x0614		
0x0633		ACT_RULE_63_62	Action of ACL Rule 63&62, same as 0x0614		
0x0668	[0]	ACL_PORT0_ENABLE	Per port ACL function enable setting	R/W	0
	[1]	ACL_PORT1_ENABLE	0b0:disable	R/W	0
	[2]	ACL_PORT2_ENABLE	0b1:enable	R/W	0
	[3]	ACL_PORT3_ENABLE		R/W	0
	[4]	ACL_PORT4_ENABLE		R/W	0
	[5]	ACL_PORT5_ENABLE		R/W	0
	[6]	ACL_PORT6_ENABLE		R/W	0
	[7]	ACL_PORT7_ENABLE		R/W	0
	[8]	ACL_PORT8_ENABLE		R/W	0
	[9]	ACL_PORT9_ENABLE		R/W	0
	[15:10]	RESERVED	Reserved		
0x06d5	[0]	ACL_PORT0_ENABLE	Per port ACL function enable setting	R/W	0
	[1]	ACL_PORT1_ENABLE	0b0:disable	R/W	0
	[2]	ACL_PORT2_ENABLE	0b1:enable	R/W	0
	[3]	ACL_PORT3_ENABLE		R/W	0
	[4]	ACL_PORT4_ENABLE		R/W	0
	[5]	ACL_PORT5_ENABLE		R/W	0
	[6]	ACL_PORT6_ENABLE		R/W	0
	[7]	ACL_PORT7_ENABLE		R/W	0
	[15:8]	RESERVED	Reserved		
0x06d6	[0]	ACL_PORT0_PERMIT	Per port ACL function permit setting	R/W	0
	[1]	ACL_PORT1_PERMIT	0b0:disable	R/W	0
	[2]	ACL_PORT2_PERMIT	0b1:enable	R/W	0
	[3]	ACL_PORT3_PERMIT		R/W	0
	[4]	ACL_PORT4_PERMIT		R/W	0
	[5]	ACL_PORT5_PERMIT		R/W	0
	[6]	ACL_PORT6_PERMIT		R/W	0
	[7]	ACL_PORT7_PERMIT		R/W	0
	[15:8]	RESERVED	Reserved		

22. 8051 and NIC Control

22.1. 8051 and NIC function Control Register

Address	Bit(s)	Name	Description	R/W	Default
0x130c	[3:0]	RESERVED	Reserved		
	[4]	AUTOLOAD_EN	Autoload function 0: Disable autoload 1: Enable autoload (Bonding Option)	R/W	0x0
	[5]	DW8051_EN	Enable 8051 0: Disable 8051 1: Enable 8051 (Bonding Option)	R/W	0x0
	[9:6]	RESERVED	Reserved		
	[10]	NIC_ENABLE	Enable NIC 0: Disable NIC 1: Enable NIC	R/W	0x0
	[15:11]	RESERVED	Reserved		
0x1322	[3:0]	RESERVED	Reserved		
	[4]	DW8051_RST	8051 Reset 0: Disable 1: Enable	R/W	0x0
	[5]	NIC_RST	NIC Reset 0b1: reset	WO	0x0
	[15:6]	RESERVED	Reserved		
0x1336	[0]	DW8051_READY	8051 is ready. This bit should be written in boot sequence when DW8051_EN is enabled. 0: 8051 is not ready. 1: 8051 is ready.	R/W	0
	[1]	ACS_IROM_ENABLE	IROM access enable 0: Disable access IROM 1: Enable access IROM	R/W	0x0
	[3:2]	IROM_MSB	MSB of IROM address	R/W	0x0
	[6:4]	DW_8051RATE	000: 200M 001: 125M 010: 100M 100: 62.5M 101: 20.8M	R/W	0x0
	[7]	RRCP_MODE	IP^{2P}C Access Mode 0: IP^{2P}C Slave 1: IP^{2P}C Master	R/W	0
	[15:8]	RESERVED	Reserved		

22.2. NIC Pointer and Status Register

Address	Bit(s)	Name	Description	R/W	Default
0x1a04	[7:0]	NIC_RXRDL	Used space of RX buffer (unit: 8 bytes)	R/O	0
	[15:8]	RESERVED	Reserved		
0x1a05	[7:0]	NIC_RXRDH	Used space of RX buffer (unit: 8 bytes)	R/O	0
	[15:8]	RESERVED	Reserved		
0x1a08	[7:0]	NIC_TXASRL	Available space of TX buffer (unit: 8 bytes)	R/O	0
	[15:8]	RESERVED	Reserved		
0x1a09	[7:0]	NIC_TXASRH	Available space of TX buffer (unit: 8 bytes)	R/O	0x3
	[15:8]	RESERVED	Reserved		
0x1a50	[7:0]	NIC_CRXCPRL	Address of CPU pointer of RX buffer (unit: 8bytes)	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1a51	[7:0]	NIC_CRXCPRH	Address of CPU pointer of RX buffer (unit: 8bytes)	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1a52	[7:0]	NIC_CTXCPRL	Address of CPU pointer of TX buffer (unit: 8bytes)	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1a53	[7:0]	NIC_CTXCPRH	Address of CPU pointer of TX buffer (unit: 8bytes)	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1a54	[7:0]	NIC_SRXCURPKTL	Address of NIC pointer of RX buffer (unit: 8bytes)	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1a55	[7:0]	NIC_SRXCURPKTH	Address of NIC pointer of RX buffer (unit: 8bytes)	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1a56	[7:0]	NIC_STXCURPKTL	Address of NIC pointer of TX buffer (unit: 8bytes)	R/O	0x0
	[15:8]	RESERVED	Reserved		
0x1a57	[7:0]	NIC_STXCURPKTH	Address of NIC pointer of TX buffer (unit: 8bytes)	R/O	0x3
	[15:8]	RESERVED	Reserved		

22.3. NIC Configuration Register

Address	Bit(s)	Name	Description	R/W	Default
0x1a0c	[0]	NIC_RXCMD	RX Command. When this bit is set to 1, the current Rx frame buffer is released. This bit is self cleared after the buffer is released	W1C	0x0
	[15:1]	RESERVED	Reserved		
0x1a0d	[0]	NIC_TXCMD	TX Command. When this bit is set to 1, the current frame pointed by NIC_CTXPR in TX buffer is ready to transmit This bit is self cleared.	W1C	0x0
	[15:1]	RESERVED	Reserved		
0x1a0e	[0]	RESERVED	Reserved		
	[7]	NIC_RXIS	Rx interrupt Status When this bit is set, it indicates that the MAC has received a packet from switch core. The bit is cleared by writing 1	R/W	0x0
	[15:8]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
0x1a0f	[0]	RESERVED	Reserved		
	[7]	NIC_RXIE	Rx interrupt enable 0: disable interrupt when packet has been received 1: enable interrupt when packet has been received	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a14	[0]	NIC_ARPPE	ARP pass enable 0: ARP pass is disabled 1: Allow to receive ARP packet when RXBPE is disabled and broadcast packets are discarded	R/W	0x0
	[1]	NIC_RXAPE	Receive all packet enable 0: according to other rules (RXPPS, RXMPE, RXBPE) 1: when HFPPE and HFMPE set to 0, receive all pkts. Otherwise, receive broadcast packets, phiscal address matched packets, receive multicast packet and physical address unmatched	R/W	1
	[3:2]	NIC_RXPPS	Receive Physical Address Packet Select 00: drop all physical address packets 01: receive physical address matched packets 10: when HFPPE set to 0, receive all physical address unmatched packets. Otherwise receive physical address unmatched packets according to HFPPE. 11: when HFPPE set to 0, receive all physical address packets. Otherwise receive physical address matched packets, receive physical address unmatched packets according to HFPPE.	R/W	0
	[4]	NIC_RXMPE	Receive multicast packet enable 0: all multicast packets are discarded 1: when HFMPE is set to 0, receive all multicast packets. Otherwise, receive multicast packets according to HFMPE	R/W	0
	[5]	NIC_RXBPE	Receive broadcast packet enable 0: broadcast packets are discarded 1: allow to receive broadcast packet	R/W	0
	[6]	NIC_HFMPE	Hash filtering multicast address packets enable When this bit set to 1, hash filtering for all multicast address unmatch packets	R/W	0
	[7]	NIC_HFPPE	Hash filtering physical address packets enable When this bit set to 1, hash filtering for all physical address unmatch packets	R/W	0
	[15:8]	RESERVED	Reserved		
0x1a15	[0]	NIC_RXENABLE	Rx Enable 0: disable Rx 1: enable Rx	R/W	0
	[1]	NIC_RMCRC	Remove packet CRC enable 0: don't remove received packet 4 bytes CRC field 1: remove received packet 4 bytes CRC field	R/W	1

Address	Bit(s)	Name	Description	R/W	Default
	[2]	NIC_RCRCEPE	Receive CRC Error Packet Enable 0: error packets are discarded 1: error packets are allowed to be received	R/W	1
	[3]	NIC_RL3CEPE	Receive layer3 checksum error packet enable 0: error packets are discarded 1: error apckets are allowed to be received	R/W	1
	[4]	NIC_RL4CEPE	Receive layer 4 checksum error packet enable 0: error packets are discarded 1: error packets are allowed to be received	R/W	1
	[15:5]	RESERVED	Reserved		
0x1a16	[0]	NIC_TXENABLE	Tx enable 0: disable Tx function 1: enable Tx function	R/W	0x0
	[1]	NIC_TXMFM	Tx buffer memory fre mode select 0: packet-based memory free 1: byte-based memory free	R/W	0x0
	[2]	NIC_LBE	Loopback Enable. When this bit is set to 1, NIC Tx loopback to NIC Rx, not to switch core 0: disable loopback 1: enable loopback	R/W	0x0
	[15:3]	RESERVED	Reserved		
0x1a17	[3:0]	RESERVED	Reserved		
	[5:4]	NIC_RXMTU	The maximum transmission unit of Rx packet 00: 1522 bytes 01: 2k bytes 10: 4kbytes 11: reserved	R/W	0x1
	[15:6]	RESERVED	Reserved		
0x1a24	[7:0]	NIC_MHR0	Multicast hash register 0	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a25	[7:0]	NIC_MHR1	Multicast hash register 1	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a26	[7:0]	NIC_MHR2	Multicast hash register 2	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a27	[7:0]	NIC_MHR3	Multicast hash register 3	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a28	[7:0]	NIC_MHR4	Multicast hash register 4	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a29	[7:0]	NIC_MHR5	Multicast hash register 5	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a2a	[7:0]	NIC_MHR6	Multicast hash register 6	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a2b	[7:0]	NIC_MHR7	Multicast hash register 7	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a2c	[7:0]	NIC_PAHR0	Physical address hash register 0	R/W	0x0
	[15:8]	RESERVED	Reserved		

Address	Bit(s)	Name	Description	R/W	Default
0x1a2d	[7:0]	NIC_PAHR1	Physical address hash register 1	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a2e	[7:0]	NIC_PAHR2	Physical address hash register 2	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a2f	[7:0]	NIC_PAHR3	Physical address hash register 3	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a30	[7:0]	NIC_PAHR4	Physical address hash register 4	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a31	[7:0]	NIC_PAHR5	Physical address hash register 5	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a32	[7:0]	NIC_PAHR6	Physical address hash register 6	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a33	[7:0]	NIC_PAHR7	Physical address hash register 7	R/W	0x0
	[15:8]	RESERVED	Reserved		
0x1a44	[7:0]	NIC_TXSTOPL	NIC TX buffer end addres, unit: 8 octets	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x1a45	[7:0]	NIC_TXSTOPH	NIC TX buffer end address, unit: 8 octets	R/W	0x3
	[15:8]	RESERVED	Reserved		
0x1a46	[7:0]	NIC_RXSTOPL	NIC RX buffer end address, unit: 8 octets	R/W	0xFF
	[15:8]	RESERVED	Reserved		
0x1a47	[7:0]	NIC_RXSTOPH	NIC RX buffer end address, unit: 8 octets	R/W	0x5
	[15:8]	RESERVED	Reserved		
0x1a48	[7:0]	NIC_RXFST	Rx buffer free space threshold When free space of Rx buffer is less than RXFST, NIC will flow control switch core, and stop writing packets to Rx buffer. NIC will continue to write packets to Rx buffer when the free space of Rx buffer is more than RXFST.	R/W	1
	[15:8]	RESERVED	Reserved		