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RTL8382L-VB-CG

UN-MANAGED 26*10/100/1000M-PORT SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing the Realtek Ethernet Switch Controllers.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2014/01/20	First release.
1.1	2016/1/8	Remove the support for 10M-EEE and I2C master for EEPROM.
1.2	2016/6/30	Separate managed & unmanaged series.

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1. General Description

The RTL8382L-VB-CG is a new generation Gigabit switches supporting Energy Efficient Ethernet (EEE).It is a 26-port 10/100/1000M switch controller which has an 8-port 10/100/1000M Ethernet PHY embedded.

The RTL8382L-VB-CG is provided via a 55nm CMOS process in an LQFP-216 E-PAD package. It supports SPI Flash.

Features	RTL8382L-VB
Port Capacity	24G*UTP + 2*1000Base-X
Management Mode	Unmanaged Mode Only
SPI Flash	Yes
EEPROM Config.	Yes
Internal CPU	Yes

The RTL8382L-VB supports four pairs of serially connected QSGMII interface ports to connect to two Octal Gigabit PHYs (RTL8218B).

The RTL8382L-VB has an embedded CPU that supports a 32MByte (max.) SPI flash.

There are 8K entries in the 4-way hash L2 table for MAC address learning and searching. The RTL8382L-VB has a 4K-entry VLAN table for 802.1Q port-based to separate logical connectivity from physical connectivity.

The RTL8382L-VB has 4 user queues in each port.

Support is provided for link aggregation to increase link redundancy, and increase linear bandwidth.

2. Features

- Hardware Interface
  - RTL8382L-VB
    - Provides 26-port Gigabit wire speed forwarding capability
    - Supports 8-port 10/100/1000M Ethernet PHY
    - Supports 4-pairs of QSGMII to connect to external 8-port 10/100/1000M Ethernet PHYs
    - Supports 2 pairs of SGMII/1000Base-X
  - Flash Interface
    - Supports one 32MByte SPI flash interface
  - Embedded CPU
    - Built-in 128KByte SRAM
    - UART interfaces to control the internal CPU
- L2 VLAN Function
  - Supports IEEE 802.1Q VLAN
    - 4K-entry VLAN Table
- L2 MAC Function
  - 4.1 Mbit SRAM Packet Buffer
  - 8K-entry L2 MAC table with 4-way hashing algorithm
  - Supports Reserved Multicast Addresses processing
- L2 Miscellaneous Functions
  - Supports broadcast, multicast, unknown-multicast, and unknown-unicast packet suppression control
  - Supports Link Aggregation (IEEE 802.3ad) for 8 groups of link aggregators with up to 8 ports per-group
  - Port isolation function to enhance port security
- QoS Functions
  - 4 user queues per port
- IEEE 802.3az Energy Efficient Ethernet (EEE)
- Others
  - 55nm CMOS process
  - 3.3V/1.1V dual power input
  - LQFP216 E-PAD package

3. System Applications

*3.1. RTL8382L-VB: Unmanaged 24*1000M UTP+2*1000Base-X Switch*

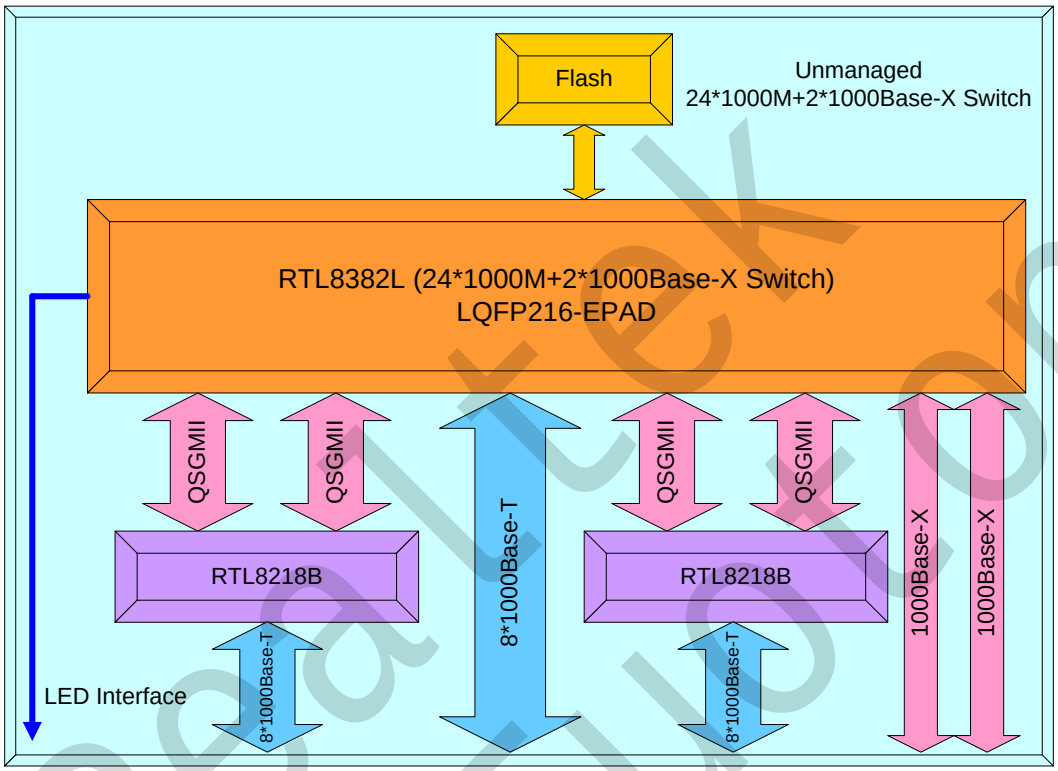


Figure 1. Unmanaged 24*1000M UTP+2*1000Base-X Switch

4. Block Diagrams

4.1. RTL8382L-VB Block Diagram

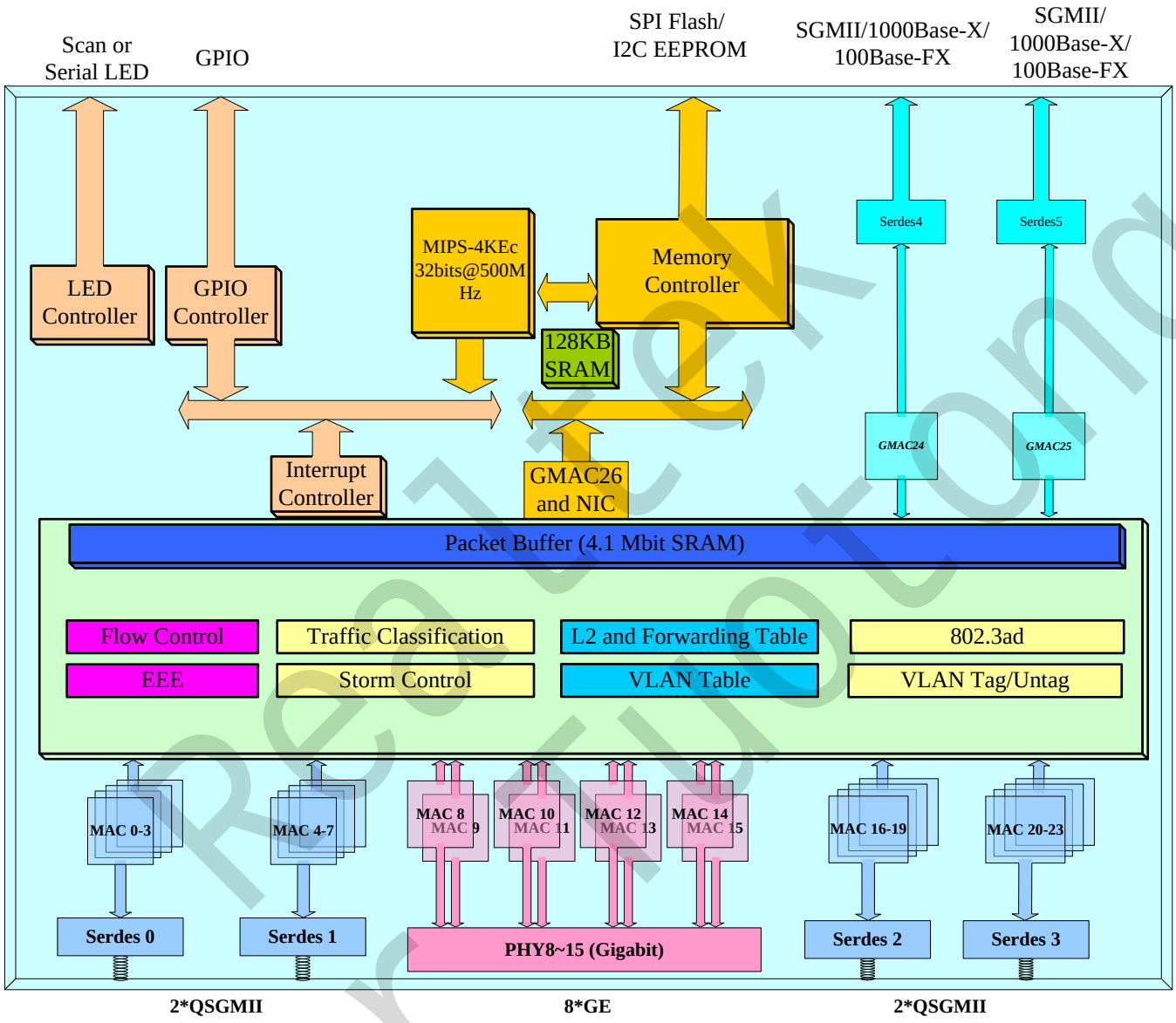


Figure 2. RTL8382L-VB Block Diagram

5. Pin Assignments and Descriptions

5.1. Pin Assignments Figure

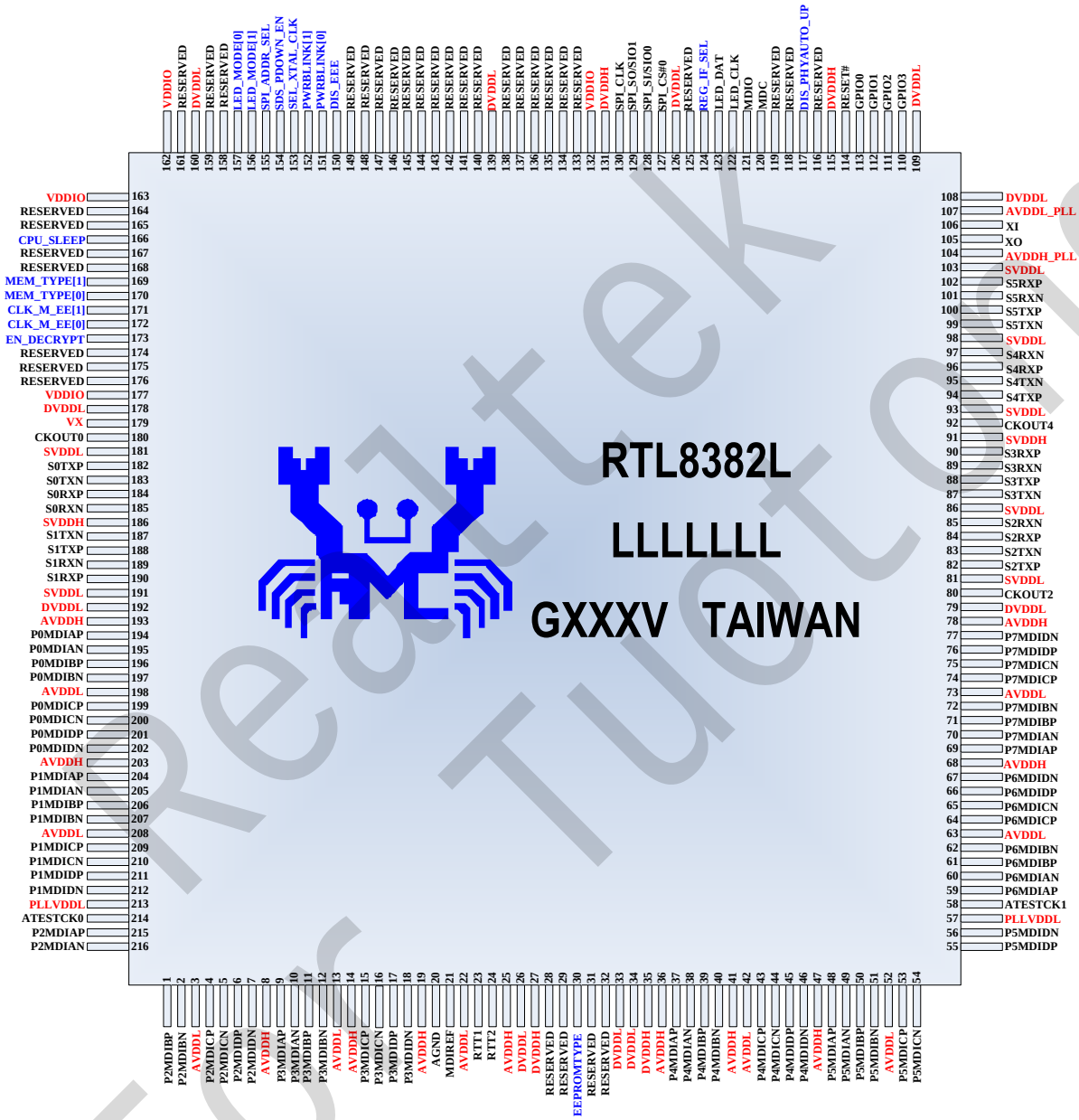


Figure 3. Pin Assignments

5.2. Package Identification

Green package is indicated by a 'G' in 'GXXXX' (Figure 3). The version number is shown in the location marked 'v'.

5.3. Pin Assignments Table Codes

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

$I_{PU:}$ Input Pin With Pull-Up Resistor; (Typical Value = 75KΩ)

$I_{PD:}$ Input Pin With Pull-Down Resistor; (Typical Value = 75KΩ)

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

$O_{PU:}$ Output Pin With Pull-Up Resistor; (Typical Value = 75KΩ)

$O_{PD:}$ Output Pin With Pull-Down Resistor; (Typical Value = 75KΩ)

5.4. Pin Assignments Table

Table 1. Pin Assignments Table

Name	Pin No.	Type
P2MDIBP	1	AI/O
P2MDIBN	2	AI/O
AVDDL	3	AP
P2MDICP	4	AI/O
P2MDICN	5	AI/O
P2MDIDP	6	AI/O
P2MDIDN	7	AI/O
AVDDH	8	AP
P3MDIAP	9	AI/O
P3MDIAN	10	AI/O
P3MDIBP	11	AI/O
P3MDIBN	12	AI/O
AVDDL	13	AP
AVDDH	14	AP
P3MDICP	15	AI/O
P3MDICN	16	AI/O
P3MDIDP	17	AI/O
P3MDIDN	18	AI/O

Name	Pin No.	Type
AVDDH	19	AP
AGND	20	AG
MDIREF	21	A
AVDDL	22	AP
RTT1	23	AI/O
RTT2	24	AI/O
AVDDH	25	AP
DVDDL	26	DP
DVDDH	27	DP
RESERVED	28	-
RESERVED	29	-
EEPROMTYPE	30	I/O_{PD}
RESERVED	31	-
RESERVED	32	-
DVDDL	33	DP
DVDDL	34	DP
DVDDH	35	DP
AVDDH	36	AP

Name	Pin No.	Type
P4MDIAP	37	AI/O
P4MDIAN	38	AI/O
P4MDIBP	39	AI/O
P4MDIBN	40	AI/O
AVDDH	41	AP
AVDDL	42	AP
P4MDICP	43	AI/O
P4MDICN	44	AI/O
P4MDIDP	45	AI/O
P4MDIDN	46	AI/O
AVDDH	47	AP
P5MDIAP	48	AI/O
P5MDIAN	49	AI/O
P5MDIBP	50	AI/O
P5MDIBN	51	AI/O
AVDDL	52	AP
P5MDICP	53	AI/O
P5MDICN	54	AI/O
P5MDIDP	55	AI/O
P5MDIDN	56	AI/O
PLLVDDL	57	AP
ATESTCK1	58	AO
P6MDIAP	59	AI/O
P6MDIAN	60	AI/O
P6MDIBP	61	AI/O
P6MDIBN	62	AI/O
AVDDL	63	AP
P6MDICP	64	AI/O
P6MDICN	65	AI/O
P6MDIDP	66	AI/O
P6MDIDN	67	AI/O
AVDDH	68	AP
P7MDIAP	69	AI/O
P7MDIAN	70	AI/O
P7MDIBP	71	AI/O
P7MDIBN	72	AI/O
AVDDL	73	AP
P7MDICP	74	AI/O
P7MDICN	75	AI/O
P7MDIDP	76	AI/O
P7MDIDN	77	AI/O
AVDDH	78	AP

Name	Pin No.	Type
DVDDL	79	DP
CKOUT2	80	AO
SVDDL	81	AP
S2TXP	82	AO
S2TXN	83	AO
S2RXP	84	AI
S2RXN	85	AI
SVDDL	86	AP
S3TXN	87	AO
S3TXP	88	AO
S3RXN	89	AI
S3RXP	90	AI
SVDDH	91	AP
CKOUT4	92	AO
SVDDL	93	AP
S4TXP	94	AO
S4TXN	95	AO
S4RXP	96	AI
S4RXN	97	AI
SVDDL	98	AP
S5TXN	99	AO
S5TXP	100	AO
S5RXN	101	AI
S5RXP	102	AI
SVDDL	103	AP
AVDDH_PLL	104	AP
XO	105	AO
XI	106	AI
AVDDL_PLL	107	AP
DVDDL	108	P
DVDDL	109	P
GPIO3	110	I/O_{PD}
GPIO2	111	I/O_{PD}
GPIO1	112	I/O_{PD}
GPIO0	113	I/O_{PD}
RESET#	114	AI
DVDDH	115	P
RESERVED	116	-
DIS_PHYAUTO_UP	117	I_{PD}
RESERVED	118	-
RESERVED	119	-

Name	Pin No.	Type
MDC	120	O_{PU}
MDIO	121	I/O_{PU}
LED_CLK	122	O_{PU}
LED_DAT	123	I/O_{PU}
REG_IF_SEL	124	I_{PD}
RESERVED	125	-
DVDDL	126	P
SPI_CS#0	127	O
SPI_SI/SIO0	128	I/O_{PD}
SPI_SO/SIO1	129	I/O_{PD}
SPI_CLK	130	O_{PD}
DVDDH	131	P
VDDIO	132	P
RESERVED	133	I/O
RESERVED	134	I/O
RESERVED	135	I/O
RESERVED	136	I/O
RESERVED	137	I/O
RESERVED	138	I/O
DVDDL	139	P
RESERVED	140	O
RESERVED	141	O
RESERVED	142	I/O
RESERVED	143	P
RESERVED	144	I/O
RESERVED	145	I/O
RESERVED	146	I/O
RESERVED	147	I/O
RESERVED	148	O
RESERVED	149	O
DIS_EEE	150	I
PWRBLINK[0]	151	I
PWRBLINK[1]	152	I
SEL_XTAL_CLK	153	I
SDS_PDOWN_EN	154	I
SPI_ADDR_SEL	155	I
LED/MODE[1]	156	I
LED/MODE[0]	157	I
RESERVED	158	-
RESERVED	159	-
DVDDL	160	P

Name	Pin No.	Type
RESERVED	161	-
VDDIO	162	P
VDDIO	163	P
RESERVED	164	-
RESERVED	165	-
CPU_SLEEP	166	I/O_{PD}
RESERVED	167	-
RESERVED	168	-
MEM_TYPE[1]	169	I/O_{PD}
MEM_TYPE[0]	170	I/O_{PD}
CLK_M_EE[1]	171	I/O_{PD}
CLK_M_EE[0]	172	I/O_{PD}
EN_DECRYPT	173	I/O_{PD}
RESERVED	174	-
RESERVED	175	-
RESERVED	176	-
VDDIO	177	P
DVDDL	178	P
VX	179	A
CKOUT0	180	AO
SVDDL	181	AP
S0TXP	182	AO
S0TXN	183	AO
S0RXP	184	AI
S0RXN	185	AI
SVDDH	186	AP
S1TXN	187	AO
S1TXP	188	AO
S1RXN	189	AI
S1RXP	190	AI
SVDDL	191	AP
DVDDL	192	P
AVDDH	193	AP
P0MDIAP	194	AI/O
P0MDIAN	195	AI/O
P0MDIBP	196	AI/O
P0MDIBN	197	AI/O
AVDDL	198	AP
P0MDICP	199	AI/O
P0MDICN	200	AI/O
P0MDIDP	201	AI/O
P0MDIDN	202	AI/O

Name	Pin No.	Type
AVDDH	203	AP
P1MDIAP	204	AI/O
P1MDIAN	205	AI/O
P1MDIBP	206	AI/O
P1MDIBN	207	AI/O
AVDDL	208	AP
P1MDICP	209	AI/O
P1MDICN	210	AI/O

Name	Pin No.	Type
P1MDIDP	211	AI/O
P1MDIDN	212	AI/O
PLLVDDL	213	AP
ATESTCK0	214	AO
P2MDIAP	215	AI/O
P2MDIAN	216	AI/O
DGND	EPAD	G

5.5. Pin Descriptions

5.5.1. 1000M Ethernet PHY MDI Interface Pins

Table 2. 1000M Ethernet PHY MDI Interface Pins

Pin Name	Pin No.	Type	Description
P0MDIAP	194	AI/O	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P0MDIAN	195	AI/O	
P0MDIBP	196	AI/O	
P0MDIBN	197	AI/O	
P0MDICP	199	AI/O	
P0MDICN	200	AI/O	
P0MDIDP	201	AI/O	
P0MDIDN	202	AI/O	
P1MDIAP	204	AI/O	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P1MDIAN	205	AI/O	
P1MDIBP	206	AI/O	
P1MDIBN	207	AI/O	
P1MDICP	209	AI/O	
P1MDICN	210	AI/O	
P1MDIDP	211	AI/O	
P1MDIDN	212	AI/O	
P2MDIAP	215	AI/O	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P2MDIAN	216	AI/O	
P2MDIBP	1	AI/O	
P2MDIBN	2	AI/O	
P2MDICP	4	AI/O	
P2MDICN	5	AI/O	
P2MDIDP	6	AI/O	
P2MDIDN	7	AI/O	
P3MDIAP	9	AI/O	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P3MDIAN	10	AI/O	
P3MDIBP	11	AI/O	
P3MDIBN	12	AI/O	
P3MDICP	15	AI/O	
P3MDICN	16	AI/O	
P3MDIDP	17	AI/O	
P3MDIDN	18	AI/O	

Pin Name	Pin No.	Type	Description
P4MDIAP	37	AI/O	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P4MDIAN	38	AI/O	
P4MDIBP	39	AI/O	
P4MDIBN	40	AI/O	
P4MDICP	43	AI/O	
P4MDICN	44	AI/O	
P4MDIDP	45	AI/O	
P4MDIDN	46	AI/O	
P5MDIAP	48	AI/O	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P5MDIAN	49	AI/O	
P5MDIBP	50	AI/O	
P5MDIBN	51	AI/O	
P5MDICP	53	AI/O	
P5MDICN	54	AI/O	
P5MDIDP	55	AI/O	
P5MDIDN	56	AI/O	
P6MDIAP	59	AI/O	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P6MDIAN	60	AI/O	
P6MDIBP	61	AI/O	
P6MDIBN	62	AI/O	
P6MDICP	64	AI/O	
P6MDICN	65	AI/O	
P6MDIDP	66	AI/O	
P6MDIDN	67	AI/O	
P7MDIAP	69	AI/O	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100 ohm termination resistor.
P7MDIAN	70	AI/O	
P7MDIBP	71	AI/O	
P7MDIBN	72	AI/O	
P7MDICP	74	AI/O	
P7MDICN	75	AI/O	
P7MDIDP	76	AI/O	
P7MDIDN	77	AI/O	

5.5.2. SGMII Interface Pins

Table 3. SGMII Interface Pins

Pin Name	Pin No.	Type	Description
S4RXP	96	AI	SGMII Interface Receive Data Differential Input Pair.
S4RXN	97	AI	
S4TXP	94	AO	SGMII Interface Transmit Data Differential Output Pair.
S4TXN	95	AO	
S5RXP	102	AI	SGMII Interface Receive Data Differential Input Pair.
S5RXN	101	AI	
S5TXP	100	AO	SGMII Interface Transmit Data Differential Output Pair.
S5TXN	99	AO	

5.5.3. QSGMII Interface Pins

Table 4. QSGMII Interface Pins

Pin Name	Pin No.	Type	Description
S0RXP	184	AI	QSGMII Interface Receive Data Differential Input Pair.
S0RXN	185	AI	
S0TXP	182	AO	QSGMII Interface Transmit Data Differential Output Pair.
S0TXN	183	AO	
S1RXP	190	AI	QSGMII Interface Receive Data Differential Input Pair.
S1RXN	189	AI	
S1TXP	188	AO	QSGMII Interface Transmit Data Differential Output Pair.
S1TXN	187	AO	
S2RXP	84	AI	QSGMII Interface Receive Data Differential Input Pair.
S2RXN	85	AI	
S2TXP	82	AO	QSGMII Interface Transmit Data Differential Output Pair.
S2TXN	83	AO	
S3RXP	90	AI	QSGMII Interface Receive Data Differential Input Pair.
S3RXN	89	AI	
S3TXP	88	AO	QSGMII Interface Transmit Data Differential Output Pair.
S3TXN	87	AO	

5.5.4. 1000Base-X/100Base-FX Interface Pins

Table 5. 1000Base-X/100Base-FX Interface Pins

Pin Name	Pin No.	Type	Description
S4RXP	96	AI	1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.
S4RXN	97	AI	
S4TXP	94	AO	1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair.
S4TXN	95	AO	
S5RXP	102	AI	1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.
S5RXN	101	AI	
S5TXP	100	AO	1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair.
S5TXN	99	AO	

5.5.5. Master Mode SPI Flash Interface Pins

Table 6. Master Mode SPI Flash Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SPI_CLK	130	O_{PD}	12	Serial Clock Output Pin.
SPI_SO/SIO1	129	I/O_{PD}	12	In Serial Mode: This is a flash chip output pin In Dual Mode: This is a flash chip bi-directional pin *Note: This is MSB first.*
SPI_SI/SIO0	128	I/O_{PD}	12	In Serial Mode: This is a flash chip input pin In Dual Mode: This is a flash chip bi-directional pin *Note: This is LSB first.*
SPI_CS#0	127	O	12	Chip Select Output Pin. Slave Transmit Enable and active low.

5.5.6. LED Interface Pins

Table 7. LED Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_CLK	122	O_{PU}	12	(1) In Serial LED Mode Reference output clock for serial LED interface and Data is latched on the rising of LEDCK. (2) In SMI-like LED Mode Reference output clock for I2C-like interface.
LED_DAT	123	I/O_{PU}	12	(1) In Serial LED Mode Serial bit stream of link status information. (2) In I2C-like LED Mode The data written to the LED IC.

5.5.7. GPIO Interface Pins

Table 8. GPIO Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
GPIO0	113	I/O_{PD}	4	This pin default set as system LED. Can be configured as General Purpose Input/Output Pin.
GPIO[3:1]	110, 111, 112	I/O_{PD}	4	General Purpose Input/Output Pins.

5.5.8. Configuration Strapping Pins

Table 9. Configuration Strapping Pins

Pin Name	Pin No.	Default	Description
EEPROMTYPE	30	0b0	Select EEPROM Address Byte Size. 0b0: 1-byte 0b1: 2-byte
REG_IF_SEL	124	0b0	Select Switch Core Register Access Interface. 0b0: I2C 0b1: SPI slave Note: RTL8382L doesn't support reg debug interface, this pin should be pulled down.
DIS_PHYAUTO_UP	117	0b0	Disable ASIC Auto Power Up PHY. 0b0: Enable ASIC auto power up PHY 0b1: Disable ASIC auto power up PHY
DIS_EEE	150	0b0	Disable 1000M EEE and 100M EEE Function. 0b0: Enable 0b1: Disable
PWRBLINK[1:0]	152, 151	0b00	Select LED Power On Blinking Timer. 0b00: Disable 0b01:800ms 0b10: 1.6s 0b11: 3.2s
SEL_XTAL_CLK	153	0b0	Select XTAL Input is 25M. 0b0: 25M 0b1:RESERVED
SDS_PDOWN_EN	154	0b0	Enable SerDes Power Down Mode. 0b0: SerDes4/5 operate in normal mode 0b1: SerDes4/5 operate in power down mode
SPI_ADDR_SEL	155	0b0	Select Address Mode for SPI Flash. 0b0: 3-byte address 0b1: 4-byte address
LED_MODE[1:0]	156, 157	0b0	Select LED Mode. 0b00: Serial LED mode 0b01: Scan Single mode 0b10: Scan Bicolor mode 0b11: Disable LED
CPU_SLEEP	166	0b0	Enable CPU Function. 0b0: CPU is always under reset state 0b1: CPU is enabled
MEM_TYPE[1:0]	169, 170	0b00	Select Memory Type for SOC. 0b00: Select SPI flash 0b01: Reserved 0b10: Select SPI flash 0b11: Select EEPROM

Pin Name	Pin No.	Default	Description
CLK_M_EE[1:0]	171, 172	0b00	When MEM_TYPE Select is SPI Flash: This Strapping Pin Selects the Initial Clock for The Memory Controller. 0b00: Reserved for test; 0b01: Reserved for test; 0b10: 100MHz 0b11: Reserved for test; *Note: The initial value for this strapping pin must be set as recommended in the reference design guide.* When MEM_TYPE Select is EEPROM: CLK_M_EE[0] is used to select SOC EEPROM address byte size. 0b0: 1-byte address 0b1: 2-byte address
EN_DECRYPT	173	0b0	Enable or Disable Decrypt for Flash. 0b0: Disable decrypt 0b1: Enable decrypt

5.5.9. Miscellaneous Interface Pins

Table 10. Miscellaneous Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
MDC	120	O_{PU}	12	MII Management Interface Clock Pin.
MDIO	121	I/O_{PU}	12	MII Management Interface Data Pin.
RESET#	114	AI	-	System Pin Reset Input (Low Active). To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled up for normal operation.
XI	106	AI	-	25MHz Crystal Clock Input and Feedback Pin.
XO	105	AO	-	25MHz Crystal Clock Output Pin.
MDIREF	21	AO	-	MDI Bias Resistor. Adjust the reference current for all PHYs. This pin must connect to AGND via a 2.49k ohm resistor.
RTT1	23	AI/O	-	Reserved for Internal Use (Must be Left Floating).
RTT2	24	AI/O	-	Reserved for Internal Use (Must be Left Floating).
VX	179	A	-	Low Voltage Power Control Resistor.
CKOUT0	180	AO	8	25MHz Clock Output.
CKOUT2	80	AO	8	25MHz Clock Output.
CKOUT4	92	AO	8	25MHz Clock Output.
ATESTCK[1:0]	58, 214	AO	-	Reserved for Internal Use (Must be Left Floating).

Pin Name	Pin No.	Type	Drive (mA)	Description
RESERVED	28, 29, 31, 32, 116,118,119, 125, 133, 134, 135, 136, 137, 138, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 158, 159, 161, 164, 165, 167, 168, 174, 175, 176	-	-	Reserved (Must be Left Floating).

5.5.10. Power and Ground Pins

Table 11. Power and Ground Pins

Pin Name	Pin No.	Type	Description
AVDDL	3, 13, 22, 42, 52, 63, 73, 198, 208	AP	Analog Low Voltage Power.
PLLVDDL	57, 213	AP	Analog PLL Low Voltage Power.
AVDDH	8, 14, 19, 25, 36, 41, 47, 68, 78, 193, 203	AP	Analog High Voltage Power.
DVDDL	26, 33, 34, 79, 108, 109, 126, 139, 160, 178, 192	P	Digital Low Voltage Power.
DVDDH	27, 35, 115, 131	P	Digital High Voltage Power.
SVDDL	81, 86, 93, 98, 103, 181, 191	AP	SerDes Low Voltage Power.
AVDDL_PLL	107	AP	PLL Low Voltage Power.
SVDDH	91, 186	AP	SerDes High Voltage Power.
AVDDH_PLL	104	AP	PLL High Voltage Power.
VDDIO	132, 162, 163,177	P	Strapping pin IO Voltage Power.
AGND	20	AG	Analog Ground.
DGND	E-PAD	G	Digital Ground.

6. Switch Function Description

6.1. Hardware Reset and Software Reset

6.1.1. Hardware Reset

A hardware reset forces the RTL8382L-VB to start the initial power-on sequence. First hardware will strap pins to give all default values when the 'RESET' signal terminates. Next the complete SRAM BIST (Built-In Self Test) process is run. Finally the packet buffer descriptors are initialized and internal registers and external CPU will access them.

6.1.2. Software Reset

The RTL8382L-VB supports software queue resets, CPU&Memory reset, and Switch NIC reset. Reset sources are the signals that will trigger the reset command to the chip.

- CPU&Memory Reset: Resets MIPS 4KEc + Memory Controller + Peripheral + NIC
- Switch NIC Reset: Resets the NIC interface between the CPU and Switch

6.2. Crystal

The RTL8382L-VB clock input frequency is 25MHz. When using a crystal, connect a loading capacitor from XI and XO to ground. The maximum Frequency Tolerance is +/-50ppm. Duty cycle should range from 40%~60%.

6.3. IEEE 802.3az Energy Efficient Ethernet (EEE)

The RTL8382L-VB supports IEEE 802.3az Energy Efficient Ethernet (EEE) for 1000Base-T, 100Base-TX in full duplex operation. The Energy Efficient Ethernet (EEE) operational mode combines the IEEE 802.3 Media Access Control (MAC) Sub-layer with a family of Physical Layers defined to support operation in Low Power Idle (LPI) Mode. When Low Power Idle Mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

The RTL8382L-VB EEE operational mode supports IEEE 802.3 MAC operation at 1000Mbps/100Mbps. For 1000Mbps/100Mbps operation, the1000Base-T/ 100Base-TX PHY is supported.

6.4. Layer 2 Learning and Forwarding

The RTL8382L-VB has a 4K-entry VLAN table database.

6.4.1. Forwarding

The VLAN Frame Forwarding Rules are defined as follows:

- The received broadcast/multicast frame will flood to VLAN member ports only, except for the source port

- The received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded

6.4.2. Learning

The RTL8382L-VB features a Layer 2 table (8K entries) that uses a 4-way hash structure to store L2 entries.

The L2 Unicast hash key is {MAC(48bits), VID(12bits)}.

6.5. Port Isolation

The RTL8382L-VB supports the Port Isolation feature. We can control whether the hosts communicate with each other or not by controlling a register value.

If we set the register to cut the connection between hosts, all packets from a host cannot be transmitted to another host directly. These packets can only be transmitted by passing through the router. This feature is called 'Port Isolation'. In Figure 4, Host A and host B connect to the port0 and port3 of the switch, respectively, and port7 is a router. If we set the port isolation enable bit of port0 and port3 to 1, all packets between A and B need to pass through the router (in both directions, A to B and B to A).

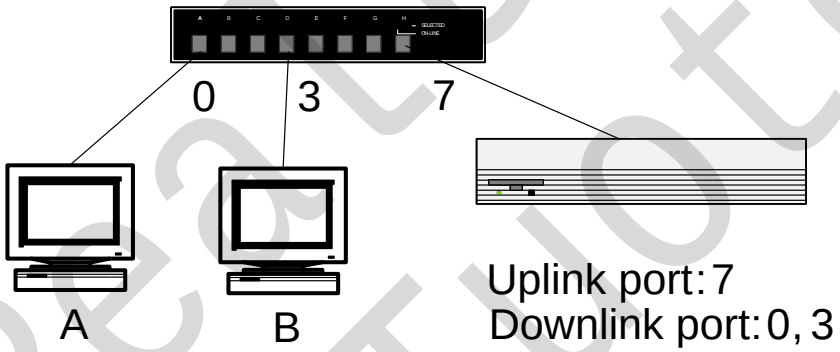


Figure 4. Port Isolation Example

Each port has its own 29 bits port mask configuration. These bits and the TX port list will be mixed to a list. We call this mixed list the final TX port list.

Port isolation port mask settings will affect received packets.

6.6. IEEE 802.3x Flow Control

The RTL8382L-VB supports IEEE 802.3x full duplex flow control. If one port's received frame buffer is over the pause threshold, a pause-on frame is sent to indicate to the link partner to stop the transmission. When a port's received frame buffer drops below the pause threshold, it sends a pause-off frame. The TX pause frame format is shown in Figure 5.

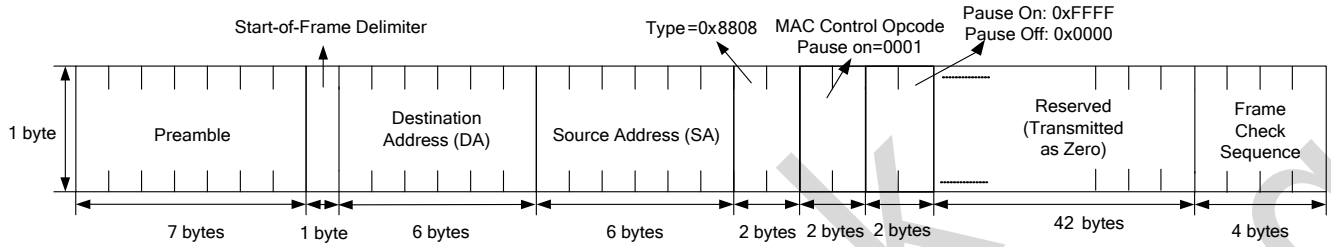


Figure 5. TX Pause Frame Format

The flow control mechanism of the RTL8382L-VB is implemented on the RX side. It counts the received pages on the RX side in order to determine on which port it should send out Pause On/Off packets.

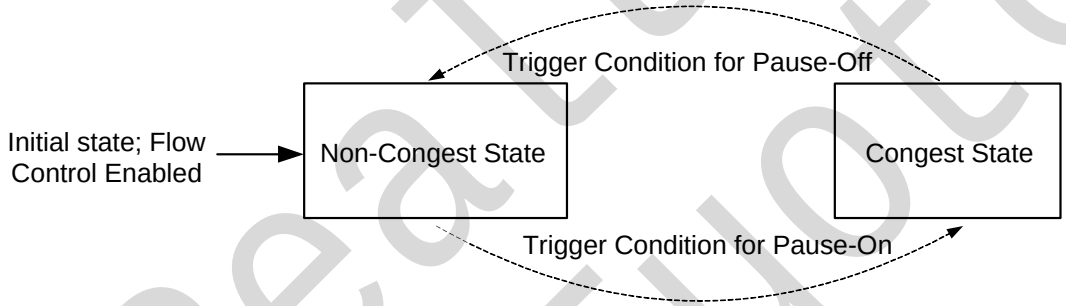


Figure 6. Flow Control State Machine

When RTL8382L-VB flow control is enabled, the initial state is 'Non_Congest'. The state is monitored continuously. If a pause-on trigger condition occurs, it enters the 'Congest' state. When in the 'congest' state, it is also continuously monitored. When a pause-off trigger condition occurs it re-enters the 'Non_Congest' state. Figure 6 shows the flow control state machine.

6.7. Half Duplex Backpressure

There are two mechanisms for half duplex backpressure (Backpressure is for input buffer overflow).

6.7.1. Collision-Based Backpressure (Jam Mode)

If the input buffer is ready to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- When the link partner detects the collision, it waits for a random backoff time. RTL8382L-VB will handle packets that are in the input packet buffer during this time
- RXDV and TXEN will be driven high. The RTL8382L-VB will send a 12-byte Jam signal (pattern is preamble (7bytes) + SFD (1byte) + 0xAA (4bytes)). RTL8382L-VB will then drive TXEN low
- When the link partner (which could be another RTL8382L-VB) receives the Jam signal, it will feedback a 4-byte signal (pattern is derived from the CRC of all transmitted bytes)
- After the RTL8382L-VB receives this jamming signal, it drives RXDV low. The link partner waits for a random backoff time then re-sends the packet. The timing is shown in Figure 7

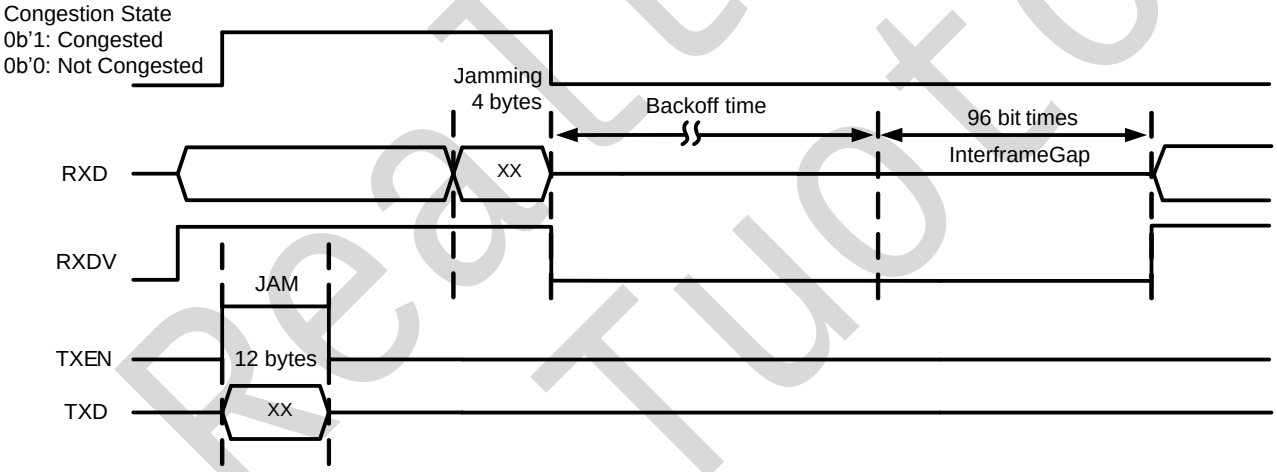


Figure 7. Signal Timing for Collision-Based Backpressure

6.7.2. Carrier-Based Backpressure (I.e., Defer Mode)

If the input buffer is about to overflow, this mechanism will send a fix pattern to defer the other station's transmission. The RTL8382L-VB will continuously send the defer signal until the input buffer overflow is resolved.

6.8. IEEE 802.1p and IEEE 802.1Q (VLAN)

The RTL8382L-VB supports IEEE 802.1Q tag-based VLAN. It supports a 4K-entry VLAN table.

For un-managed switches, there is a register setting to disable tag-based VLANs and force 'no check' for any VLAN settings. If a packet is tagged in, then it is tagged out. If untagged in, then it is untagged out.

6.9. Reserved Multicast Address Handling

There are some Reserved Multicast Address (RMA) definitions in the IEEE 802.1 standard. The RTL8382L-VB includes 01-80-C2-00-00-00 to 01-80-C2-00-00-2F RMA support and provides user defined RMA settings. For each RMA, the actions include: Table lookup, Drop, Trap to CPU, and always Flood. The action priority is higher than the results of a L2 Table lookup.

6.10. Layer 2 Traffic Suppression (Storm Control)

The per-port L2 storm filtering control mechanism suppresses the flow rate of some specific packets. The RTL8382L-VB supports three control types: Unknown Unicast Storm, Unknown Multicast Storm, and Broadcast Storm. Each port has control registers to enable or disable the storm filtering function. These three traffic type definitions are:

- Unknown Unicast: If the I/G bit of the packet's destination address is 0, it is a unicast packet and its DA look-up in the L2 unicast table failed. I.e., the packet's destination address is unknown
- Unknown Multicast: If the I/G bit of the packet's destination address is 1, it is a multicast packet and its DA look-up in the L2 unicast table failed, i.e., the packet's destination address is unknown
- Broadcast: DMAC = FF-FF-FF-FF-FF-FF indicates this is a broadcast packet

The traffic rate for these three types can be set on a per-port basis.

6.11. IEEE 802.3ad Link Aggregation Protocol

The RTL8382L-VB supports 802.3ad (Link Aggregation) for 8 groups of link aggregators with up to 8 ports per-group.

Frame Distribution

Link aggregation group frames are sent to an aggregation port of the link aggregation group according to a hash algorithm. There are seven parameters (DMAC, SMAC, SPA, SIP, DIP, SPORT, DPROT).

7. CPU Function Description

7.1. SPI Flash

The RTL8382L-VB support 32M-Byte (max) serial I/O, dual I/O SPI Flash.

8. Interface Descriptions

8.1. QSGMII

QSGMII-plus (Quad Serial Gigabit Media Independent Interface) reduces PCB complexity and IC pin count. This innovative 5Gbps serial interface provides an up to 10 inch MAC to PHY communication path. QSGMII can carry the full duplex gigabit Ethernet data streams of four ports simultaneously, using only 4 pins.

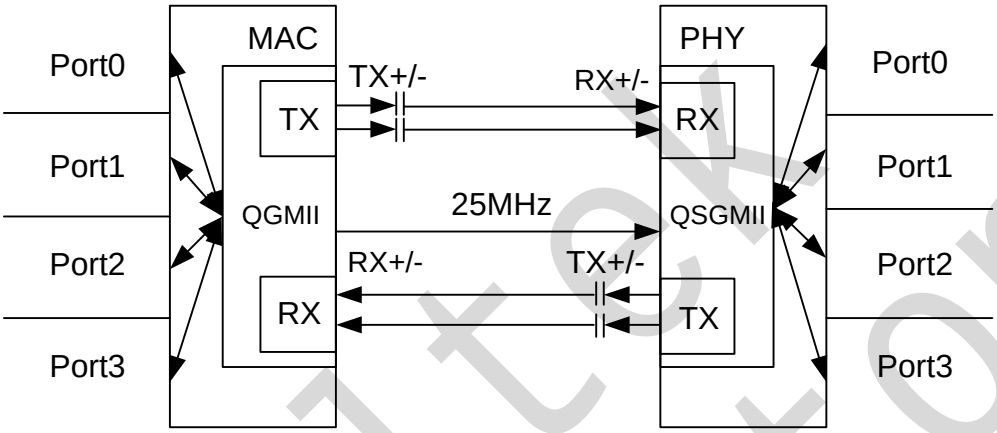


Figure 8. QSGMII Interconnection

8.2. SGMII

SGMII (Serial Gigabit Media Independent Interface) conveys PHY and MAC data with significantly less pins than required for GMII. It operates in both half and full duplex, and at all port speeds. It includes 4 data signals and 2 CLK signals to convey frame data and link rate information between the PHY and MAC. The data signals operate at 1.25Gbaud, and the CLK operates at 625MHz. Each of these signals is carried as a differential pair, thus providing signal integrity while minimizing system noise.

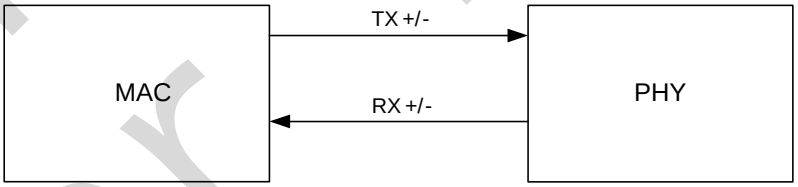


Figure 9. SGMII Signal

8.3. SPI Flash Interface

RTL8382L-VB support SPI Flash with the following features:

- Supports serial I/O, dual I/O SPI Flash (max)

- Supports both MMIO (Memory Mapped I/O) and PIO (Programmed I/O) mode
- One chip selection
- Supports maximum 32M Bytes SPI Flash in PIO mode and 16M Bytes in MMIO mode

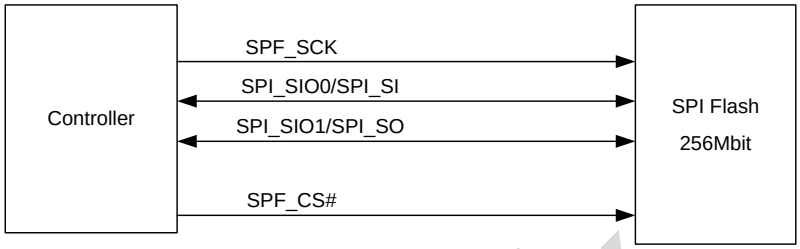


Figure 10. SPI Flash Configuration

8.4. Serial LED

The RTL8382L-VB supports a serial LED interface to display the link status. The serial LED interface, LED_CK and LED_DA provide clock and data to enable/disable the external shift registers. A 74HC164 8-Bit Serial-In, Parallel-Out Shift Register captures the per-port link status and diagnostic information. In serial shift LED mode, the RTL8382L-VB supports per-port one/two/three single-color LED to show the speed, link status, and other information.

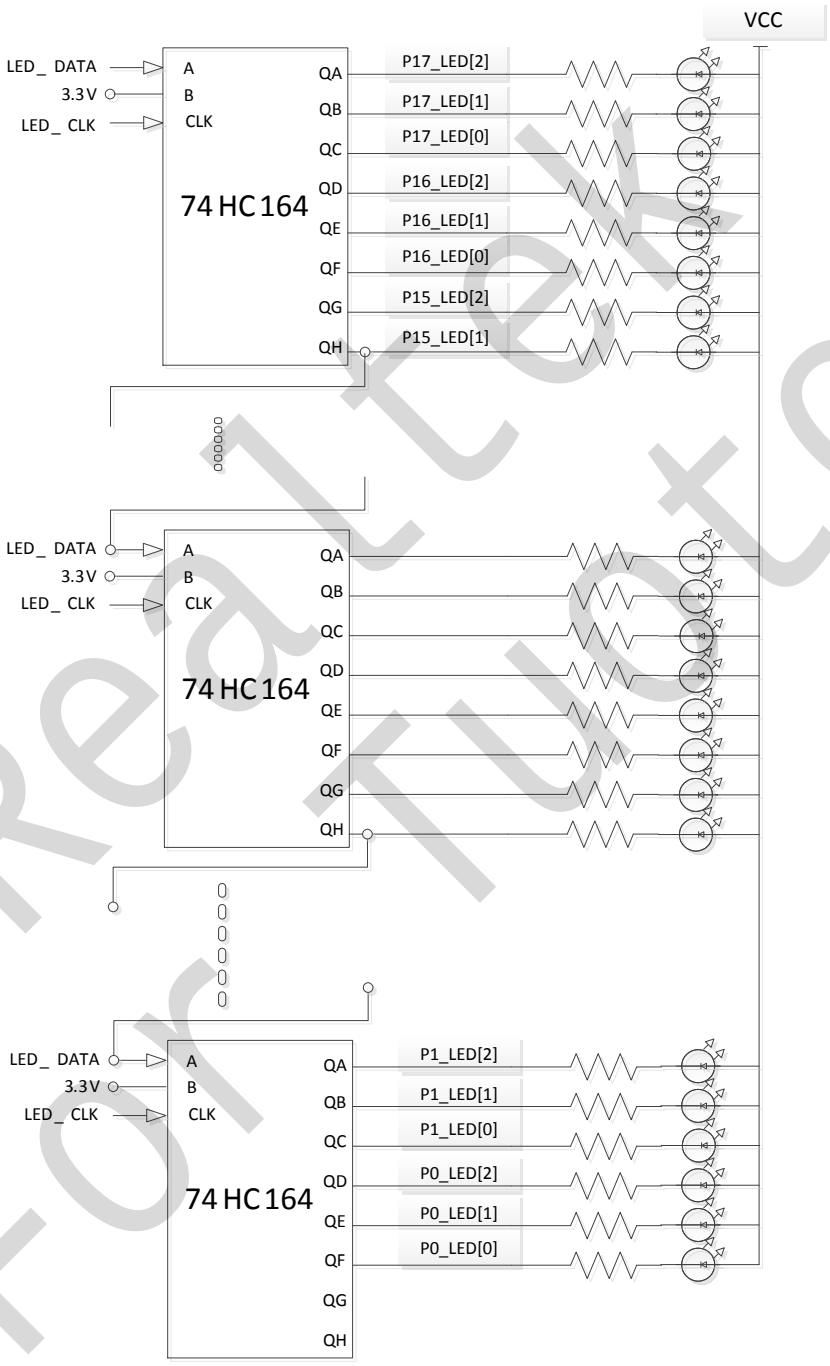


Figure 11. Serial LED Connection

The default LED status for the RTL8382L-VB is as follows:

LED Number	3-LEDs
LED0 Definition	1000M Link
LED1 Definition	100M Link
LED2 Definition	Link/Act

9. Electrical AC/DC Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified referenced to GND unless otherwise specified.

Table 12. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDH, AVDDH, SVDDH, AVDDH_PLL Supply Referenced to DGND and AGND	2.97	3.63	V
DVDDL, AVDDL, SVDDL, AVDDL_PLL, PLLVDDL Supply Referenced to DGND and AGND	0.90	1.18	V
VDDIO	1.875(2.5)	2.625(2.5)	V
	1.350(1.5)	1.732(1.5)	V

9.2. Operating Range

Table 13. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature (Ta)	0	-	55	°C
DVDDH, AVDDH, SVDDH, AVDDH_PLL Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL, AVDDL_PLL, PLLVDDL Supply Voltage Range	0.95	1.1	1.15	V
SVDDL Supply Voltage Range	1.05	1.1	1.15	V
VDDIO	1.875	2.5	2.625	V
	1.350	1.5	1.732	V

9.3. DC Characteristics

Table 14. DC Characteristics (IO Power =3.3V)

Symbol	Parameter	Min	Typical	Max	Units
V_{IH}	TTL Input High Voltage	2.0	-	-	V
V_{IL}	TTL Input Low Voltage	-	-	0.8	V
V_{OH}	Output High Voltage	2.4	-	-	V
V_{OL}	Output Low Voltage	-	-	0.4	V

9.4. AC Characteristics

9.4.1. QSGMII Differential Transmitter Characteristics

Table 15. QSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	199.94	200	200.06	ps	200ps ±300ppm
T_X1	Eye Mask	-	-	0.2	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	150	-	-	mV	-
T_Y2	Eye Mask	-	-	650	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	600	900	1300	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.6	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.4	UI	-
$T_{TX-RISE}$	Output Rise Time	0.15	-	-	UI	-
$T_{TX-FALL}$	Output Fall Time	0.15	-	-	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

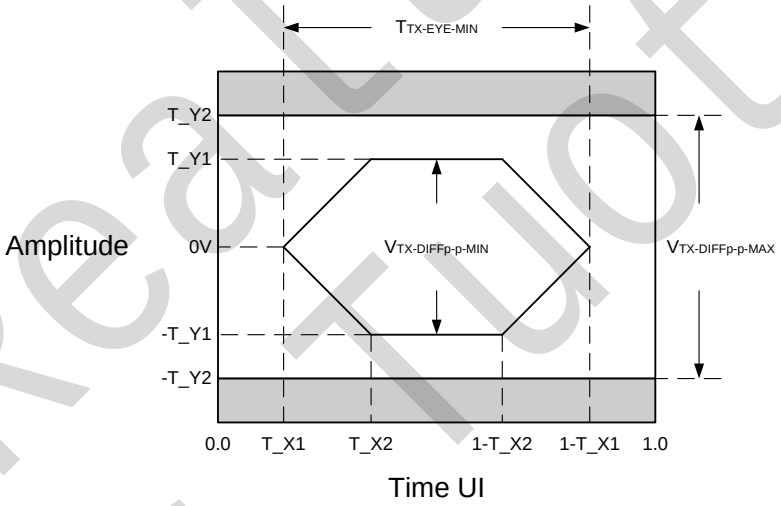


Figure 12. QSGMII Differential Transmitter Eye Diagram

9.4.2. QSGMII Differential Receiver Characteristics

Table 16. QSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	199.94	200	200.06	ps	200ps ±300ppm
R_X1	Eye Mask	-	-	0.3	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	650	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	1300	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.4	-	-	UI	-

Symbol	Parameter	Min	Typical	Max	Units	Notes
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.6	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

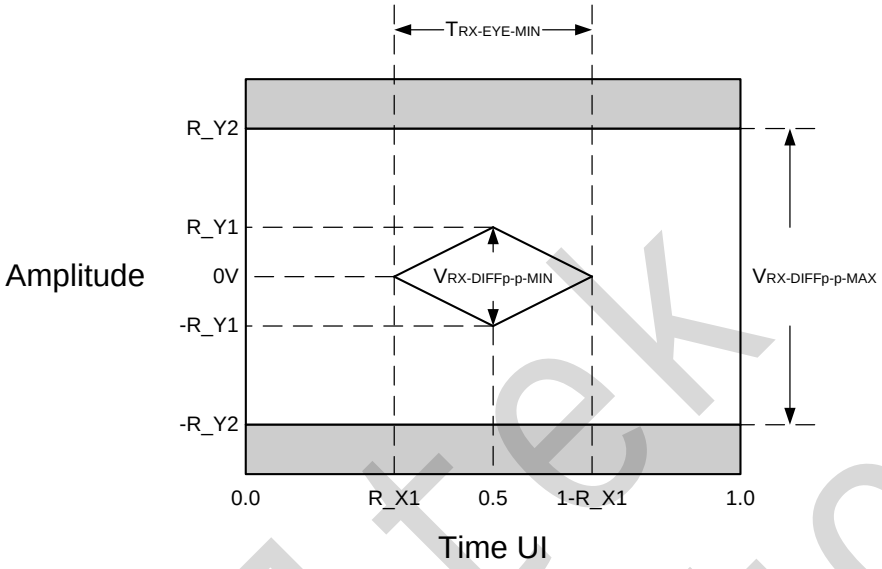


Figure 13. QSGMII Differential Receiver Eye Diagram

9.4.3. SGMII Differential Transmitter Characteristics

Table 17. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ±300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	125	-	-	mV	-
T_Y2	Eye Mask	-	-	500	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

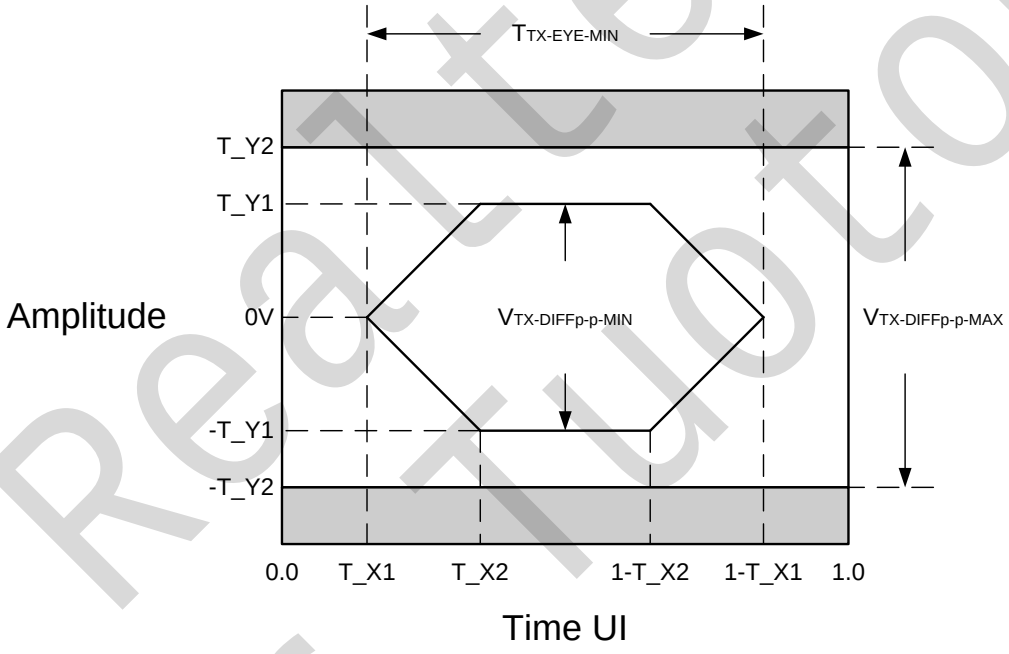


Figure 14. SGMII Differential Transmitter Eye Diagram

9.4.4. SGMII Differential Receiver Characteristics

Table 18. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ±300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

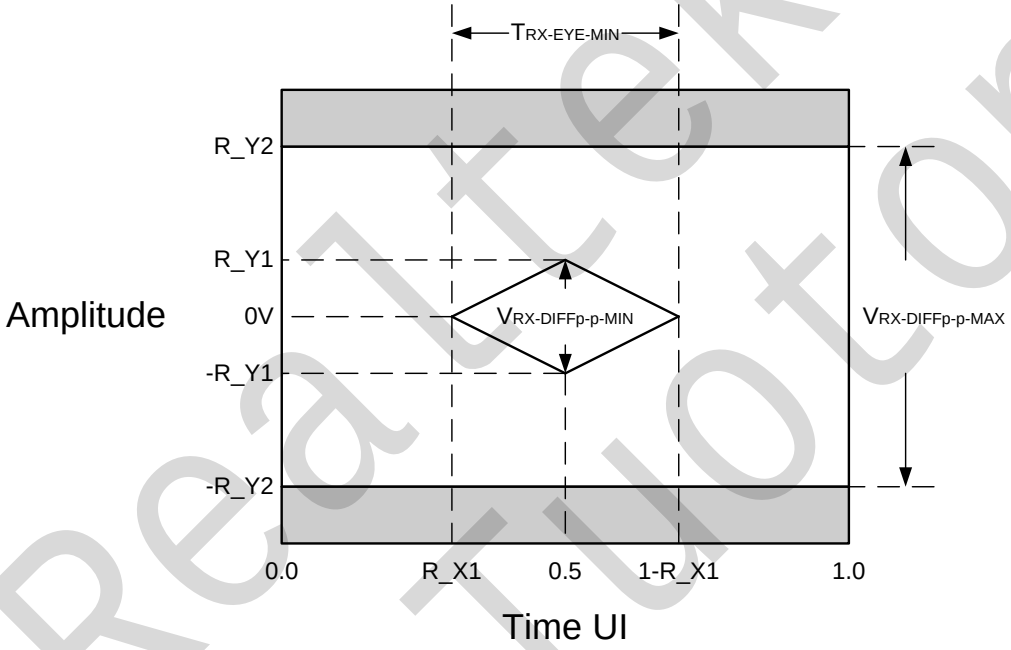


Figure 15. SGMII Differential Receiver Eye Diagram

9.4.5. 1000Base-X/100Base-FX Differential Transmitter Characteristics

Table 19. 1000Base-X/100Base-FX Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval (1000Base-X)	799.76	800	800.24	ps	800ps ±300ppm
	Unit Interval (100Base-FX)	7.9976	8.0	8.0024	ns	8ns ±300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	125	-	-	mV	-
T_Y2	Eye Mask	-	-	650	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	800	1300	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

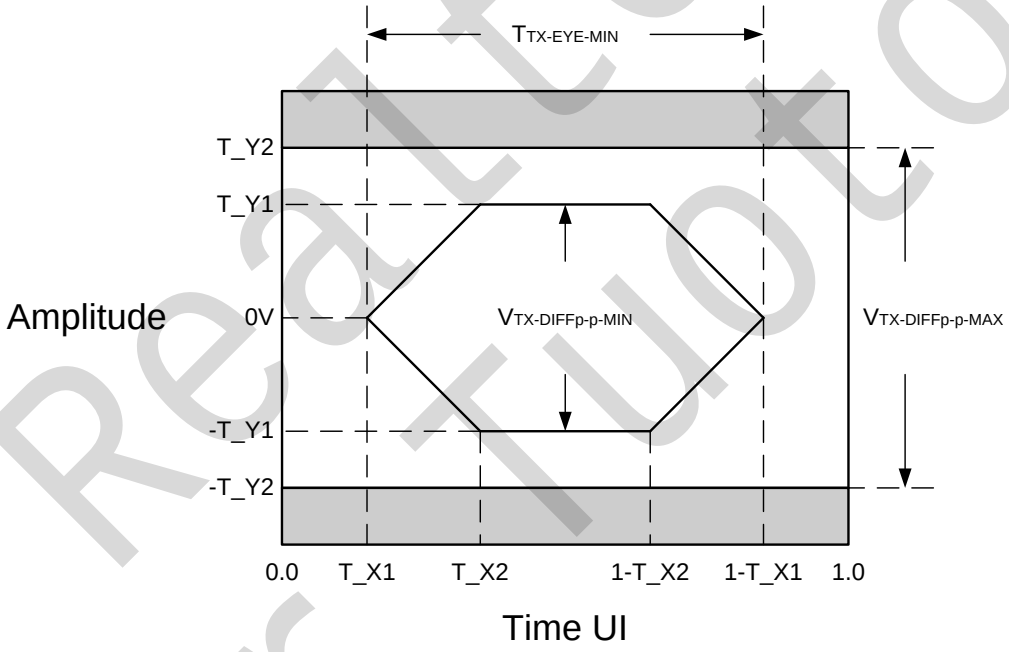


Figure 16. 1000Base-X/100Base-FX Differential Transmitter Eye Diagram

9.4.6. 1000Base-X/100Base-FX Differential Receiver Characteristics

Table 20. 1000Base-X/100Base-FX Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval (1000Base-X)	799.76	800	800.24	ps	800ps ±300ppm
	Unit Interval (100Base-FX)	7.9976	8.0	8.0024	ns	8ns ±300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

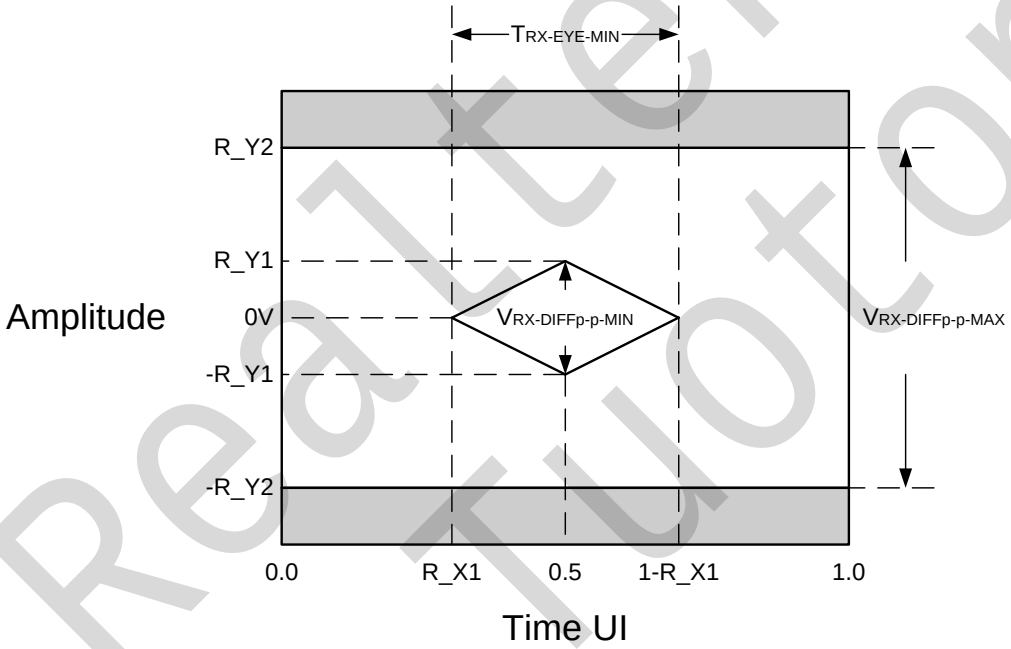


Figure 17. 1000Base-X/100Base-FX Differential Receiver Eye Diagram

9.4.7. SPI Interface Characteristics

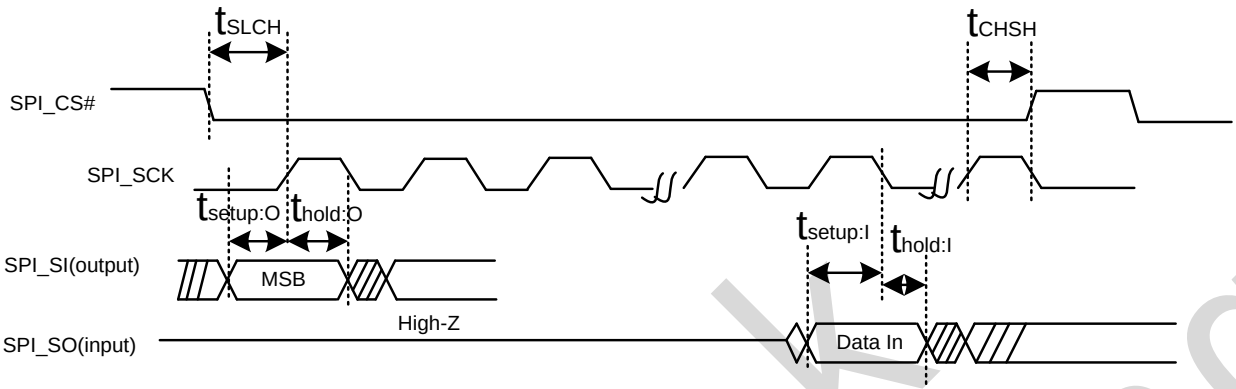


Figure 18. SPI Interface Timing

Table 21. SPI Interface Timing Characteristics

Symbol	Description	Min	Typical	Max	Units
f_{SPI_SCK}	Clock Frequency of the SPI_SCK	49.5	50	50.5	MHz
Duty	Duty Cycle of the SPI_SCK	45	50	55	%
t_{SLCH}	CS# Active Setup Time	7	8.1	-	ns
t_{CHSH}	CS# Active Hold Time	8	9.65	-	ns
$t_{setup:O}$	Data Output Setup Time	4	8.3	-	ns
$t_{hold:O}$	Data Output Hold Time	6	9.65	-	ns
$t_{setup:I}$	Data Input Setup Time	4	-	-	ns
$t_{hold:I}$	Data Input Hold Time	0	-	-	ns

Note: Test Condition, fSPI_SCK=50MHz.

9.4.8. SMI (MDC/MDIO) Interface Characteristics

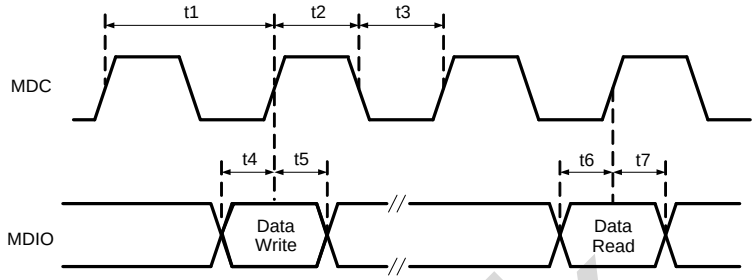


Figure 19. SMI (MDC/MDIO) Timing

Table 22. SMI (MDC/MDIO) Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	380	-	-	ns
t2	MDC High Time	-	190	-	ns
t3	MDC Low Time	-	190	-	ns
t4	MDIO to MDC Rising Setup Time (Write Data)	-	190	-	ns
t5	MDIO to MDC Rising Hold Time (Write Data)	-	190	-	ns
t6	MDIO to MDC Rising Setup Time (Read Data)	40	-	-	ns
t7	MDIO to MDC rising hold time (Read Data)	2	-	-	ns

9.4.9. Serial Mode LED

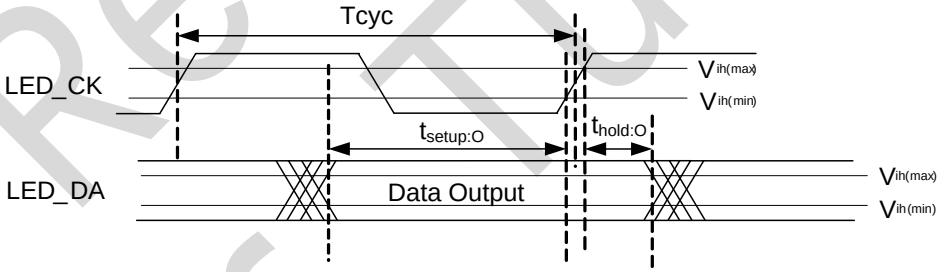


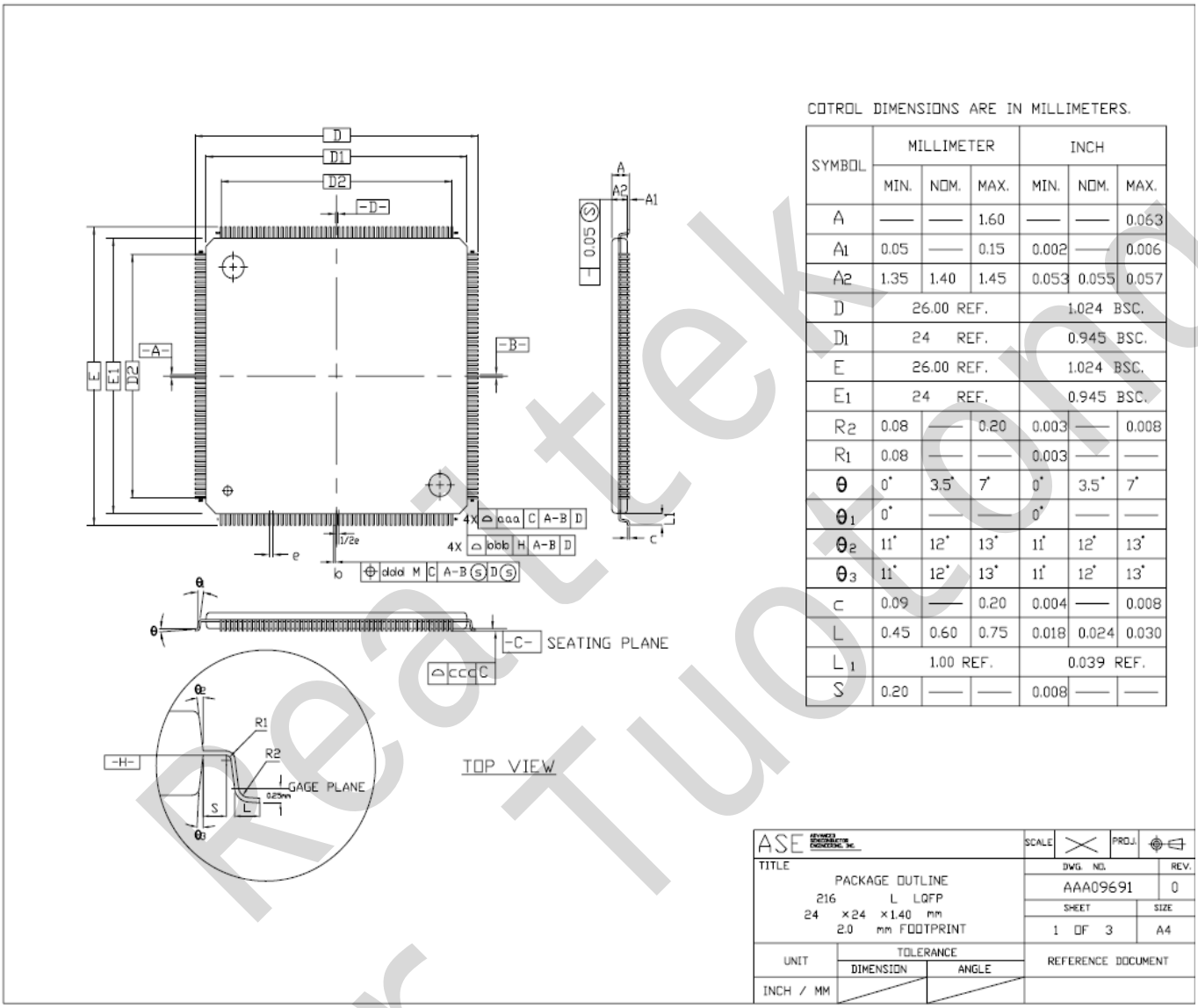
Figure 20. Serial Mode LED AC Timing Parameters

Table 23. Serial Mode LED AC Timing

Mode and Description		Symbol	Min	Typical	Max	Units
Serial LED	Input High Voltage	Vih	2.0	-	-	V
	Input Low Voltage	Vil	-	-	0.8	V
	LED_CK Clock Cycle	Tcyc	-	600	-	ns
	Duty Cycle of the LED_CK	Duty	45	50	55	%
	LED_DA to LED_CK Output Setup Time	$t_{setup:O}$	-	314	-	ns
	LED_DA to LED_CK Output Hold Time	$t_{hold:O}$	-	285	-	ns

10. Package Information

*10.1. LQFP216-E-PAD (24*24mm)*



CONTROL DIMENSIONS ARE IN MILLIMETERS.

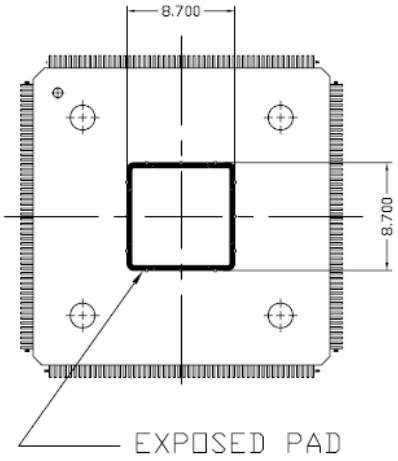
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	——	——	1.60	——	——	0.063
A1	0.05	——	0.15	0.002	——	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D		26.00 REF.			1.024 BSC.	
D1		24 REF.			0.945 BSC.	
E		26.00 REF.			1.024 BSC.	
E1		24 REF.			0.945 BSC.	
R2	0.08	——	0.20	0.003	——	0.008
R1	0.08	——	——	0.003	——	——
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	——	——	0°	——	——
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	——	0.20	0.004	——	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF.			0.039 REF.	
S	0.20	——	——	0.008	——	——

ASE SCALE PROJ.

TITLE: PACKAGE OUTLINE
216 L LQFP
24 ×24 ×1.40 mm
2.0 mm FOOTPRINT

DWG. NO. AAA09691 REV. 0
SHEET 1 OF 3 SIZE A4

UNIT: INCH / MM
TOLERANCE: DIMENSION / ANGLE
REFERENCE DOCUMENT



BOTTOM VIEW

SYMBOL	216L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e		0.40 BSC.			0.016 BSC.	
D2		21.20			0.835	
E2		21.20			0.835	
TOLERANCES OF FORM AND POSITION						
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.08			0.003	
ddd		0.07			0.003	

NOTES :
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. THE MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.
3. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.

ASE	SCALE: X	PROJ.	
TITLE: PACKAGE OUTLINE 216 L LQFP 24 x24 x1.40 mm 2.0 mm FOOTPRINT		DWG. NO. AAA09691	REV. 0
		SHEET 2 OF 3	SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	

11. Ordering Information

Table 24. Ordering Information

Part Number	Package	Status
RTL8382L-VB-CG	LQFP 216-Pin E-PAD (24*24mm) 'Green' Package (Un-Managed)	MP

Note: See page 32 (RTL8382L-VB) for package identification.

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