NOT FOR PUBLIC RELEASE

RTL8364NB-CG

LAYER 2 MANAGED 2+2-PORT 10/100/1000M SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.1
16 January 2017
Track ID: JATR-8275-15

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211 Fax: +886-3-577-6047
www.realtek.com

COPYRIGHT

DISCLAIMER

Realtek provides this document 'as is', without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8364NB IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2016/09/06	First release.
1.1	2017/01/16	Revised Table 13 Miscellaneous Pins, page 21 (nReset Description). Revised Table 26 PCS Register (PHY 0~4), page 49 (PHY Identifier 2 default value) Revised Table 30 Register 3: PHY Identifier 2, page 52 (Default values) Revised Table 36 Register 9: 1000Base-T Control Register, page 55 (register 9 bit 8 mode). Revised Figure 38 Power and Reset Characteristics, page 73. Revised Table 58 Power and Reset Timing Requirements, page 73. Added Table 59 Power Monitor Reset Characteristics, page 73.

Table of Contents

List of Tables

List of Figures

1. General Description

The RTL8364NB-CG is a QFN88, high-performance 2+2-port 10/100/1000M Ethernet switch featuring a low-power integrated 2-port Giga-PHY that supports 1000Base-T, 100Base-TX, and 10Base-T.

For specific applications, the RTL8364NB supports two extra interfaces that could be configured as RGMII/MII interfaces. The RTL8364NB integrates all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8364NB features superior memory management technology to efficiently utilize memory space. The RTL8364NB integrates a 2K-entry look-up table with a 4-way XOR hashing algorithm for address searching and learning. The table provides read/write access from the EEPROM Serial Management Interface (SMI), Media Independent Interface Management (MIIM), or SPI Interface. Each of the table entries can be configured as a static entry. The entry aging time is between 200 and 400 seconds. Eight Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB implement dual RGMII/MII interfaces. These interfaces could be connected to an external PHY, MAC, CPU, or RISC for specific applications. In router applications, the RTL8364NB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. When using this function, VID information carried in the VLAN tag will be changed to PVID.

Note: The RTL8364NB Extra Interface (Extension GMAC1 and Extension GMAC2) supports:

Dual-Port Reduced Gigabit Media Independent Interface (RGMII)

Dual-Port Media Independent Interface (MII)

The RTL8364NB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8364NB supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast applications, the RTL8364NB supports IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping.

In order to support flexible traffic classification, the RTL8364NB supports 96-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, force output tag format and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

In Bridge operation the RTL8364NB supports 16 sets of port configurations: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol. To meet security and management application requirements, the RTL8364NB supports IEEE 802.1x Port-based/MAC-based Access Control. For those ports that do not pass IEEE 802.1x authentication, the RTL8364NB provides a Port-based/MAC-based Guest VLAN function for them to access limited network resources. A 1-set Port

Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time or multimedia networking applications, the RTL8364NB supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or mixed.

The RTL8364NB provides a 4K-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8364NB supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or EEPROM SMI Slave after reset.

In router applications, the router may want to know the input port of the incoming packet. The RTL8364NB supports an option to insert a VLAN tag with VID=Port VID (PVID) on each egress port. The RTL8364NB also provides an option to admit VLAN tagged packet with a specific PVID only. If this function is enabled, the RTL8364NB will drop all non-tagged packets and packets with an incorrect PVID.

2. Features

- Single-chip 2+2-port 10/100/1000M non-blocking switch architecture
- Embedded 2 -port 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Extra Interface (Extension GMAC1 and Extension GMAC2) supports
  - Dual-port Media Independent Interface (MII)
  - Dual-port Reduced 10/100/1000M Media Independent Interface (RGMII)
- Supports High Speed Serial Interface (Extension GMAC1)
  - SGMII (1.25GHz) Interface
  - High SGMII (3.125GHz) Interface
- Supports High Speed Serial Interface (Extension GMAC1)
  - SGMII (1.25GHz) Interface
  - HSGMII (3.125GHz) Interface
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Realtek Cable Test (RTCT) function
- Supports 96-entry ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions include mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment GPIO control, force output tag format, interrupt and logging counter
  - Supports five types of user defined ACL rule format for 96 ACL rules
  - Optional per-port enable/disable of ACL function
  - Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
  - Supports 4K VLANs and 32 Extra Enhanced VLANs
  - Supports Un-tag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
  - 2K-entry MAC address table with 4-way hash algorithm
  - Up to 2K-entry L2/L3 Filtering Database
  - Per-port MAC learning limitation
  - System base MAC learning limitation
- Supports Spanning Tree Port Behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Supports Auto protection from Denial-of-Service attacks

- Supports H/W IGMP/MLD Snooping
  - IGMPv1/v2/v3 and MLD v1/v2
  - Supports Fast Leave
  - Static router port configuration
  - Dynamic router port learning and aging
- Supports Quality of Service (QoS)
  - Supports per port Input Bandwidth Control
  - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority and SVLAN based priority
  - Eight Priority Queues per port
  - Per queue flow control
  - Min-Max Scheduling
  - Strict Priority and Weighted Fair Queue (WFQ) to provide minimum bandwidth
  - One leaky bucket to constrain the average packet rate of each queue
- Supports rate limiting (32 shared meters, with 8kbps granulation or packets per second configuration)
- Supports RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
- Supports Stacking VLAN and Port Isolation with eight Enhanced Filtering Databases
- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLANs
  - Supports 32 L2/IPv4 Multicast mappings to SVLAN
  - Supports MAC-based 1:N VLAN
- Supports two IEEE 802.3ad Link aggregation port groups
- Supports Port Mirror function for one monitor port for multiple mirroring ports
- Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol
- Supports Loop Detection
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports IEEE 802.3az Energy Efficient Ethernet (EEE)
- Supports Realtek Green Ethernet features
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving
- Supports one interrupt output to external CPU for notification
- Each port supports 3 LED outputs
- Management Interface Supports
  - EEPROM SMI Slave interface
  - Media Independent Interface Management (MIIM)
  - SPI Slave Interface
- Supports 32K-byte EEPROM space for configuration
- Integrated 8051 microprocessor.
- 25MHz crystal or 3.3V OSC input
- 10x10 QFN 88-pin package

3. System Applications

- 2-Port 1000Base-T Router with Dual MII/RGMII

4. Application Examples

4.1. 2-Port 1000Base-T Router with Dual MII/RGMII

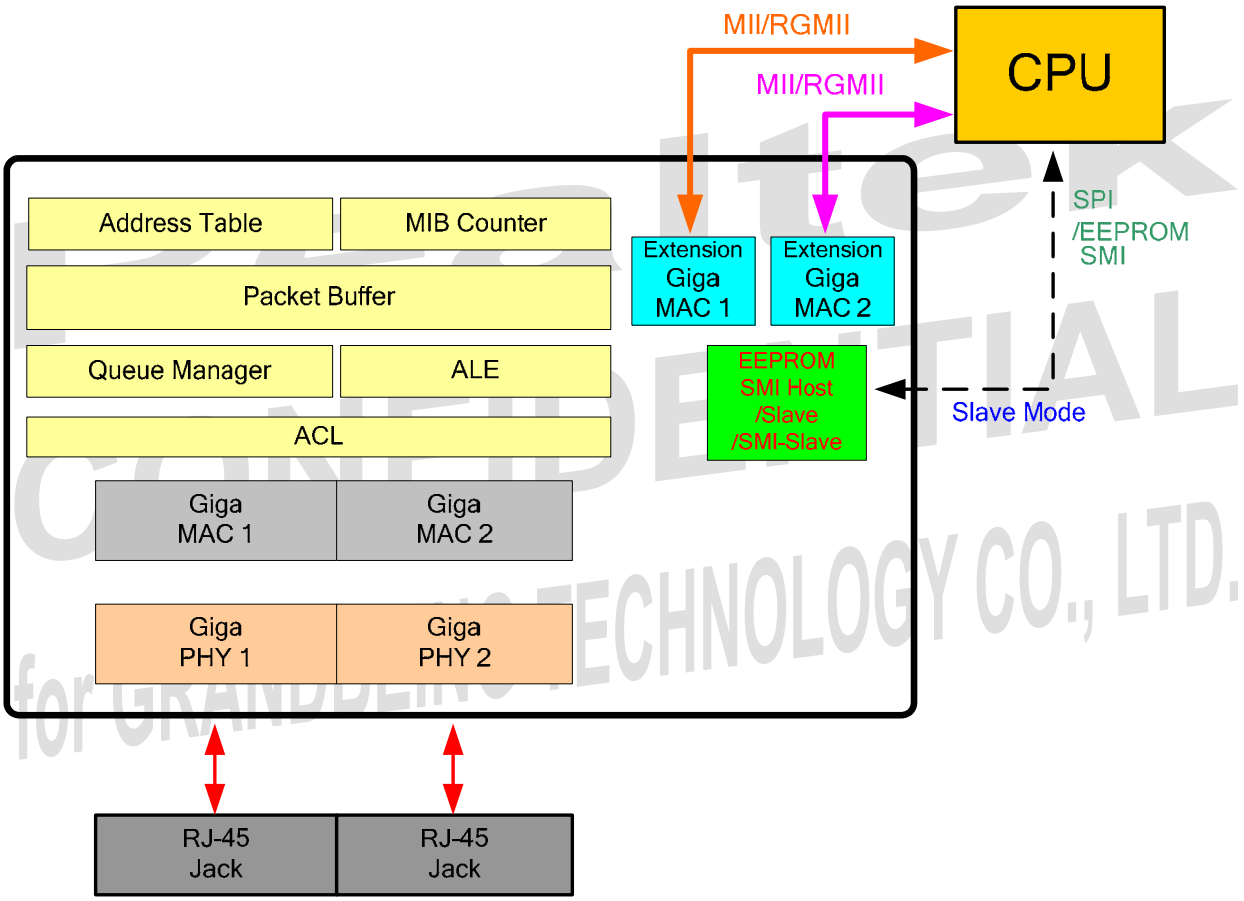


Figure 1. 2-Port 1000Base-T Router with Dual MII/RGMII

Note: Extra Interface (Extension GMAC1 and Extension GMAC2) in MII/RGMII Mode.

5. Block Diagram

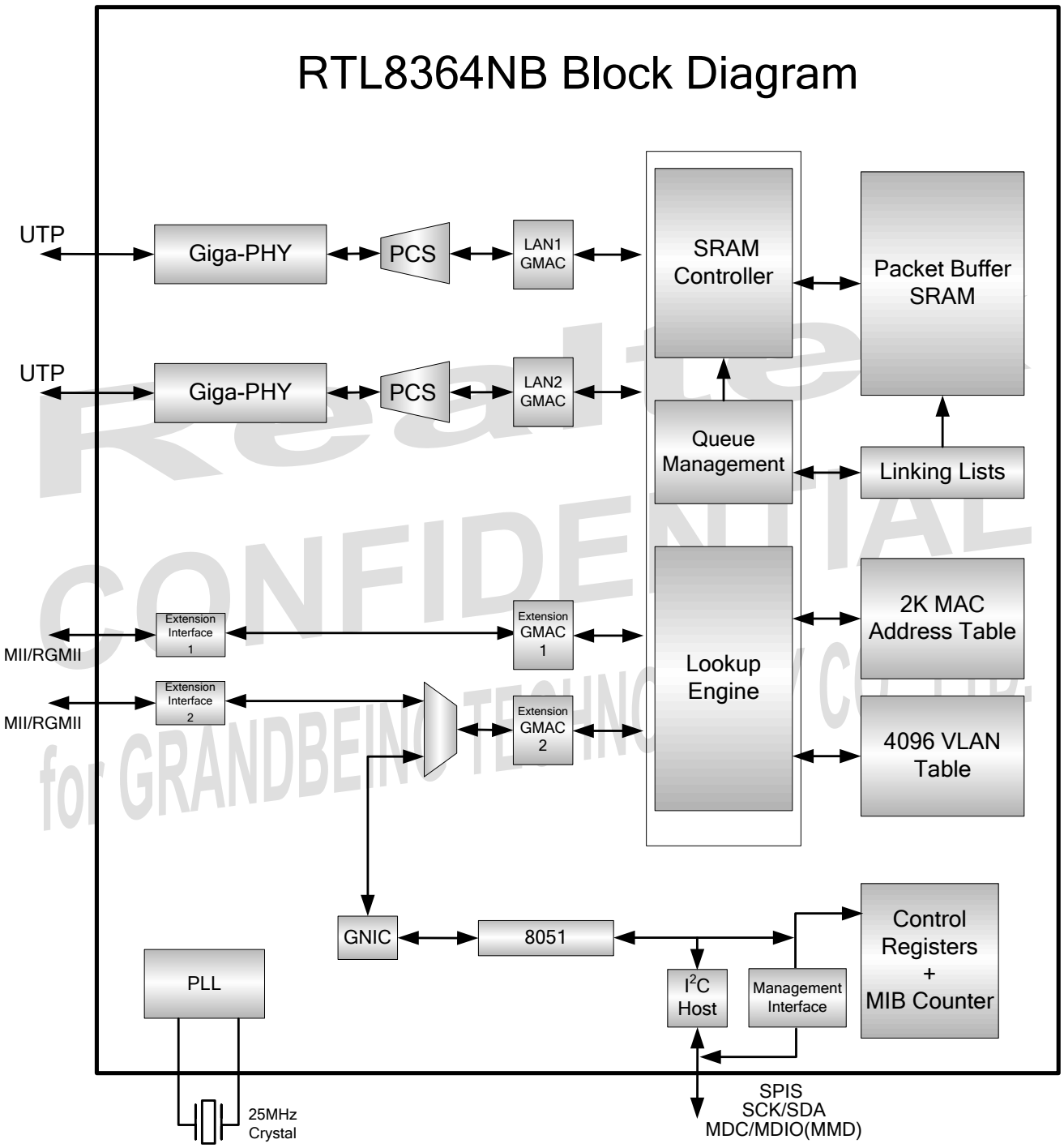


Figure 2. Block Diagram

6. Pin Assignments

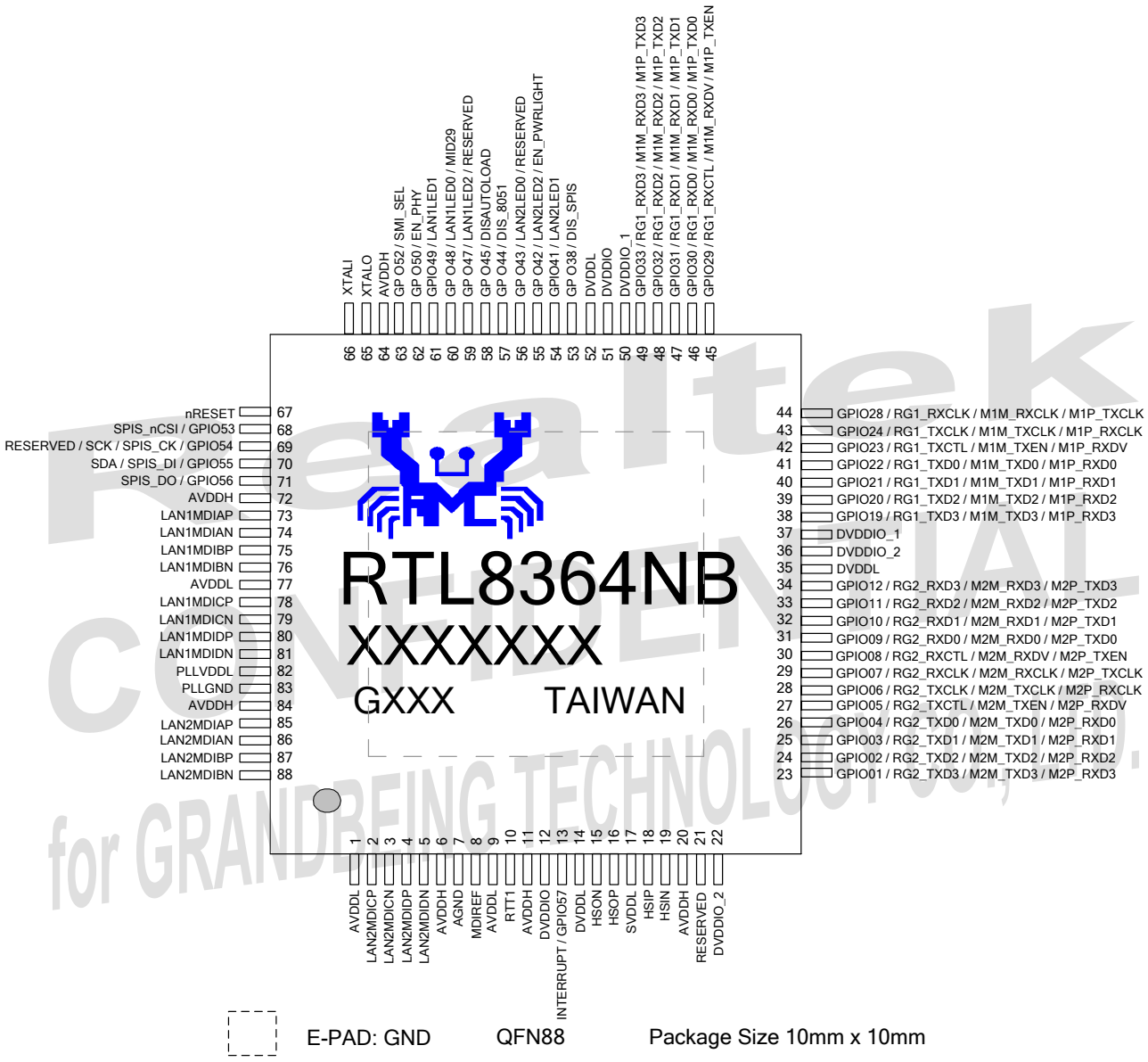


Figure 3. Pin Assignments (QFN-88)

6.1. Package Identification

Green package is indicated by the 'G' in GXXX (Figure 3).

6.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

I_S: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Assignments Table

Name	Pin No.	Type
AVDDL	1	AP
LAN2MDICP	2	AI/O
LAN2MDICN	3	AI/O
LAN2MDIDP	4	AI/O
LAN2MDIDN	5	AI/O
AVDDH	6	AP
AGND	7	AG
MDIREF	8	AO
AVDDL	9	AP
RTT1	10	AO
AVDDH	11	AP
DVDDIO	12	P
GPIO57/INTERRUPT	13	I/O_{PD}
DVDDL	14	P
HSON	15	AO
HSOP	16	AO
SVDDL	17	AP
HSIP	18	AI
HSIN	19	AI
AVDDH	20	AP
RESERVED	21	AO
DVDDIO_2	22	P
GPIO01/E2_DO3/RG2_TXD3 /M2M_TXD3/M2P_RXD3	23	I/O

Name	Pin No.	Type
GPIO02/E2_DO2/RG2_TXD2 /M2M_TXD2/M2P_RXD2	24	I/O
GPIO03/E2_DO1/RG2_TXD1 /M2M_TXD1/M2P_RXD1	25	I/O
GPIO04/E2_DO0/RG2_TXD0 /M2M_TXD0/M2P_RXD0	26	I/O
GPIO05/E2_DOEN/RG2_TXCTL/ M2M_TXEN/M2P_RXDV	27	I/O
GPIO06/E2_DOCLK/RG2_TXCLK /M2M_TXCLK/M2P_RXCLK	28	I/O
GPIO07/E2_DICLK/RG2_RXCLK/ M2M_RXCLK/M2P_TXCLK	29	I/O
GPIO08/E2_DIDV/RG2_RXCTL /M2M_RXDV/M2P_TXEN	30	I/O
GPIO09/E2_DI0/RG2_RXD0 /M2M_RXD0/M2P_TXD0	31	I/O
GPIO10/E2_DI1/RG2_RXD1 /M2M_RXD1/M2P_TXD1	32	I/O
GPIO11/E2_DI2/RG2_RXD2/M2M _RXD2/M2P_TXD2	33	I/O
GPIO12/E2_DI3/RG2_RXD3/M2M _RXD3/M2P_TXD3	34	I/O
DVDDL	35	P
DVDDIO_2	36	P
DVDDIO_1	37	P

Name	Pin No.	Type
GPIO19/E1_DO3/RG1_TXD3 /M1M_TXD3/M1P_RXD3	38	I/O
GPIO20/E1_DO2/RG1_TXD2/M1 M_TXD2/M1P_RXD2	39	I/O
GPIO21/E1_DO1/RG1_TXD1/M1 M_TXD1/M1P_RXD1	40	I/O
GPIO22/E1_DO0/RG1_TXD0/M1 M_TXD0/M1P_RXD0	41	I/O
GPIO23/E1_DOEN/RG1_TXCTL /M1M_TXEN/M1P_RXDV	42	IO
GPIO24/E1_DOCLK/RG1_TXCLK /M1M_TXCLK/M1P_RXCLK	43	I/O
GPIO28/E1_DICLK/RG1_RXCLK /M1M_RXCLK/M1P_TXCLK	44	I/O
GPIO29/E1_DIDV/RG1_RXCTL /M1M_RXDV/M1P_TXEN	45	I/O
GPIO30/E1_DI0/RG1_RXD0 /M1M_RXD0/M1P_TXD0	46	I/O
GPIO31/E1_DI1/RG1_RXD1 /M1M_RXD1/M1P_TXD1	47	I/O
GPIO32/E1_DI2/RG1_RXD2 /M1M_RXD2/M1P_TXD2	48	I/O
GPIO33/E1_DI3/RG1_RXD3 /M1M_RXD3/M1P_TXD3	49	I/O
DVDDIO_1	50	P
DVDDIO	51	P
DVDDL	52	P
GP O38/DIS_SPIS	53	I/O_{PU}
GPIO41/LAN2LED1	54	I/O_{PU}
GP O42/LAN2LED2 /EM_PWRLIGHT	55	I/O_{PU}
GPO43/LAN2LED0/ RESERVED	56	I/O_{PU}
GP O44/DIS_8051	57	I/O_{PU}
GP O45/DISAUTOLOAD	58	I/O_{PU}

Name	Pin No.	Type
GP O47/LAN1LED2/RESERVED	59	I/O_{PU}
GP O48/LAN1LED0/MID29	60	I/O_{PU}
GPIO49/LAN1LED1	61	I/O_{PU}
GP O50/EN_PHY	62	I/O_{PU}
GP O52/SMI_SEL	63	I/O_{PU}
AVDDH	64	AP
XTALO	65	AO
XTALI	66	AI
nRESET	67	I_{PU}
GPIO53/SPIS_nCSI	68	I/O_{PU}
GPIO54/SPIS_CK/SCK/MDC/ RESERVED	69	I/O
GPIO55/SPIS_DI/SDA/MDIO	70	I/O
GPIO56/SPIS_DO	71	I/O
AVDDH	72	AP
LAN1MDIAP	73	AI/O
LAN1MDIAN	74	AI/O
LAN1MDIBP	75	AI/O
LAN1MDIBN	76	AI/O
AVDDL	77	AP
LAN1MDICP	78	AI/O
LAN1MDICN	79	AI/O
LAN1MDIDP	80	AI/O
LAN1MDIDN	81	AI/O
PLLVDDL	82	AP
PLLGND	83	AG
AVDDH	84	AP
LAN2MDIAP	85	AI/O
LAN2MDIAN	86	AI/O
LAN2MDIBP	87	AI/O
LAN2MDIBN	88	AI/O
GND	EPAD	G

7. Pin Descriptions

7.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LAN1MDIAP/N LAN1MDIBP/N LAN1MDICP/N LAN1MDIDP/N	73 74 75 76 78 79 80 81	AI/O	10	LAN 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
LAN2MDIAP/N LAN2MDIBP/N LAN2MDICP/N LAN2MDIDP/N	85 86 87 88 2 3 4 5	AI/O	10	LAN 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

7.2. High Speed Serial Interface Pins

Table 3. High Speed Serial Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
HSOP/N	16 15	AO	10	High Speed Serial Output Pins: 1.25GHz/3.125GHz Differential serial interface to transmit data. Keep floating when unused.
HSIP/N	18 19	AI	10	High Speed Serial Input Pins: 1.25GHz/3.125GHz Differential serial interface to receive data. Keep floating when unused.

7.3. General Purpose Interfaces

The RTL8364NB supports multi-function General Purpose Interfaces that can be configured as MII/RGMII mode for extension GMAC interfaces. The RTL8364NB supports two extension interfaces (Extension GMAC1 and Extension GMAC2) for connecting with an external PHY, MAC, or CPU in specific applications. These extension interfaces support RGMII, MII MAC mode, or MII PHY mode via register configuration.

Table 4. General Purpose Interfaces Pins

Pin No.	GPIO	RGMII	MII MAC Mode	MII PHY Mode	Other function	Configuration Strapping
13	GPIO57	-	-	-	INTERRUPT	-
23	GPIO01	RG2_TXD3	M2M_TXD3	M2P_RXD3	-	-
24	GPIO02	RG2_TXD2	M2M_TXD2	M2P_RXD2	-	-
25	GPIO03	RG2_TXD1	M2M_TXD1	M2P_RXD1	-	-
26	GPIO04	RG2_TXD0	M2M_TXD0	M2P_RXD0	-	-
27	GPIO05	RG2_TXCTL	M2M_TXEN	M2P_RXDV	-	-
28	GPIO06	RG2_TXCLK	M2M_TXCLK	M2P_RXCLK	-	-
29	GPIO07	RG2_RXCLK	M2M_RXCLK	M2P_TXCLK	-	-
30	GPIO08	RG2_RXCTL	M2M_RXDV	M2P_TXEN	-	-
31	GPIO09	RG2_RXD0	M2M_RXD0	M2P_TXD0	-	-
32	GPIO10	RG2_RXD1	M2M_RXD1	M2P_TXD1	-	-
33	GPIO11	RG2_RXD2	M2M_RXD2	M2P_TXD2	-	-
34	GPIO12	RG2_RXD3	M2M_RXD3	M2P_TXD3	-	-
38	GPIO19	RG1_TXD3	M1M_TXD3	M1P_RXD3	-	-
39	GPIO20	RG1_TXD2	M1M_TXD2	M1P_RXD2	-	-
40	GPIO21	RG1_TXD1	M1M_TXD1	M1P_RXD1	-	-
41	GPIO22	RG1_TXD0	M1M_TXD0	M1P_RXD0	-	-
42	GPIO23	RG1_TXCTL	M1M_TXEN	M1P_RXDV	-	-
43	GPIO24	RG1_TXCLK	M1M_TXCLK	M1P_RXCLK	-	-
44	GPIO28	RG1_RXCLK	M1M_RXCLK	M1P_TXCLK	-	-
45	GPIO29	RG1_RXCTL	M1M_RXDV	M1P_TXEN	-	-
46	GPIO30	RG1_RXD0	M1M_RXD0	M1P_TXD0	-	-
47	GPIO31	RG1_RXD1	M1M_RXD1	M1P_TXD1	-	-
48	GPIO32	RG1_RXD2	M1M_RXD2	M1P_TXD2	-	-
49	GPIO33	RG1_RXD3	M1M_RXD3	M1P_TXD3	-	-
53	GP O38	-	-	-	-	DIS_SPIS
54	GPIO41	-	-	-	LAN2LED1	-
55	GP O42	-	-	-	LAN2LED2	EN_PWRLIGHT
56	GP O43	-	-	-	LAN2LED0	RESERVED
57	GP O44	-	-	-	-	DIS_8051
58	GP O45	-	-	-	-	DISAUTOLOAD
59	GP O47	-	-	-	LAN1LED2	RESERVED
60	GP O48	-	-	-	LAN1LED0	MID29
61	GPIO49	-	-	-	LAN1LED1	-
62	GP O50	-	-	-	-	EN_PHY

Pin No.	GPIO	RGMII	MII MAC Mode	MII PHY Mode	Other function	Configuration Strapping
63	GP O52	-	-	-	-	SMI_SEL
68	GPIO53	-	-	-	SPIS_nCSI	-
69	GPIO54	-	-	-	SPIS_CK/ SCK/ MDC	-
70	GPIO55	-	-	-	SPIS_DI/ SDA/ MDIO	-
71	GPIO56	-	-	-	SPIS_DO	-

7.3.1. RGMII Pins

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB support dual RGMII interfaces to connect with an external MAC or PHY device when register configuration is set to RGMII mode interface.

Table 5. Extension GMAC1 RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG1_TXD3 RG1_TXD2 RG1_TXD1 RG1_TXD0	38 39 40 41	O	-	RG1_TXD[3:0] Extension GMAC1 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG1_TXCLK.
RG1_TXCTL	42	O	-	RG1_TXCTL Extension GMAC1 RGMII Transmit Control signal Output. The RG1_TXCTL indicates TX_EN at the rising edge of RG1_TXCLK, and TX_ER at the falling edge of RG1_TXCLK. At the RG1_TXCLK falling edge, RG1_TXCTL= TX_EN (XOR) TX_ER.
RG1_TXCLK	43	O	-	RG1_TXCLK Extension GMAC1 RGMII Transmit Clock Output. RG1_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_TXD[3:0] and RG1_TXCTL synchronization at RG1_TXCLK on both rising and falling edges.
RG1_RXCLK	44	I	-	RG1_RXCLK Extension GMAC1 RGMII Receive Clock Input. RG1_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_RXD[3:0] and RG1_RXCTL synchronization at both RG1_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXCTL	45	I	-	RG1_RXCTL Extension GMAC1 RGMII Receive Control signal input. The RG1_RXCTL indicates RX_DV at the rising of RG1_RXCLK and RX_ER at the falling edge of RG1_RXCLK. At RG1_RXCLK falling edge, RG1_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXD0 RG1_RXD1 RG1_RXD2 RG1_RXD3	46 47 48 49	I	-	RG1_RXD[3:0] Extension GMAC1 RGMII Receive Data Input. Received data is received synchronously by RG1_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

Table 6. Extension GMAC2 RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG2_TXD3 RG2_TXD2 RG2_TXD1 RG2_TXD0	23 24 25 26	O	-	RG2_TXD[3:0] Extension GMAC2 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG2_TXCLK.
RG2_TXCTL	27	O	-	RG2_TXCTL Extension GMAC2 RGMII Transmit Control signal Output. The RG2_TXCTL indicates TX_EN at the rising edge of RG2_TXCLK, and TX_ER at the falling edge of RG2_TXCLK. At the RG2_TXCLK falling edge, RG2_TXCTL= TX_EN (XOR) TX_ER.
RG2_TXCLK	28	O	-	RG2_TXCLK Extension GMAC2 RGMII Transmit Clock Output. RG2_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG2_TXD[3:0] and RG2_TXCTL synchronization at RG2_TXCLK on both rising and falling edges.
RG2_RXCLK	29	I	-	RG2_RXCLK Extension GMAC2 RGMII Receive Clock Input. RG2_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG2_RXD[3:0] and RG2_RXCTL synchronization at both RG2_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG2_RXCTL	30	I	-	RG2_RXCTL Extension GMAC2 RGMII Receive Control signal input. The RG2_RXCTL indicates RX_DV at the rising of RG2_RXCLK and RX_ER at the falling edge of RG2_RXCLK. At RG2_RXCLK falling edge, RG2_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG2_RXD0 RG2_RXD1 RG2_RXD2 RG2_RXD3	31 32 33 34	I	-	RG2_RXD[3:0] Extension GMAC2 RGMII Receive Data Input. Received data is received synchronously by RG2_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

7.3.2. MII Pins

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB support dual MII interfaces to connect with an external MAC or PHY device when register configuration is set to MII mode interface. These two MII interfaces can be configured as MII MAC mode or MII PHY mode by register.

Table 7. Extension GMAC1 MII Pins (MII MAC Mode or MII PHY Mode)

Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_TXD3/ M1P_RXD3 M1M_TXD2/ M1P_RXD2 M1M_TXD1/ M1P_RXD1 M1M_TXD0/ M1P_RXD0	38 39 40 41	O	-	M1M_TXD[3:0] Extension GMAC1 MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXD[3:0] Extension GMAC1 MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M1P_RXCLK.
M1M_TXEN/ M1P_RXDV	42	O	-	M1M_TXEN Extension GMAC1 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXDV Extension GMAC1 MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M1P_RXCLK.
M1M_TXCLK/ M1P_RXCLK	43	I/O	-	M1M_TXCLK Extension GMAC1 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M1M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_TXCLK is 2.5MHz Clock Input. Used to synchronize M1M_TXD[3:0] and M1M_TXEN. M1P_RXCLK Extension GMAC1 MII PHY Mode Receive Clock Output. In MII 100Mbps, M1P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_RXCLK is 2.5MHz Clock Output. Used to synchronize M1P_RXD[3:0] and M1P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXCLK/ M1P_TXCLK	44	I/O	-	M1M_RXCLK Extension GMAC1 MII MAC Mode Receive Clock Input. In MII 100Mbps, M1M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_RXCLK is 2.5MHz Clock Input. Used to synchronize M1M_RXD[3:0], M1M_RXDV, and M1P_CRS. M1P_TXCLK Extension GMAC1 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M1P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_TXCLK is 2.5MHz Clock Output. Used to synchronize M1P_TXD[3:0] and M1P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_RXDV/ M1P_TXEN	45	I	-	M1M_RXDV Extension GMAC1 MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M1M_RXCLK. M1P_TXEN Extension GMAC1 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M1P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXD0/ M1P_TXD0 M1M_RXD1/ M1P_TXD1 M1M_RXD2/ M1P_TXD2 M1M_RXD3/ M1P_TXD3	46 47 48 49	I	-	M1M_RXD[3:0] Extension GMAC1 MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M1M_RXCLK. M1P_TXD[3:0] Extension GMAC1 MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M1P_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

Table 8. Extension GMAC2 MII Pins (MII MAC Mode or MII PHY Mode)

Pin Name	Pin No.	Type	Drive (mA)	Description
M2M_TXD3/ M2P_RXD3 M2M_TXD2/ M2P_RXD2 M2M_TXD1/ M2P_RXD1 M2M_TXD0/ M2P_RXD0	23 24 25 26	O	-	M2M_TXD[3:0] Extension GMAC2 MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M2M_TXCLK. M2P_RXD[3:0] Extension GMAC2 MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M2P_RXCLK.
M2M_TXEN/ M2P_RXDV	27	O	-	M2M_TXEN Extension GMAC2 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M2M_TXCLK. M2P_RXDV Extension GMAC2 MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M2P_RXCLK.

Pin Name	Pin No.	Type	Drive (mA)	Description
M2M_TXCLK/ M2P_RXCLK	28	I/O	-	M2M_TXCLK Extension GMAC2 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M2M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M2M_TXCLK is 2.5MHz Clock Input. Used to synchronize M2M_TXD[3:0] and M2M_TXEN. M2P_RXCLK Extension GMAC2 MII PHY Mode Receive Clock Output. In MII 100Mbps, M2P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M2P_RXCLK is 2.5MHz Clock Output. Used to synchronize M2P_RXD[3:0] and M2P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.
M2M_RXCLK/ M2P_TXCLK	29	I/O	-	M2M_RXCLK Extension GMAC2 MII MAC Mode Receive Clock Input. In MII 100Mbps, M2M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M2M_RXCLK is 2.5MHz Clock Input. Used to synchronize M2M_RXD[3:0], M2M_RXDV, and M2M_CRS. M2P_TXCLK Extension GMAC2 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M2P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M2P_TXCLK is 2.5MHz Clock Output. Used to synchronize M2P_TXD[3:0] and M2P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.
M2M_RXDV/ M2P_TXEN	30	I	-	M2M_RXDV Extension GMAC2 MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M2M_RXCLK. M2P_TXEN Extension GMAC2 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M2P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M2M_RXD0/ M2P_TXD0 M2M_RXD1/ M2P_TXD1 M2M_RXD2/ M2P_TXD2 M2M_RXD3/ M2P_TXD3	31 32 33 34	I	-	M2M_RXD[3:0] Extension GMAC2 MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M2M_RXCLK. M2P_TXD[3:0] Extension GMAC2 MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M2P_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

7.4. LED Pins

The RTL8364NB LED pins can be configured to parallel mode LED or serial mode LED interface via Register configuration. LED0, LED1, and LED2 of Port n indicate information that can be defined via register or EEPROM.

In parallel mode LED interface, when the LED pin is pulled low, the LED output polarity will be high active. When the LED pin is pulled high, the LED output polarity will change from high active to low active. See section 9.19 LED Indicators, page 39 for more details.

Table 9. LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LAN2LED2/ EN_PWRLIGHT	55	I/O_{PU}	-	Port 3 LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 39 for more details.
LAN2LED1	54	I/O_{PU}	-	Port 3 LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 39 for more details.
LAN2LED0/ RESERVED	56	I/O_{PU}	-	Port 3 LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 39 for more details.
LAN1LED2/ RESERVED	59	I/O_{PU}	-	Port 1 LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 39 for more details.
LAN1LED1	61	I/O_{PU}	-	Port 1 LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 39 for more details.
LAN1LED0/ MID29	60	I/O_{PU}	-	Port 1 LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM. See section 9.19 LED Indicators, page 39 for more details.

7.5. Configuration Strapping Pins

Table 10. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
DIS_SPIS	53	I/O_{PU}	SPI Slave Management Interface Selection. Pull Up: Disable SPI Slave Management Interface Pull Down: Enable SPI Slave Management Interface *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*

Pin Name	Pin No.	Type	Description
EN_PWRLIGHT/ LAN2LED2	55	I/O_{PU}	Enable Power on Light. Pull Up: Enable Power on Light *Pull Down: Disable Power on Light* *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 9.19 LED Indicators, page 39 for more details.*
RESERVED/ LAN2LED0	56	I/O_{PU}	Internal Use/Reserved. *Note: For normal operation, this pin must be pulled low via an external 4.7k ohm resistor upon power on or reset.* *When pulled low, the LED output polarity will be high active. See section 9.19 LED Indicators, page 39 for more details.*
DIS_8051/ LAN2LED2	57	I/O_{PU}	Disable Embedded 8051. Pull Up: Disable embedded 8051 Pull Down: Enable embedded 8051 *Note 1: The strapping pin DISAUTOLOAD and DIS_8051 are for power on or reset initial stage configuration. Refer to Table 11 Configuration Strapping Pins (DISAUTOLOAD and DIS_8051), page 20 for details.* *Note 2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 9.19 LED Indicator, page 39 for more details.*
DISAUTOLOAD	58	I/O_{PU}	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload Pull Down: Enable EEPROM autoload *Note 1: The strapping pin DISAUTOLOAD and DIS_8051 are for power on or reset initial stage configuration. Refer to Table 11 Configuration Strapping Pins (DISAUTOLOAD and DIS_8051), page 20 for details.* *Note 2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
RESERVED/ LAN1LED2	59	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 9.19 LED Indicators, page 39 for more details.*
MID29/ LAN1LED0	60	I/O_{PU}	Select MID29. Pull Up: MII Management Interface PHY ID is 29 Pull Down: MII Management Interface PHY ID is 0 *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 9.19 LED Indicators, page 39 for more details.*
EN_PHY	62	I/O_{PU}	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*

Pin Name	Pin No.	Type	Description
SMI_SEL	63	I/O_{PU}	EEPROM SMI/MII Management Interface Selection. Pull Up: EEPROM SMI interface when DIS_SPIS = 1 Pull Down: MII Management interface when DIS_SPIS = 1 *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*

7.5.1. Configuration Strapping Pins (DISAUTOLOAD and DIS_8051)

Table 11. Configuration Strapping Pins (DISAUTOLOAD and DIS_8051)

DISAUTOLOAD	DIS_8051	Initial Stage (Power On or Reset) Loading Data	
		From	To
0	0	EEPROM	Embedded 8051 Instruction Memory
	1	EEPROM	Register
1	Irrelevant	Do Nothing	Do Nothing

7.6. Management Interface Pins

Table 12. Management Interface Pins

Pin Name	Pin No.	Type	Description
SPIS_nCSI	68	I_{PU}	When DIS_SPIS is Pulled Low, SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Chip Selection Input pin. When DIS_SPIS is Pulled Up, SPI Slave Management Interface is Disabled. This pin is unused.
SPIS_CK/ SCK/ MDC	69	I/O	When DIS_SPIS is Pulled Low, SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Serial Clock Input pin. When DIS_SPIS is Pulled Up, SPI Slave Management Interface is Disabled. This pin acts as EEPROM SMI Interface Clock/MII Management Interface (MMD) Clock (selected via the hardware strapping pin, SMI_SEL).
SPIS_DI/ SDA/ MDIO	70	I/O	When DIS_SPIS is Pulled Low, SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Serial Data Input pin. When DIS_SPIS is Pulled Up, SPI Slave Management Interface is Disabled. This pin acts as EEPROM SMI Interface Data/MII Management Interface (MMD) Data (selected via the hardware strapping pin, SMI_SEL).
SPIS_DO	71	O	When DIS_SPIS is Pulled Low, SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Serial Data Output pin. When DIS_SPIS is Pulled Up, SPI Slave Management Interface is Disabled. This pin is unused.
INTERRUPT	13	O_{PD}	Interrupt output when Interrupt even occurs. Active High by pull-down to GND via a 1K resister. Active Low by pull-up to DVDDIO via a 4.7K resister.

7.7. Miscellaneous Pins

Table 13. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
XTALO	65	AO	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output.
XTALI	66	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz +/-50ppm tolerance crystal reference or oscillator input. When using a crystal, connect a loading capacitor from each pad to ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating. The maximum XTALI input voltage is 3.3V.
MDIREF	8	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
RESERVED	21	AO	Reserved. Must be left floating in normal operation.
nRESET	67	I_{PU}	System Reset Input Pin. When low active will reset the RTL8364NB. This pin must be kept floating, or connected to DVDDIO with a 1K~4.7K ohm resistor.
GPIO01/ E2_DO3	23	I/O	General Purpose Input/Output Interface IO01.
GPIO02/ E2_DO2	24	I/O	General Purpose Input/Output Interface IO02.
GPIO03/ E2_DO1	25	I/O	General Purpose Input/Output Interface IO03.
GPIO04/ E2_DO0	26	I/O	General Purpose Input/Output Interface IO04.
GPIO05/ E2_DOEN	27	I/O	General Purpose Input/Output Interface IO05.
GPIO06/ E2_DOCLK	28	I/O	General Purpose Input/Output Interface IO06.
GPIO07/ E2_DICLK	29	I/O	General Purpose Input/Output Interface IO07.
GPIO08/ E2_DIDV	30	I/O	General Purpose Input/Output Interface IO08.
GPIO09/ E2_DI0	31	I/O	General Purpose Input/Output Interface IO09.
GPIO10/ E2_DI1	32	I/O	General Purpose Input/Output Interface IO10.
GPIO11/ E2_DI2	33	I/O	General Purpose Input/Output Interface IO11.
GPIO12/ E2_DI3	34	I/O	General Purpose Input/Output Interface IO12.
GPIO19/ E1_DO3	38	I/O	General Purpose Input/Output Interface IO19.
GPIO20/ E1_DO2	39	I/O	General Purpose Input/Output Interface IO20.

Pin Name	Pin No.	Type	Description
GPIO21/ E1_DO1	40	I/O	General Purpose Input/Output Interface IO21.
GPIO22/ E1_DO0	41	I/O	General Purpose Input/Output Interface IO22.
GPIO23/ E1_DOEN	42	I/O	General Purpose Input/Output Interface IO23.
GPIO24/ E1_DOCLK	43	I/O	General Purpose Input/Output Interface IO24.
GPIO28/ E1_DICLK	44	I/O	General Purpose Input/Output Interface IO28.
GPIO29/ E1_DIDV	45	I/O	General Purpose Input/Output Interface IO29.
GPIO30/ E1_DI0	46	I/O	General Purpose Input/Output Interface IO30.
GPIO31/ E1_DI1	47	I/O	General Purpose Input/Output Interface IO31.
GPIO32/ E1_DI2	48	I/O	General Purpose Input/Output Interface IO32.
GPIO33/ E1_DI3	49	I/O	General Purpose Input/Output Interface IO33.
GP O38/ DIS_SPIS	53	I/O_{PU}	General Purpose Output Interface O38.
GPIO41/ LAN2LED1	54	I/O_{PU}	General Purpose Input/Output Interface IO41.
GP O42/ LAN2LED2/ EM_PWRLIGHT	55	I/O_{PU}	General Purpose Output Interface O42.
GP O43/ LAN2LED0/ RESERVED	56	I/O_{PU}	General Purpose Output Interface O43.
GP O44/ DIS_8051	57	I/O_{PU}	General Purpose Output Interface O44.
GP O45/ DISAUTOLOAD	58	I/O_{PU}	General Purpose Output Interface O45.
GP O47/ LAN1LED2/ RESERVED	59	I/O_{PU}	General Purpose Output Interface O47.
GP O48/ LAN1LED0/ MID29	60	I/O_{PU}	General Purpose Output Interface O48.
GPIO49/ LAN1LED1	61	I/O_{PU}	General Purpose Input/Output Interface IO49.
GP O50/ EN_PHY	62	I/O_{PU}	General Purpose Output Interface O50.
GP O52/ SMI_SEL	63	I/O_{PU}	General Purpose Output Interface O52.

Pin Name	Pin No.	Type	Description
GPIO53/ SPIS_nCSI	68	I/O_{PU}	General Purpose Input/Output Interface IO53.
GPIO54/ SPIS_CK/ SCK/ MDC	69	I/O	General Purpose Input/Output Interface IO54.
GPIO55/ SPIS_DI/ SDA/ MDIO	70	I/O	General Purpose Input/Output Interface IO55.
GPIO56/ SPIS_DO	71	I/O	General Purpose Input/Output Interface IO56.
GPIO57/ INTERRUPT	13	I/O_{PD}	General Purpose Input/Output Interface IO57.

7.8. Test Pins

Table 14. Test Pins

Pin Name	Pin No.	Type	Description
RTT1	10	AO	Reserved for Internal Use. Must be left floating.

7.9. Power and GND Pins

Table 15. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO	12, 51	P	Digital I/O High Voltage Power for LED, Management Interface, nRESET, and INTERRUPT.
DVDDIO_1	37, 50	P	Digital I/O High Voltage Power for Extension Port 1 General Purpose Interface.
DVDDIO_2	22, 36	P	Digital I/O High Voltage Power for Extension Port 2 General Purpose Interface.
DVDDL	14, 35, 52	P	Digital Low Voltage Power.
AVDDH	6, 11, 20, 64, 72, 84	AP	Analog High Voltage Power.
AVDDL	1, 9, 77	AP	Analog Low Voltage Power.
SVDDL	17	AP	SerDes Analog Low Voltage Power.
PLLVDDL	82	AP	PLL Low Voltage Power.
GND	EPAD	G	GND.
AGND	7	AG	Analog GND.
PLLGND	83	AG	PLL GND.

8. Physical Layer Functional Overview

8.1. MDI Interface

The RTL8364NB embeds five 10/100/1000M Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

8.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

8.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

8.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

8.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

8.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

8.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

8.8. Auto-Negotiation for UTP

The RTL8364NB obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8364NB advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

8.9. Crossover Detection and Auto Correction

The RTL8364NB automatically determines whether or not it needs to crossover between pairs (see Table 16) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8364NB automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 16. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

8.10. Polarity Correction

The RTL8364NB automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

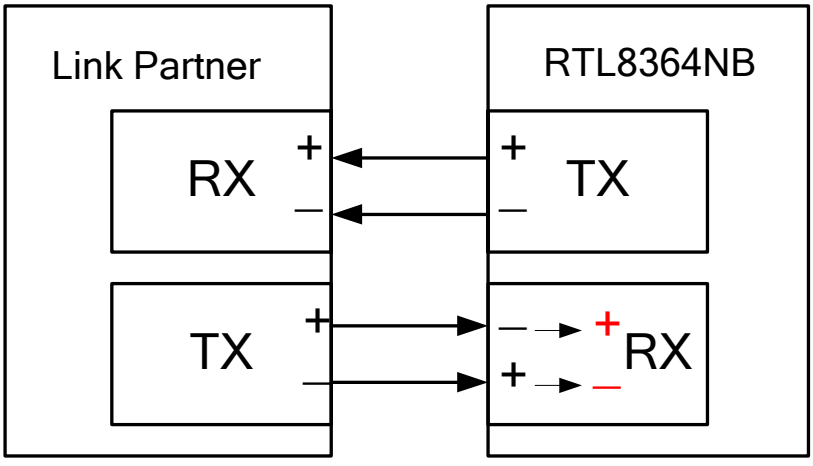


Figure 4. Conceptual Example of Polarity Correction

9. General Function Description

9.1. Reset

9.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8364NB will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Autoload the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

9.1.2. Software Reset

The RTL8364NB supports two software resets; a chip reset and a soft reset.

9.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

9.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list
2. Restart the auto-negotiation process

9.2. IEEE 802.3x Full Duplex Flow Control

The RTL8364NB supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

9.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "Truncated Binary Exponential Backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL8364NB is 9.

The half duplex back-off algorithm in the RTL8364NB does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

9.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8364NB sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL8364NB supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

9.4. Search and Learning

Search

When a packet is received, the RTL8364NB uses the destination MAC address, Filtering Identifier (FID) and Enhanced Filtering Identifier (EFID) to search the 2K-entry look-up table. The 48-bit MAC address, 4-bit FID and 3-bit EFID use a hash algorithm, to calculate an 11-bit index value. The RTL8364NB uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8364NB uses the source MAC address, FID, and EFID of the incoming packet to hash into a 9-bit index. It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8364NB will update the entry with new information. If there is no match and the 2K entries are not all occupied by other MAC addresses, the RTL8364NB will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8364NB is between 200 and 400 seconds (typical is 300 seconds).

9.5. SVL and IVL/SVL

The RTL8364NB supports a 16-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

9.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8364NB. The maximum packet length may be set from 1518 bytes to 16K bytes.

9.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8364NB supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 17 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 17. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
Provider Bridge Group Address	01-80-C2-00-00-08
Undefined 802.1 Address	01-80-C2-00-00-04 ~ 01-80-C2-00-00-07 & 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C & 01-80-C2-00-00-0F
Provider Bridge MVRP Address	01-80-C2-00-00-0D
IEEE Std 802.1AB Link Layer Discovery Protocol Address	01-80-C2-00-00-0E
All LANs Bridge Management Group Address	01-80-C2-00-00-10
Load Server Generic Address	01-80-C2-00-00-11
Loadable Device Generic Address	01-80-C2-00-00-12
Undefined 802.1 Address	01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F
Generic Address for All Manager Stations	01-80-C2-00-00-18
Generic Address for All Agent Stations	01-80-C2-00-00-1a
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F
CDP(Cisco Discovery Protocol)	01-00-0C-CC-CC-CC
CSSTP(Cisco Shared Spanning Tree Protocol)	01-00-0C-CC-CC-CD
LLDP	(01:80:c2:00:00:0e or 01:80:c2:00:00:03 or 01:80:c2:00:00:00) && ethertype = 0x88CC

9.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8364NB enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate (number of Kbps per second or number of packets per second), all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

9.9. Port Security Function

The RTL8364NB supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

9.10. MIB Counters

The RTL8364NB supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

9.11. Port Mirroring

The RTL8364NB supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets from multiple mirrored port can be mirrored to one monitor port.

9.12. VLAN Function

The RTL8364NB supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to 'Admit All', 'Admit only Untagged' or 'Admit only Tagged'
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8364NB will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8364NB also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8364NB supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8364NB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

9.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached serial EEPROM or EEPROM SMI Slave interface. The 4K-entry VLAN Table designed into the RTL8364NB provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

9.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8364NB supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8364NB uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8364NB compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When ‘802.1Q tag aware VLAN’ is enabled, the RTL8364NB performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If ‘802.1Q tag aware VLAN’ is disabled, the RTL8364NB performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when ‘802.1Q tag aware VLAN’ is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL8364NB. One is the ‘VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is ‘VLAN member set ingress filtering’, which will drop frames if the ingress port is not in the member set.

9.12.3. Protocol-Based VLAN

The RTL8364NB supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 5. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be ‘Ethernet’, and value to be ‘0x0800’. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

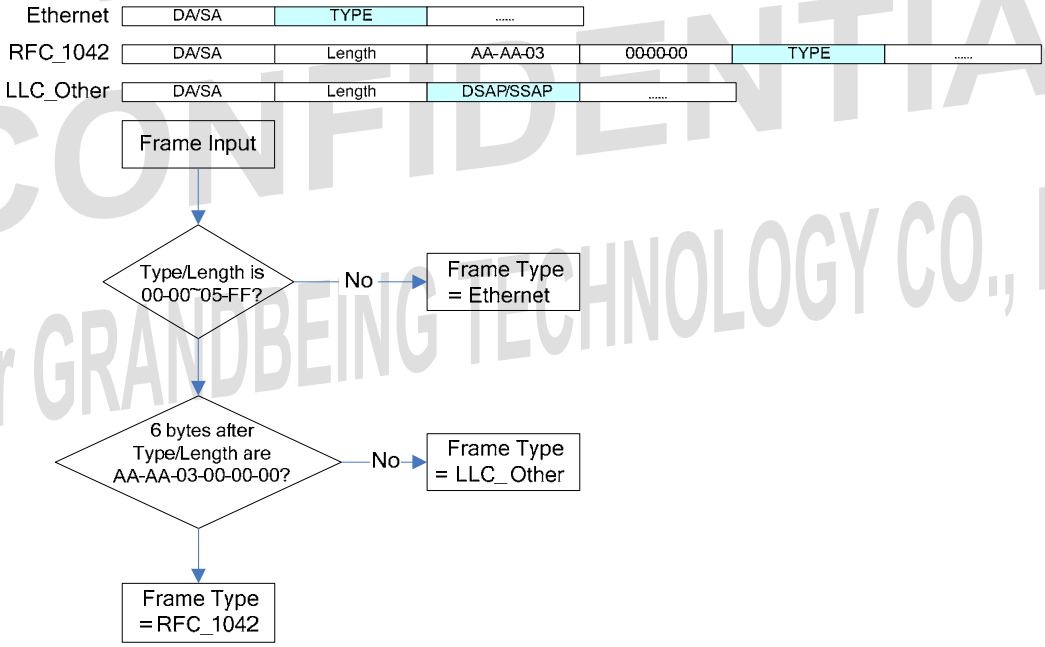


Figure 5. Protocol-Based VLAN Frame Format and Flow Chart

9.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8364NB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL8364NB will drop non-tagged packets and packets with an incorrect PVID.

9.13. QoS Function

The RTL8364NB supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8364NB, the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

9.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

9.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8364NB can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8364NB identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority
- VLAN-based priority
- MAC-based priority
- SVLAN-based priority

9.13.3. Priority Queue Scheduling

The RTL8364NB supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- Average Packet Rate (APR) leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 6 shows the RTL8364NB packet-scheduling diagram.

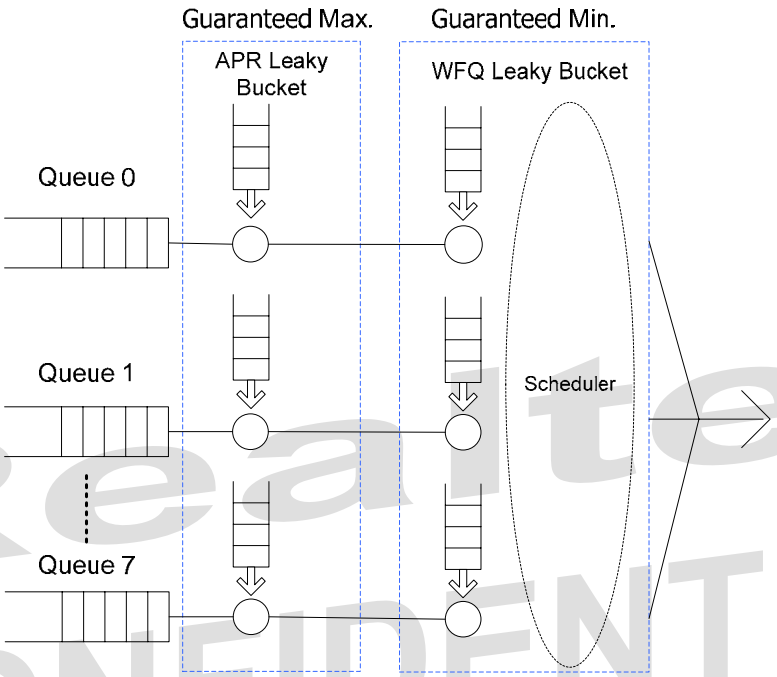


Figure 6. RTL8364NB MAX-MIN Scheduling Diagram

9.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8364NB supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. 802.1p/Q priority & IP DSCP value can be remarked based on internal priority or original 802.1p/Q priority & IP DSCP value in packets.

9.13.5. ACL-Based Priority

The RTL8364NB supports 96-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule)
- If the action bit is 'Permit', ACL rules will override other rules
- If the action bit is 'Mirror', the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism
- The priority bit will take effect only if the action bit is 'CPU', 'Permit', and 'Mirror'. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism

9.14. IGMP & MLD Snooping Function

The RTL8364NB supports hardware IGMPv1/v2/v3 and MLDv1/v2 snooping with a maximum of 256 groups (maximum 255 groups per port). These multicast groups are learned and deleted/aged out automatically. For data packets of a known multicast group, the RTL8364NB forwards them according to the learned group membership.

The RTL8364NB checks group membership every 125 seconds (default). If a specified port of the RTL8364NB does not receive a report message after 3 (default) consecutive checks, the port is removed from the multicast group. The 125 second interval and the number of consecutive checks before ageing are user configurable default values.

IPv4 multicast data packets are forwarded per group IP. IPv6 multicast data packets are forwarded per destination MAC. That is, IPv6 multicast groups that share the same destination MAC are treated as the same group. This is called address ambiguity.

Some reserved range IP addresses will always be flooded to all ports. If IGMP or MLD report message requests to join these groups, this request will be ignored silently. These reserved IP addresses could be the following IP addresses and they are configurable.

IPv4: 224.0.0.0 ~ 224.0.0.255

IPv4: 224.0.1.0 ~ 224.0.1.255

IPv4: 239.255.255.0 ~ 239.255.255.255

IPv6: 33:33:00:00:00:00 ~ 33:33:00:00:00:FF (forwarded per destination MAC)

Due to address ambiguity, some IPv6 multicast addresses that are not reserved for network protocols will be flooded, as the corresponding destination MAC address is inside the reserved IP address range (Corresponding MAC address).

The RTL8364NB learns the ‘Dynamic Router Port’ automatically by monitoring Query messages (both IGMP & MLD) and multicast routing protocol packets. Table 18 gives the multicast routing protocols that the RTL8364NB recognizes. PIMv1 is confirmed by the IGMP header type and the other multicast routing protocols are recognized by the destination IP in the IP header (in both IPv4 and IPv6).

Table 18. IPv4/IPv6 Multicast Routing Protocols

IPv4	IPv6	Multicast Routing Protocol
N/A	N/A	Check IGMP Header Type=0x14 (PIMv1)
224.0.0.13	FF02::D	PIMv2
224.0.0.4	FF02::4	DVMRP
224.0.0.5	FF02::5	MOSPF
224.0.0.6	FF02::6	MOSPF

Users can specify ‘Static Router Ports’ via API. This forces the ports to act as true router ports. All reports and Leave/Done messages will be forwarded to the specified Static Router ports.

The RTL8364NB supports a ‘Fast Leave’ feature. When enabled, group membership will be removed immediately the RTL8364NB receives an IGMPv2 Leave message or MLDv1 Done message. Normally this feature is only enabled when there is only one host.

The IGMP/MLD snooping feature is disabled by default. IGMP & MLD messages will be flooded to all ports without any further processing. This feature can be enabled and configured via API. Contact your Realtek support team for configuration details.

9.15. IEEE 802.1x Function

The RTL8364NB supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior
- Guest VLAN

9.15.1. Port-Based Access Control

Each port of the RTL8364NB can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

9.15.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

9.15.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

9.15.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

9.15.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction should be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

9.15.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

9.15.7. Guest VLAN

When the RTL8364NB enables the Port-based or MAC-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, the RTL8364NB will drop all packets from this port.

The RTL8364NB also supports one Guest VLAN to allow unauthorized ports or packets to be forwarded to a limited VLAN domain. The user can configure one VLAN ID and member set for these unauthorized packets.

9.16. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8364NB supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL8364NB also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

9.17. Embedded 8051

An 8051 MCU is embedded in the RTL8364NB to support management functions. The 8051 MCU can access all of the registers in the RTL8364NB through the internal bus. With the Network Interface Circuit (NIC) acting as the data path, the 8051 MCU connects to the switch core and can transmit frames to or receive frames from the Ethernet network. Features of the 8051 MCU include:

- 256 Bytes fast internal RAM
- On-chip 48K data memory
- On-chip 16K code memory
- Supports code-banking
- 12KBytes NIC buffer
- EEPROM read/write ability

9.18. Realtek Cable Test (RTCT)

The RTL8364NB physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open, or impedance mismatch in each differential pair. The RTL8364NB also provides LED support to indicate test status and results.

9.19. LED Indicators

The RTL8364NB supports parallel LEDs for each port. Each port has three LED indicator pins, LED0, LED1, and LED2. Each pin may have different indicator information (defined in Table 19). Refer to section 7.4 LED Pins, page 18 for pin details. Upon reset, the RTL8364NB supports chip diagnostics and LED operation test by blinking all LEDs once.

Table 19. LED Definitions

LED Statuses	Description
LED_Off	LED Pin Output Disable.
Dup/Col	Duplex/Collision Indicator. Blinking when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinking when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100 (10)/Act	10/100Mbps Speed/Activity Indicator. Low for 10/100Mbps. Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.

The LED pin also supports pin strapping configuration functions. The LANnLED0, LANnLED1, and LANnLED2 pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low

after reset. When the pin input is pulled down upon reset, the pin output is active high after reset. For details refer to Figure 7 and Figure 8. Typical values for pull-up/pull-down resistors are 4.7KΩ.

The LANnLED1 can be combined with LANnLED1 or LANnLED2 as a Bi-color LED.

LED_ PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

- LAN0LED1 should be pulled up upon reset if LAN0LED1 is combined with LAN0LED2 as a Bi-color LED, and LAN0LED2 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- LAN0LED1 should be pulled down upon reset if LAN0LED1 is combined with LAN0LED2 as a Bi-color LED, and LAN0LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

Upon reset, the RTL8364NB supports chip diagnostics and LED functions by blinking all LEDs once. This function can be disabled by asserting EN_PWRLIGHT to 0b0 (pull down).

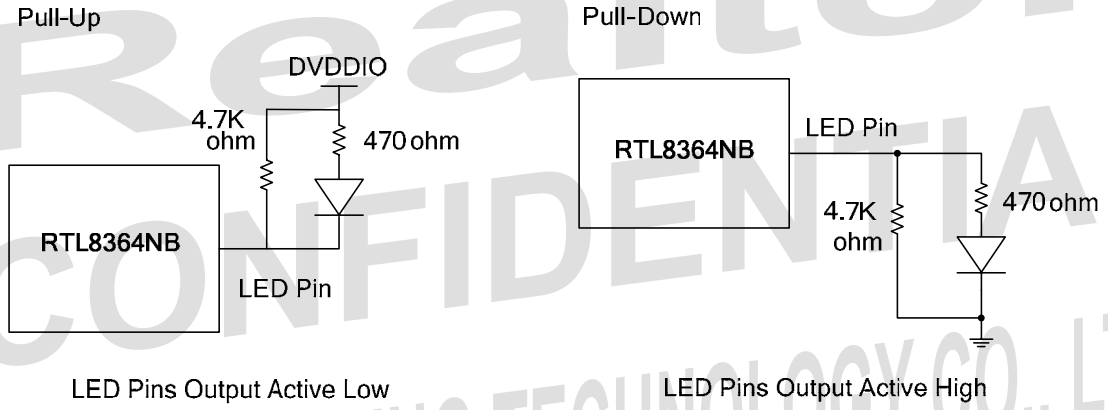


Figure 7. Pull-Up and Pull-Down of LED Pins for Single-Color LED

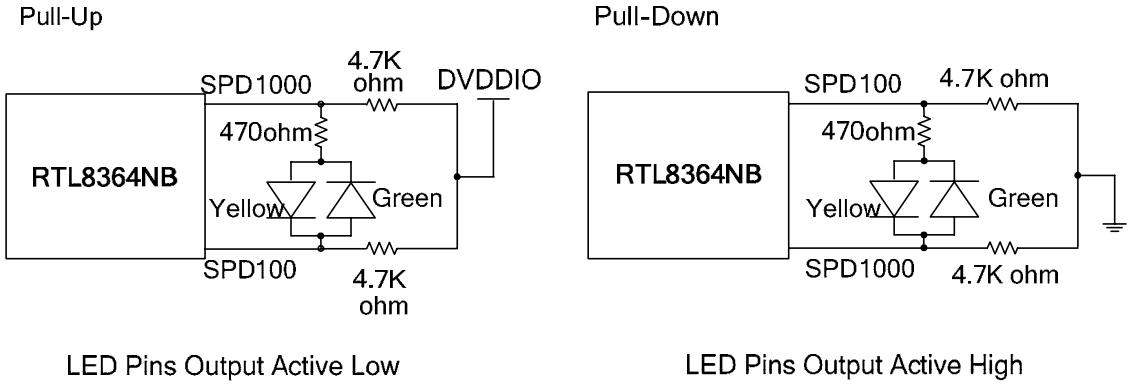


Figure 8. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

9.20. Green Ethernet

9.20.1. Link-On and Cable Length Power Saving

The RTL8364NB provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

9.20.2. Link-Down Power Saving

The RTL8364NB implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

9.21. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL8364NB supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T and 100Base-TX in full duplex operation.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) sub-layer with 100Base-TX and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

The RTL8364NB MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

9.22. Interrupt Pin for External CPU

The RTL8364NB provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with mask.

When port link-up or link-down interrupt mask is enabled, the RTL8364NB will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

10. Interface Descriptions

10.1. EEPROM SMI Host to EEPROM

The EEPROM interface of the RTL8364NB uses the serial bus EEPROM Serial Management Interface (SMI) to read the EEPROM space up to 256K-bits. When the RTL8364NB is powered up, it drives SCK and SDA to read the registers from the EEPROM.

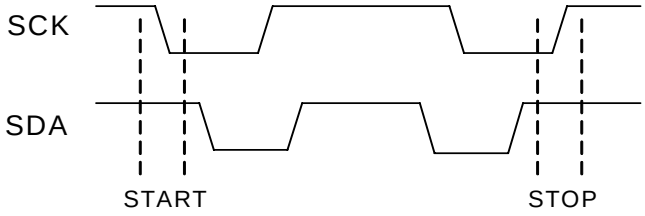


Figure 9. SMI Start and Stop Command

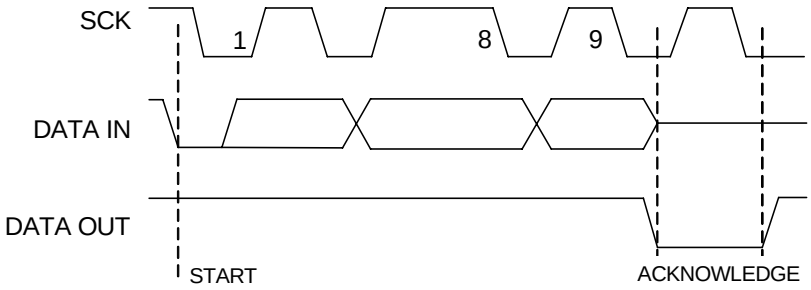


Figure 10. EEPROM SMI Host to EEPROM

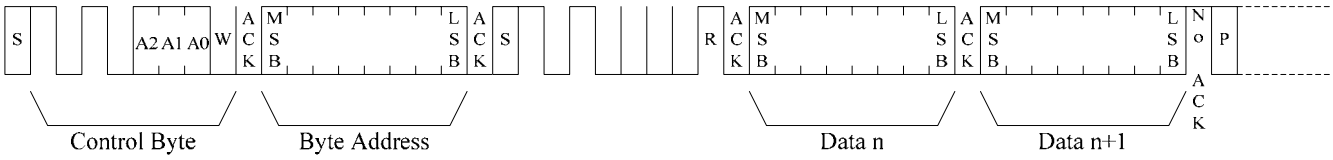


Figure 11. EEPROM SMI Host Mode Frame

10.2. EEPROM SMI Slave for External CPU

When EEPROM auto-load is complete, the RTL8364NB registers can be accessed via SCK and SDA by an external CPU. The device address of the RTL8364NB is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

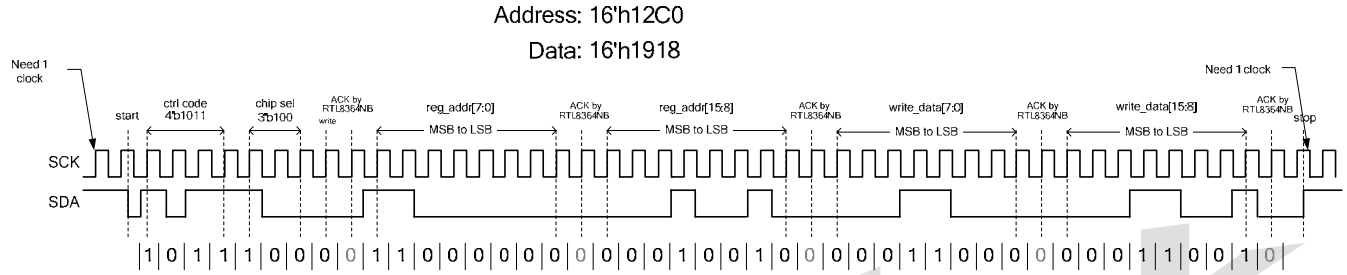


Figure 12. EEPROM SMI Write Command for Slave Mode

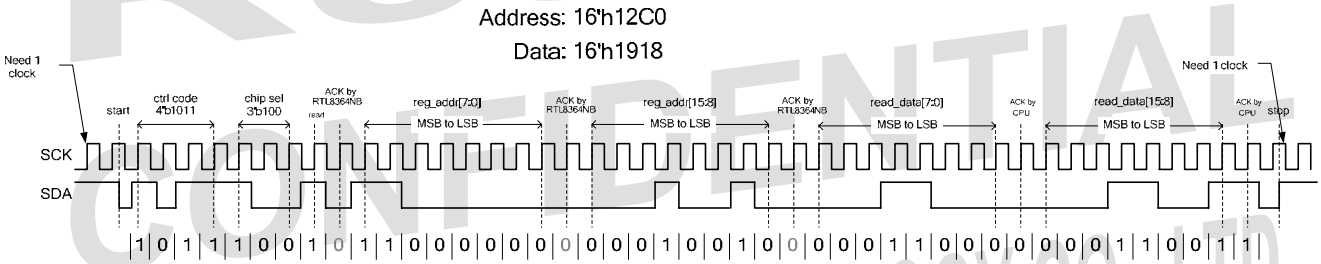


Figure 13. EEPROM SMI Read Command for Slave Mode

10.3. SPI Slave for External CPU

The RTL8364NB supports an SPI-Slave Management Interface that can be enabled via Pin configuration (see Table 10, page 18). An External CPU can configure or manage the RTL8364NB internal register through the SPI interface.

When the CPU writes data to the RTL8364NB internal register via the SPI interface, the first 8-bits is OP code, and the write command OP code is 8h'02. The second 8-bits define the address [15:8], the third 8-bits are the Address [7:0], the fourth 8-bits are write data [15:8], and the fifth 8-bits are write data [7:0] (see Figure 14).

When the CPU reads data from the RTL8364NB internal register via the SPI interface, the first 8-bits OP code is 8h'03. The second 8-bits define the address [15:8] and the third 8-bits are the Address [7:0]. The RTL8364NB returns read data [15:8] at the fourth 8-bits, and data [7:0] at the fifth 8-bits (see Figure 15).

10.3.1. SPI-Slave Interface Access Format

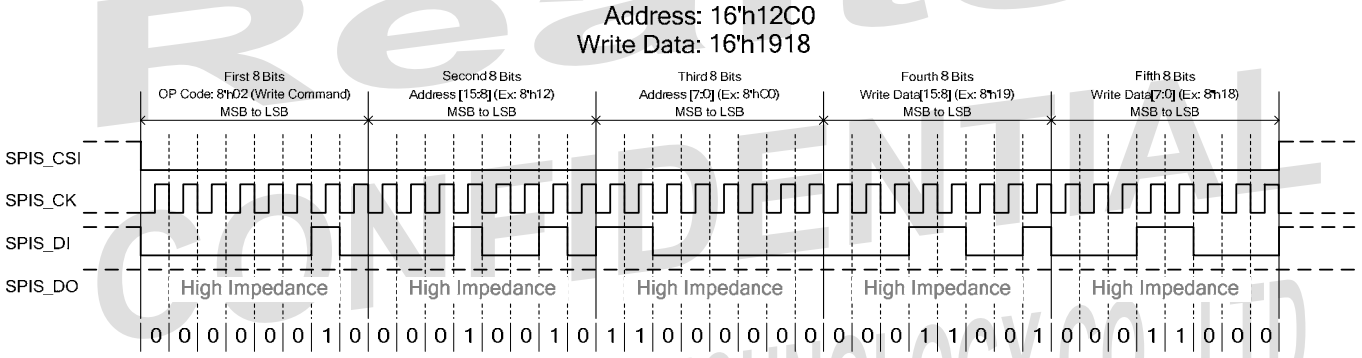


Figure 14. SPI-Slave Write Command Access Format

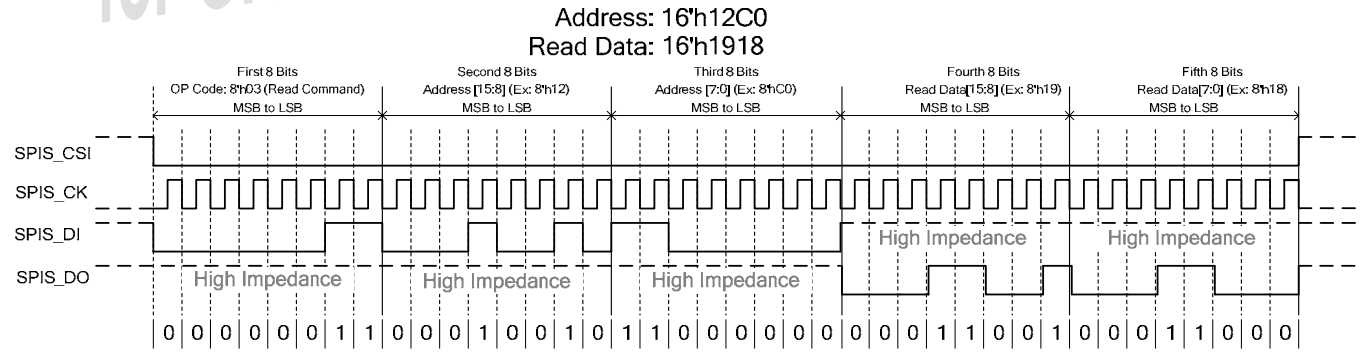


Figure 15. SPI-Slave Read Command Access Format

10.4. General Purpose Interface

The RTL8364NB supports two extension interfaces. The interface function mux is summarized in Table 20 and Table 21. The Extension GMAC1 and Extension GMAC2 of the RTL8364NB support RGMII, MII MAC mode, or MII PHY mode via register configuration.

Table 20. RTL8364NB Extension Port 1 Pin Definitions

Pin No.	Extension Interface	Type	RGMII	MII MAC Mode	MII PHY Mode
38	E1_DO3	O	RG1_TXD3	M1M_TXD3	M1P_RXD3
39	E1_DO2	O	RG1_TXD2	M1M_TXD2	M1P_RXD2
40	E1_DO1	O	RG1_TXD1	M1M_TXD1	M1P_RXD1
41	E1_DO0	O	RG1_TXD0	M1M_TXD0	M1P_RXD0
42	E1_DOEN	O	RG1_TXCTL	M1M_TXEN	M1P_RXDV
43	E1_DOCLK	O	RG1_TXCLK	M1M_TXCLK	M1P_RXCLK
44	E1_DICLK	I	RG1_RXCLK	M1M_RXCLK	M1P_TXCLK
45	E1_DIDV	I	RG1_RXCTL	M1M_RXDV	M1P_TXEN
46	E1_DI0	I	RG1_RXD0	M1M_RXD0	M1P_TXD0
47	E1_DI1	I	RG1_RXD1	M1M_RXD1	M1P_TXD1
48	E1_DI2	I	RG1_RXD2	M1M_RXD2	M1P_TXD2
49	E1_DI3	I	RG1_RXD3	M1M_RXD3	M1P_TXD3

Table 21. RTL8364NB Extension Port 2 Pin Definitions

Pin No.	Extension Interface	Type	RGMII	MII MAC Mode	MII PHY Mode
23	E2_DO3	O	RG2_TXD3	M2M_TXD3	M2P_RXD3
24	E2_DO2	O	RG2_TXD2	M2M_TXD2	M2P_RXD2
25	E2_DO1	O	RG2_TXD1	M2M_TXD1	M2P_RXD1
26	E2_DO0	O	RG2_TXD0	M2M_TXD0	M2P_RXD0
27	E2_DOEN	O	RG2_TXCTL	M2M_TXEN	M2P_RXDV
28	E2_DOCLK	O	RG2_TXCLK	M2M_TXCLK	M2P_RXCLK
29	E2_DICLK	I	RG2_RXCLK	M2M_RXCLK	M2P_TXCLK
30	E2_DIDV	I	RG2_RXCTL	M2M_RXDV	M2P_TXEN
31	E2_DI0	I	RG2_RXD0	M2M_RXD0	M2P_TXD0
32	E2_DI1	I	RG2_RXD1	M2M_RXD1	M2P_TXD1
33	E2_DI2	I	RG2_RXD2	M2M_RXD2	M2P_TXD2
34	E2_DI3	I	RG2_RXD3	M2M_RXD3	M2P_TXD3

10.4.1. Extension Ports RGMII Mode (1Gbps)

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB support dual-port RGMII interfaces to an external CPU. The pin numbers and names are shown in Table 22 and Table 23. Figure 16 shows the signal diagram for Extension Port 1 and Extension Port 2 in RGMII interfaces.

Table 22. Extension GMAC1 RGMII Pins

RTL8364NB Pin No.	Type	Extension Port 1 RGMII
38, 39, 40, 41	O	RG1_TXD[3:0]
42	O	RG1_TXCTL
43	O	RG1_TXCLK
44	I	RG1_RXCLK
45	I	RG1_RXCTL
46, 47, 48, 49	I	RG1_RXD[0:3]

Table 23. Extension GMAC2 RGMII Pins

RTL8364NB Pin No.	Type	Extension Port 2 RGMII
23, 24, 25, 26	O	RG2_TXD[3:0]
27	O	RG2_TXCTL
28	O	RG2_TXCLK
29	I	RG2_RXCLK
30	I	RG2_RXCTL
31, 32, 33, 34	I	RG2_RXD[0:3]

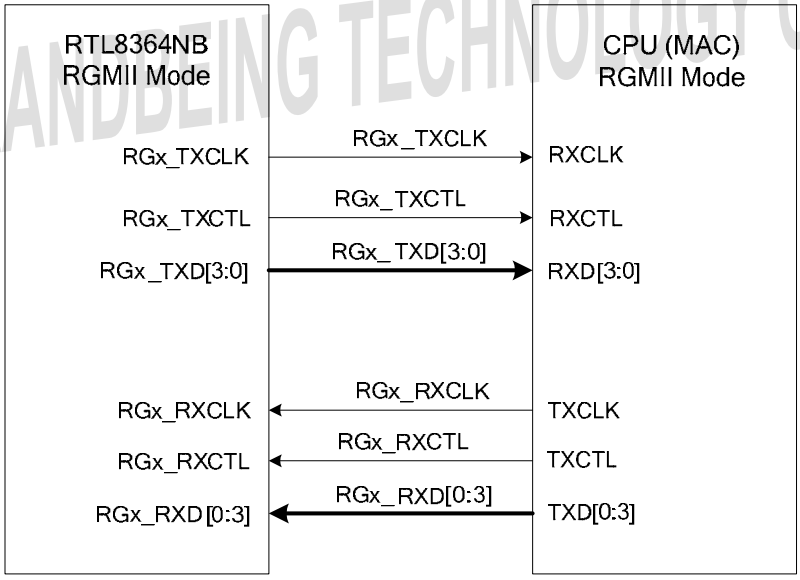


Figure 16. RGMII Mode Interface Signal Diagram

10.4.2. Extension Ports MII MAC/PHY Mode Interface (10/100Mbps)

Both the Extension GMAC1, and Extension GMAC2 of the RTL8364NB support MII MAC/PHY mode interfaces to an external CPU. The pin numbers and names are shown in Table 24, and Table 25.

Figure 17, page 48, shows the signal diagram for the MII PHY mode interface, and Figure 18, page 48, shows the signal diagram for the MAC mode interface.

Table 24. Extension GMAC1 MII Pins

RTL8364NB Pin No.	Type	Extension Port 1 MII MAC Mode	Type	Extension Port 1 MII PHY Mode
38, 39, 40, 41	O	M1M_TXD[3:0]	O	M1P_RXD[3:0]
42	O	M1M_TXEN	O	M1P_RXDV
43	I	M1M_TXCLK	O	M1P_RXCLK
44	I	M1M_RXCLK	O	M1P_TXCLK
45	I	M1M_RXDV	I	M1P_TXEN
46, 47, 48, 49	I	M1M_RXD[0:3]	I	M1P_TXD[0:3]

Table 25. Extension GMAC2 MII Pins

RTL8364NB Pin No.	Type	Extension Port 2 MII MAC Mode	Type	Extension Port 2 MII PHY Mode
23, 24, 25, 26	O	M2M_TXD[3:0]	O	M2P_RXD[3:0]
27	O	M2M_TXEN	O	M2P_RXDV
28	I	M2M_TXCLK	O	M2P_RXCLK
29	I	M2M_RXCLK	O	M2P_TXCLK
30	I	M2M_RXDV	I	M2P_TXEN
31, 32, 33, 34	I	M2M_RXD[0:3]	I	M2P_TXD[0:3]

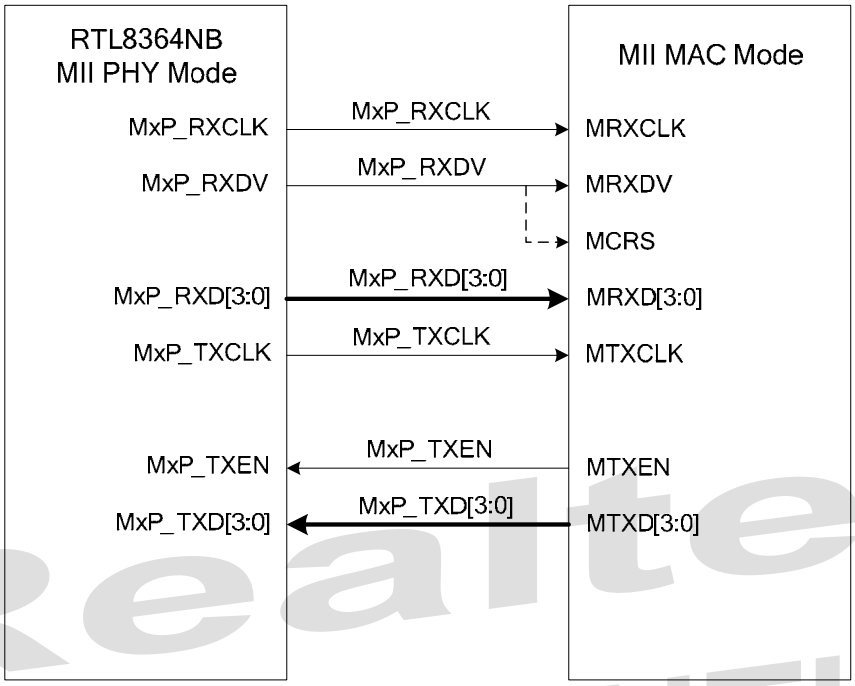


Figure 17. Signal Diagram of MII PHY Mode Interface (100Mbps)

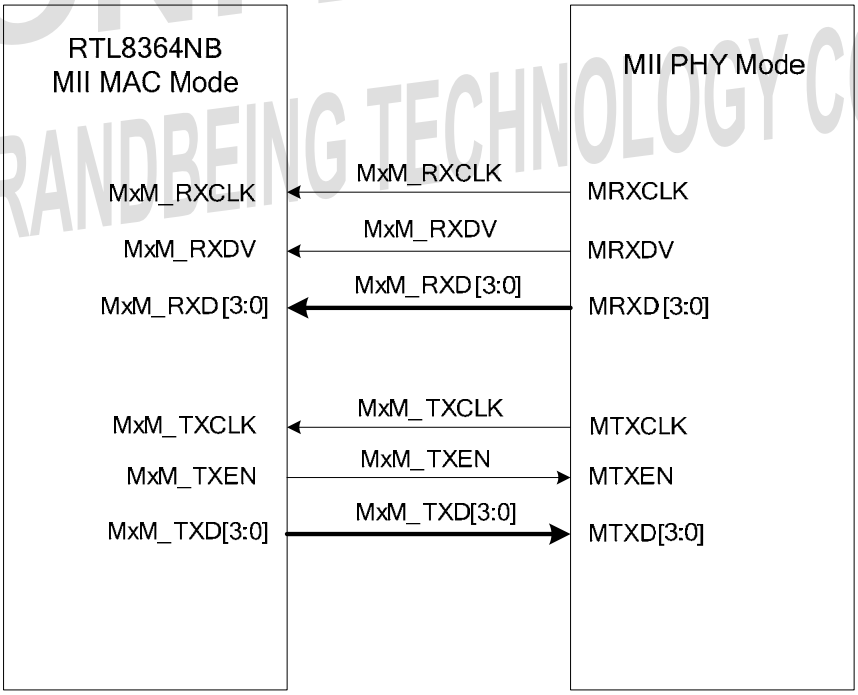


Figure 18. Signal Diagram of MII MAC Mode Interface (100Mbps)

11. Register Descriptions

In this section the following abbreviations are used:

RO: Read Only
RW: Read/Write
LL: Latch Low until clear
LH: Latch High until clear
SC: Self Clearing

11.1. PCS Register (PHY 0~4)

Table 26. PCS Register (PHY 0~4)

Register	Register Description	Default
0	Control Register	0x1140
1	Status Register	0x7949
2	PHY Identifier 1	0x001C
3	PHY Identifier 2	0xC942
4	Auto-Negotiation Advertisement Register	0x0DE1
5	Auto-Negotiation Link Partner Ability Register	0x0000
6	Auto-Negotiation Expansion Register	0x0004
7	Auto-Negotiation Page Transmit Register	0x2001
8	Auto-Negotiation Link Partner Next Page Register	0x0000
9	1000Base-T Control Register	0x0E00
10	1000Base-T Status Register	0x0000
11~14	Reserved	0x0000
15	Extended Status	0x2000
16~31	ASIC Control Register	-

11.2. Register 0: Control

Table 27. Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1: PHY reset 0: Normal operation This bit is self-clearing.	0
0.14	Loopback (Digital Loopback)	RW	1: Enable loopback. This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex, 100Base-TX full duplex, or 1000Base-T full duplex.	0
0.13	Speed Selection[0]	RW	[0.6, 0.13] Speed Selection[1:0] 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps This bit can be set through SMI (Read/Write).	0
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	1
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from GMII. The PHY is still able to respond to SMI 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation This bit can be set through SMI (Read/Write).	1
0.7	Collision Test	RO	1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.	0
0.6	Speed Selection[1]	RW	See bit 13	1
0.[5:0]	Reserved	RO	Reserved	000000

11.3. Register 1: Status

Table 28. Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base-T4	RO	0: No 100Base-T4 capability The RTL8364NB does not support 100Base-T4 mode and this bit should always be 0.	0
1.14	100Base-TX-FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base-TX-HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base-T-FD	RO	1: 10Base-T full duplex capable 0: Not 10Base-T full duplex capable	1
1.11	10Base-T-HD	RO	1: 10Base-T half duplex capable 0: Not 10Base-T half duplex capable	1
1.10	100Base-T2-FD	RO	0: Not 100Base-T2 full duplex capable The RTL8364NB does not support 100Base-T2 mode and this bit should always be 0.	0
1.9	100Base-T2-HD	RO	0: Not 100Base-T2 half duplex capable The RTL8364NB does not support 100Base-T2 mode and this bit should always be 0.	0
1.8	Extended Status	RO	1: Extended status information in Register 15 The RTL8364NB always supports Extended Status Register.	1
1.7	Reserved	RO	Reserved	0
1.6	MF Preamble Suppression	RO	The RTL8364NB will accept management frames with preamble suppressed.	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/LH	1: Remote fault condition detected 0: No remote fault detected This bit will remain set until it is cleared by reading register 1 via the management interface.	0
1.3	Auto-Negotiation Ability	RO	1: Auto-negotiation capable (permanently =1)	1
1.2	Link Status	RO/LL	1: Link is established. If the link fails, this bit will be 0 until after reading this bit again 0: Link has failed since previous read If the link fails, this bit will be set to 0 until bit is read.	0
1.1	Jabber Detect	RO/LH	1: Jabber detected 0: No Jabber detected Jabber is supported only in 10Base-T mode.	0
1.0	Extended Capability	RO	1: Extended register capable (permanently =1)	1

11.4. Register 2: PHY Identifier 1

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number, and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 29. Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	0x001C

11.5. Register 3: PHY Identifier 2

Table 30. Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the OUI	110010
3.[9:4]	Model Number	RO	Manufacturer's model number	010100
3.[3:0]	Revision Number	RO	Manufacturer's revision number	0010

11.6. Register 4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device as they will be transmitted to its Link Partner during Auto-negotiation.

Note: Each time the link ability of the RTL8364NB is reconfigured, the auto-negotiation process should be executed to allow the configuration to take effect.

Table 31. Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Additional next pages exchange desired 0: No additional next pages exchange desired	0
4.14	Acknowledge	RO	Permanently=0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8364NB has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved	0
4.11	Reserved	RW	Reserved	0
4.10	Pause	RW	1: Advertises that the RTL8364NB has flow control capability 0: No flow control capability	1
4.9	100Base-T4	RO	1: 100Base-T4 capable 0: Not 100Base-T4 capable (Permanently =0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1

Reg.bit	Name	Mode	Description	Default
4.6	10Base-T-FD	RW	1: 10Base-T full duplex capable 0: Not 10Base-T full duplex capable	1
4.5	10Base-T	RW	1: 10Base-T half duplex capable 0: Not 10Base-T half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

Note 1: The setting of Register 4 has no effect unless auto-negotiation is restarted or the link goes down.
Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted.

11.7. Register 5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after a successful Auto-negotiation.

Table 32. Register 5: Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Reserved	0
5.11	Asymmetric Pause	RO	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability	0
5.10	Pause	RO	1: Flow control supported by Link Partner. 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner	0
5.6	10Base-T-FD	RO	1: 10Base-T full duplex supported by Link Partner 0: 10Base-T full duplex not supported by Link Partner	0
5.5	10Base-T	RO	1: 10Base-T half duplex supported by Link Partner 0: 10Base-T half duplex not supported by Link Partner	0
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00000

11.8. Register 6: Auto-Negotiation Expansion

Table 33. Register 6: Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:5]	Reserved	RO	Ignore on read	0
6.4	Parallel Detection Fault	RO/ LH	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
6.3	Link Partner Next Page Ability	RO	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	0
6.2	Local Next Page Ability	RO	Not supported. Permanently =0	1
6.1	Page Received	RO/ LH	1: A New Page has been received 0: A New Page has not been received	0
6.0	Link Partner Auto-Negotiation Ability	RO	If Auto-Negotiation is enabled, this bit means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	0

11.9. Register 7: Auto-Negotiation Page Transmit Register

Table 34. Register 7: Auto-Negotiation Page Transmit Register

Reg.bit	Name	Mode	Description	Default
7.15	Next Page	RW	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
7.14	Reserved	RO	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
7.13	Message Page	RW	1: Message page 0: No Message page ability	1
7.12	Acknowledge 2	RW	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	0
7.11	Toggle	RO	Toggle bit	0
7.[10:0]	Message/ Unformatted Field	RW	Content of message/unformatted page	1

11.10. Register 8: Auto-Negotiation Link Partner Next Page Register

Table 35. Register 8: Auto-Negotiation Link Partner Next Page Register

Reg.bit	Name	Mode	Description	Default
8.15	Next Page	RO	Received Link Code Word Bit 15	0
8.14	Acknowledge	RO	Received Link Code Word Bit 14	0
8.13	Message Page	RO	Received Link Code Word Bit 13	0
8.12	Acknowledge 2	RO	Received Link Code Word Bit 12	0
8.11	Toggle	RO	Received Link Code Word Bit 11	0
8.[10:0]	Message/ Unformatted Field	RO	Received Link Code Word Bit 10:0	0

11.11. Register 9: 1000Base-T Control Register

Table 36. Register 9: 1000Base-T Control Register

Reg.bit	Name	Mode	Description	Default
9.[15:13]	Test Mode	RW	Test Mode Select. 000: Normal mode 001: Test mode 1 – Transmit waveform test 010: Test mode 2 – Transmit jitter test in MASTER mode 011: Test mode 3 – Transmit jitter test in SLAVE mode 100: Test mode 4 – Transmitter distortion test 101, 110, 111: Reserved	000
9.12	MASTER/SLAVE Manual Configuration Enable	RW	1: Enable MASTER/SLAVE manual configuration 0: Disable MASTER/SLAVE manual configuration	0
9.11	MASTER/SLAVE Configuration Value	RW	1: Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one 0: Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one	1
9.10	Port Type	RW	1: Multi-port device 0: Single-port device	1
9.9	1000Base-T Full Duplex	RW	1: Advertise PHY is 1000Base-T full duplex capable 0: Advertise PHY is not 1000Base-T full duplex capable	1
9.8	1000Base-T Half Duplex	RO	1: Advertise PHY is 1000Base-T half duplex capable 0: Advertise PHY is not 1000Base-T half duplex capable	0
9.[7:0]	Reserved	RW	Reserved	0

11.12. Register 10: 1000Base-T Status Register

Table 37. Register 10: 1000Base-T Status Register

Reg.bit	Name	Mode	Description	Default
10.15	MASTER/SLAVE Configuration Fault	RO/LH/SC	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected	0
10.14	MASTER/SLAVE Configuration Resolution	RO	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	0
10.13	Local Receiver Status	RO	1: Local receiver OK 0: Local receiver not OK	0
10.12	Remote Receiver Status	RO	1: Remote receiver OK 0: Remote receiver not OK	0
10.11	Link Partner 1000Base-T Full Duplex	RO	1: Link partner is capable of 1000Base-T full duplex 0: Link partner is not capable of 1000Base-T full duplex	0
10.10	1000Base-T Half Duplex	RO	1: Link partner is capable of 1000Base-T half duplex 0: Link partner is not capable of 1000Base-T half duplex	0
10.[9:8]	Reserved	RO	Reserved	0
10.[7:0]	Idle Error Count	RO/SC	Idle Error Counter. The counter stops automatically when it reaches 0xFF	0

11.13. Register 15: Extended Status

Table 38. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
15.15	1000Base-X Full Duplex	RO	1: 1000Base-X full duplex capable 0: Not 1000Base-X full duplex capable	0
15.14	1000Base-X Half Duplex	RO	1: 1000Base-X half duplex capable 0: Not 1000Base-X half duplex capable	0
15.13	1000Base-T Full Duplex	RO	1: 1000Base-T full duplex capable 0: Not 1000Base-T full duplex capable	1
15.12	1000Base-T Half Duplex	RO	1: 1000Base-T half duplex capable 0: Not 1000Base-T half duplex capable	0
15.[11:0]	Reserved	RO	Reserved	0

12. Electrical Characteristics

12.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 39. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, DVDDIO_1, DVDDIO_2, AVDDH, Supply Referenced to GND and AGND	GND-0.3	+3.63	V
DVDDL, AVDDL, SVDDL, PLLVDDL, Supply Referenced to GND, AGND, and PLLGND.	GND-0.3	+1.21	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

12.2. Recommended Operating Range

Table 40. Recommended Operating Range

Parameter		Min	Typical	Max	Units
Ambient Operating Temperature (Ta)		0	-	70	°C
DVDDIO, AVDDH Supply Voltage Range		3.135	3.3	3.465	V
DVDDIO_2 Supply Voltage Range (DVDDIO_2: Extension Port 2 Supports 2.5V or 3.3V)	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
DVDDIO_1 Supply Voltage Range (DVDDIO_1: Extension Port 1 Supports 1.8V, 2.5V, or 3.3V)	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
	1.8V	1.710	1,8	1.890	V
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Voltage Range		1.045	1.1	1.155	V

12.3. Thermal Characteristics

12.3.1. Assembly Description

Table 41. Assembly Description

Package	Type	QFN88
	Dimension (L×W)	10×10mm
	Thickness	0.65mm
PCB	PCB Dimension (L×W)	70x87 mm
	PCB Thickness	1.6mm
	Number of Cu Layer-PCB	2-Layer: - Top layer (1oz): 20% coverage of Cu - Bottom layer (1oz): 75% coverage of Cu 4-Layer: - 1st layer (1oz): 20% coverage of Cu - 2nd layer (1oz): 80% coverage of Cu - 3rd layer (1oz): 80% coverage of Cu - 4th layer (1oz): 75% coverage of Cu

12.3.2. Material Properties

Table 42. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.88
PCB		Cu	400
		FR4	0.2

12.3.3. Simulation Conditions

Table 43. Simulation Conditions

Input Power	1.8W
Test Board (PCB)	2L (2S)/4L (2S2P)
Control Condition	Air Flow = 0, 1, 2, m/s

12.3.4. Thermal Performance of QFN-88 on PCB Under Still Air Convection

Table 44. Thermal Performance of QN-88 on PCB Under Still Air Convection

	θ_{JA}	θ_{JC}	Ψ_{JT}
4L PCB	20	4	0.07
2L PCB	23.1	4.2	0.08

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JT}: Junction to top center of package thermal characterization

12.3.5. Thermal Performance of QFN-88 on PCB Under Forced Convection

Table 45. Thermal Performance of QFN-88 on PCB Under Forced Convection

	Air Flow (m/s)	0	1	2
4L PCB	θ_{JA}	20	16.3	15.1
2L PCB	θ_{JA}	23.1	19.1	17.9

Note:
θ_{JA}: Junction to ambient thermal resistance

12.4. DC Characteristics

Table 46. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
Power Supply Current for RGMII1 DVDDIO_1 (2.5V) (For General Purpose Interface)	I_{DVDDIO_1}	-	30	-	mA
Power Supply Current for RGMII1 DVDDIO_2 (2.5V) (For General Purpose Interface)	I_{DVDDIO_2}	-	31	-	mA
System Idle (All UTP Port Link Down, and 1 Extension Port Configured as HSGMII, without LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	19	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	204	-	mA
1000M Active (All UTP Ports Link/Active, and 1 Extension Port Configured as HSGMII, without LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	112	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	467	-	mA
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	2.0	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V
VDDIO=2.5V					
TTL Input High Voltage	V_{ih}	1.7	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.6	V
Output High Voltage	V_{oh}	2.25	-	-	V
Output Low Voltage	V_{ol}	-	-	0.4	V
VDDIO=1.8V					
TTL Input High Voltage	V_{ih}	1.2	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.6	V
Output High Voltage	V_{oh}	1.45	-	-	V
Output Low Voltage	V_{ol}	-	-	0.4	V

Note: Both I_{DVDDIO_1} & I_{DVDDIO_2} should be added to the total current consumption when the dual extension ports of the RTL8364NB are used.

12.5. AC Characteristics

12.5.1. EEPROM SMI Host Mode Timing Characteristics

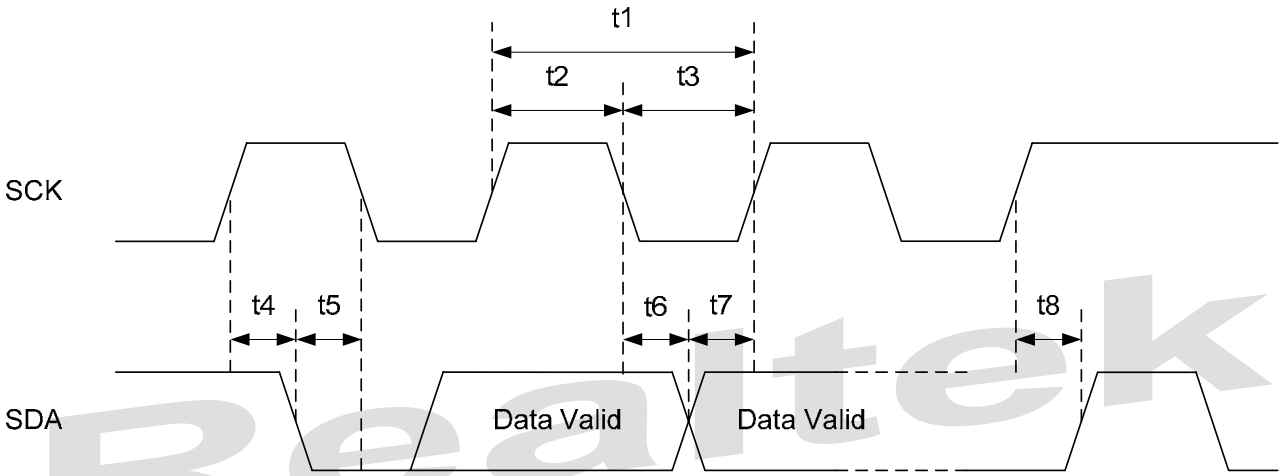


Figure 19. EEPROM SMI Host Mode Timing Characteristics

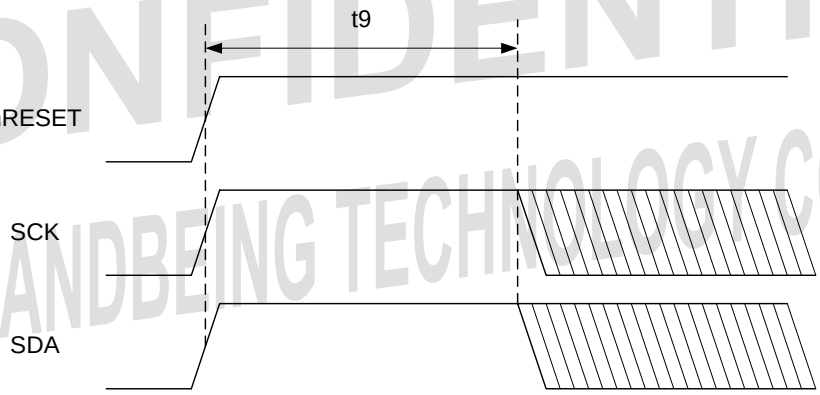


Figure 20. SCK/SDA Power on Timing

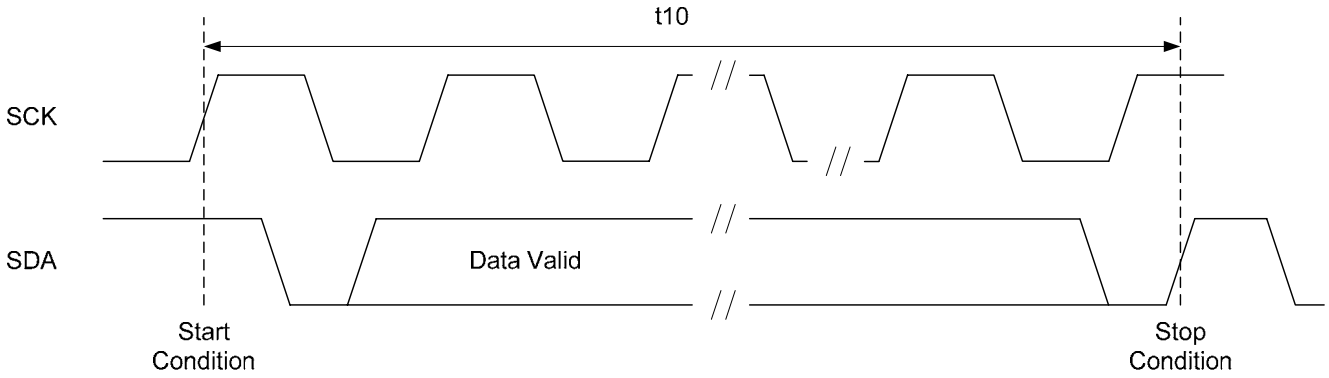


Figure 21. EEPROM Auto-Load Timing

Table 47. EEPROM SMI Host Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK Clock Period	O	9.7	10	-	µs
t2	SCK High Time	O	4.2	5	-	µs
t3	SCK Low Time	O	4.2	5	-	µs
t4	START Condition Setup Time	O	4.8	5.04	-	µs
t5	START Condition Hold Time	O	4.8	4.96	-	µs
t6	Data Hold Time	O	2.2	2.52	-	µs
t7	Data Setup Time	O	2.2	2.48	-	µs
t8	STOP Condition Setup Time	O	4.4	5.04	-	µs
t9	SCK/SDA Active from Reset Ready	O	75	78.4	-	ms
t10	8K-Bits EEPROM Auto-Load Time	O	250	278	-	ms
-	SCK Rise Time (10% to 90%)	O	-	320	-	ns
-	SCK Fall Time (90% to 10%)	O	-	320	-	ns
-	Duty Cycle	O	48.86	50	51.14	%

12.5.2. EEPROM SMI Slave Mode Timing Characteristics

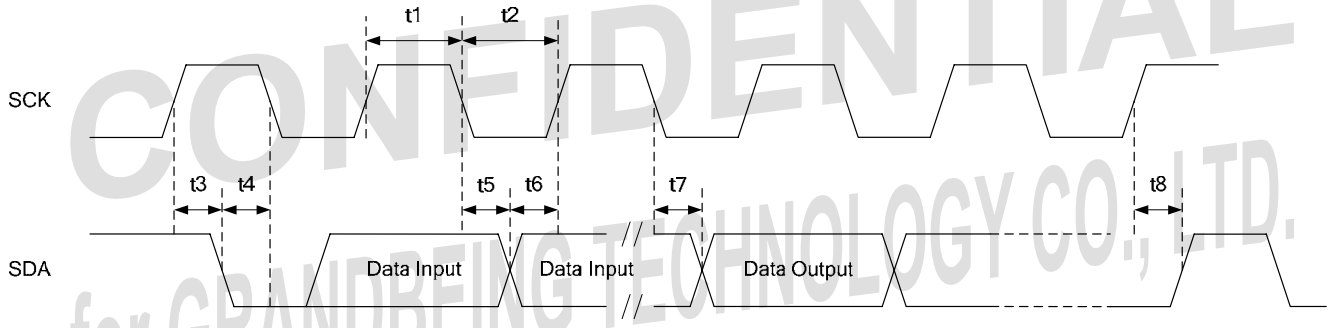


Figure 22. EEPROM SMI Slave Mode Timing Characteristics

Table 48. EEPROM SMI Slave Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK High Time	I	250	-	-	ns
t2	SCK Low Time	I	250	-	-	ns
t3	START Condition Setup Time	I	150	-	-	ns
t4	START Condition Hold Time	I	150	-	-	ns
t5	Data Hold Time	I	150	-	-	ns
t6	Data Setup Time	I	150	-	-	ns
t7	Clock to Data Output Delay	O	-	100	-	ns
t8	STOP Condition Setup Time	I	150	-	-	ns

12.5.3. SPI Slave Mode Timing Characteristics

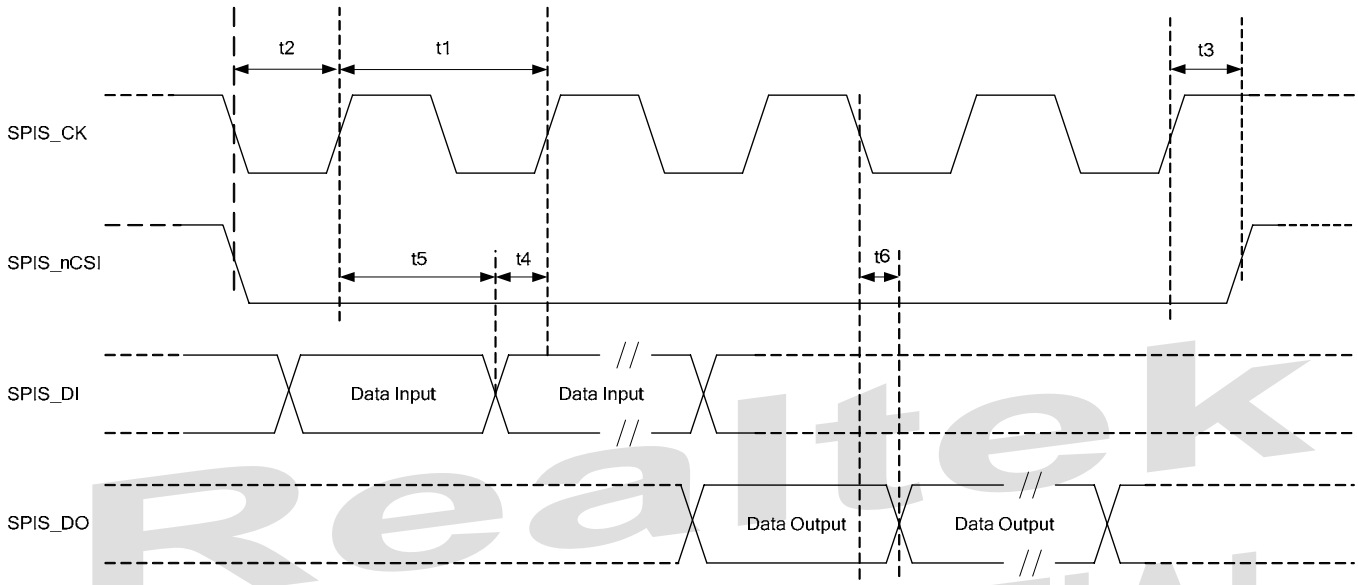


Figure 23. SPI-Slave Mode Timing Characteristics

Table 49. SPI-Slave Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SPIS_CK Clock Period	I	200	-	-	ns
t2	SPIS_nCSI active setup time relative to SPIS_CK	I	30	-	-	ns
t3	SPIS_nCSI active hold time relative to SPIS_CK	I	30	-	-	ns
t4	SPIS_DI to SPIS_CK Setup Time	I	30	-	-	ns
t5	SPIS_DI to SPIS_CK Hold Time	I	30	-	-	ns
t6	SPIS_CK Falling Edge to SPIS_DO Output Delay Time	O	10	24	-	ns

12.5.4. MDIO Slave Mode Timing Characteristics

The RTL8364NB supports MDIO (MMD) slave mode. The Master (CPU) can access the Slave (RTL8364NB) registers via the MDIO interface. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the master sources the MDIO signal. In a read command, the slave sources the MDIO signal.

- The timing characteristics t1, t2, and t3 (Table 50) of the Master (the RTL8364NB link partner CPU) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristics t4 (Table 50) of the Slave (RTL8364NB) are provided by the RTL8364NB when the RTL8364NB sources the MDIO signal (Read command)

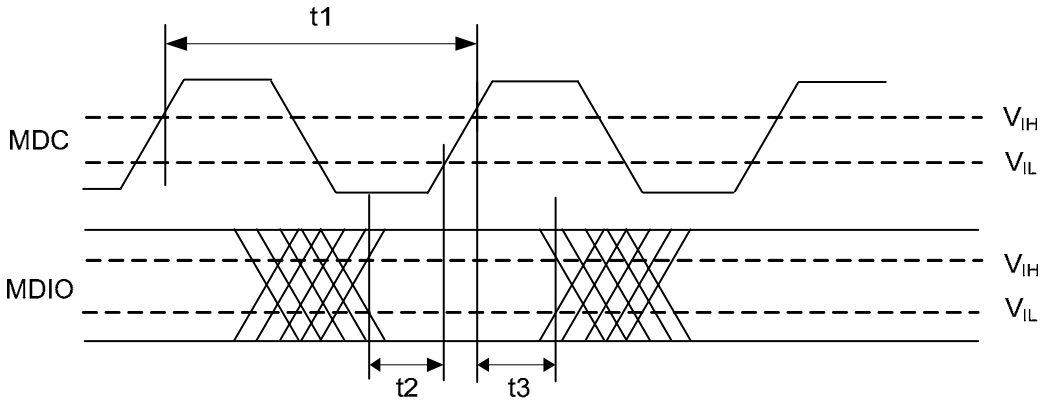


Figure 24. MDIO Sourced by Master

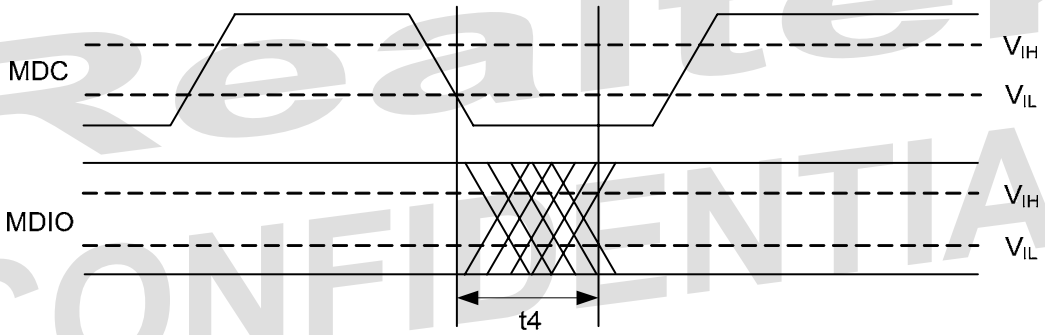


Figure 25. MDIO Sourced by RTL8364NB (Slave)

Table 50. MDIO Timing Characteristics and Requirement

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	125	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	25	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	25	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Falling Edge) to Data Delay Time	O	0	2.8	40	ns

12.5.5. MII MAC Mode Timing

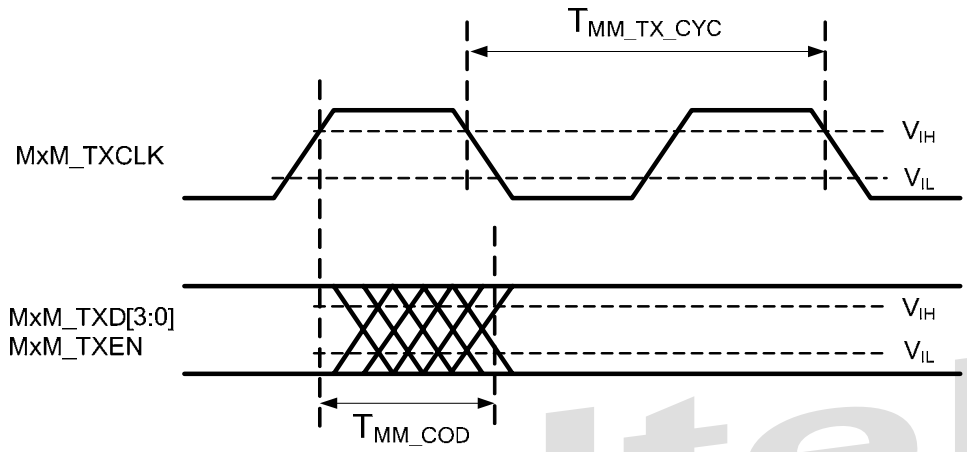


Figure 26. MII MAC Mode Clock to Data Output Delay Timing

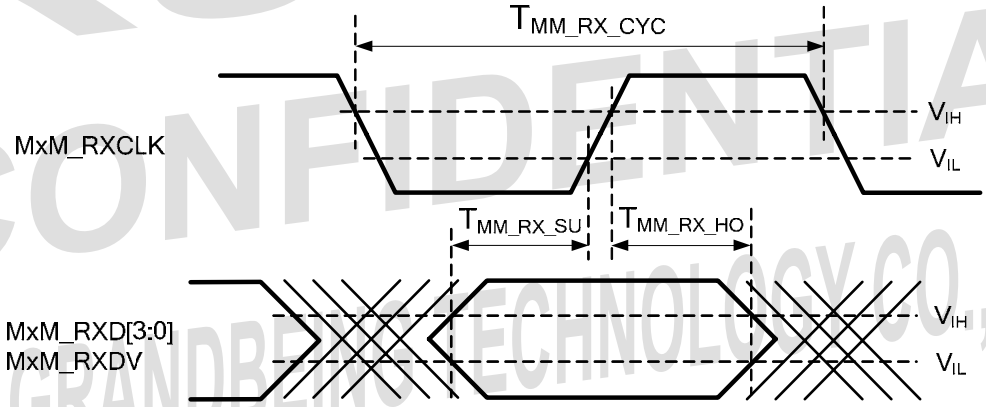


Figure 27. MII MAC Mode Input Timing

Table 51. MII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-TX MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	25MHz Clock Input.	I	-	40	-	ns
10Base-T MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	2.5MHz Clock Input.	I	-	400	-	ns
MxM_TXCLK to MxM_TXD[3:0] and MxM_TXEN Output Delay Time	T_{MM_COD}	-	O	3	5	7	ns
MxM_RXD[3:0], MxM_RXDV, and MxM_CRS Input Setup Time	$T_{MM\_RX\_SU}$	-	I	10	-	-	ns
MxM_RXD[3:0] and MxM_RXDV Input Hold Time	$T_{MM\_RX\_HO}$	-	I	10	-	-	ns

12.5.6. MII PHY Mode Timing

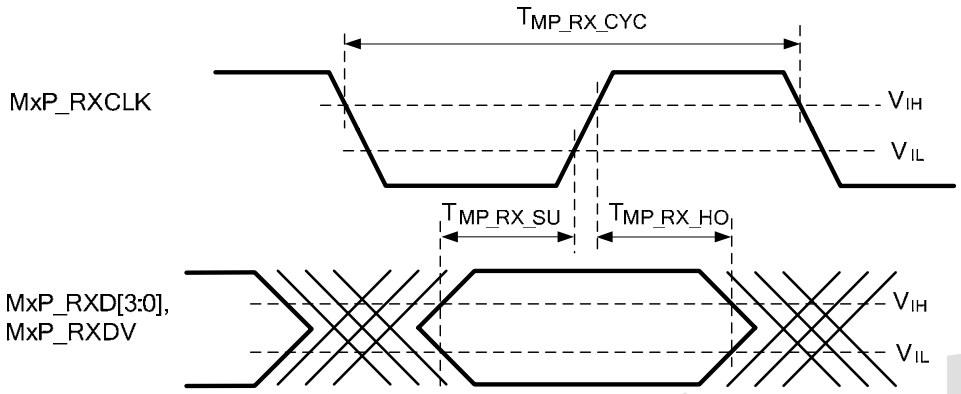


Figure 28. MII PHY Mode Output Timing

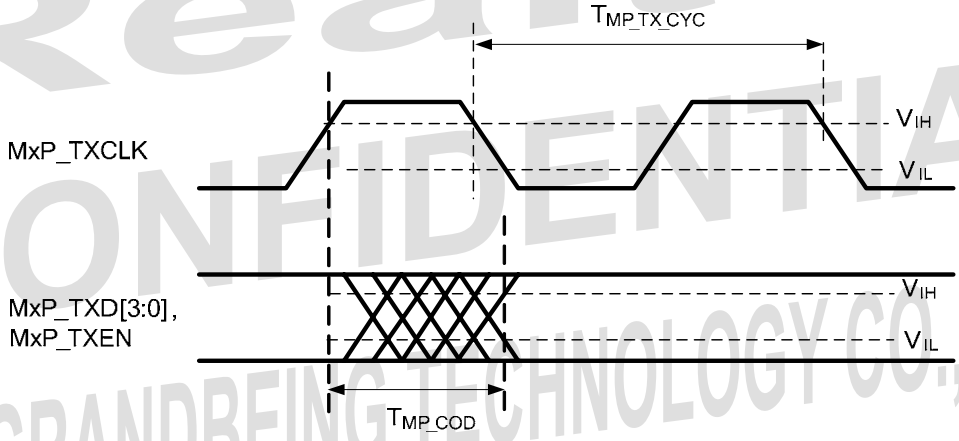


Figure 29. MII PHY Mode Clock Output to Data Input Delay Timing

Table 52. MII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	25MHz Clock Output.	O	-	40	-	ns
10M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	2.5MHz Clock Output.	O	-	400	-	ns
100M MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Setup Time	$T_{MP\_RX\_SU}$	-	O	14	18	-	ns
100M MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Hold Time	$T_{MP\_RX\_HO}$	-	O	16	19.5	-	ns
100M MxP_TXCLK Clock Output to MxP_TXD[3:0] and MxP_TXEN Input Delay Time	T_{MP_COD}	-	I	0	-	25	ns

12.5.7. RGMII Timing Characteristics

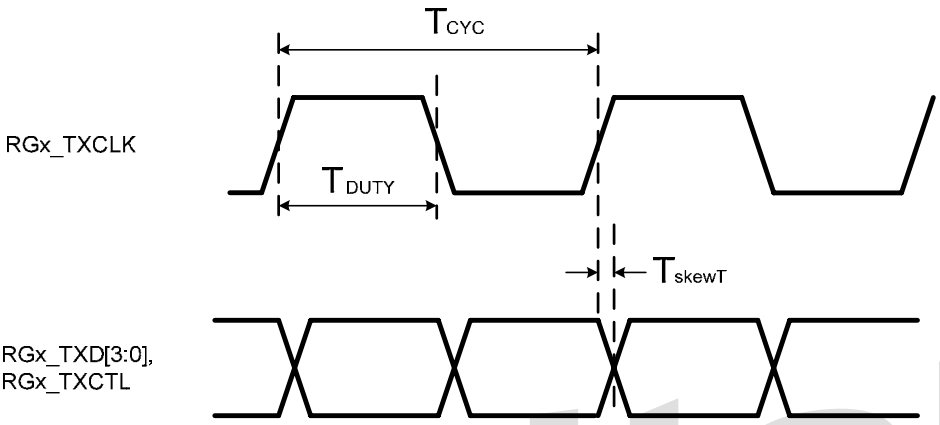


Figure 30. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=0)

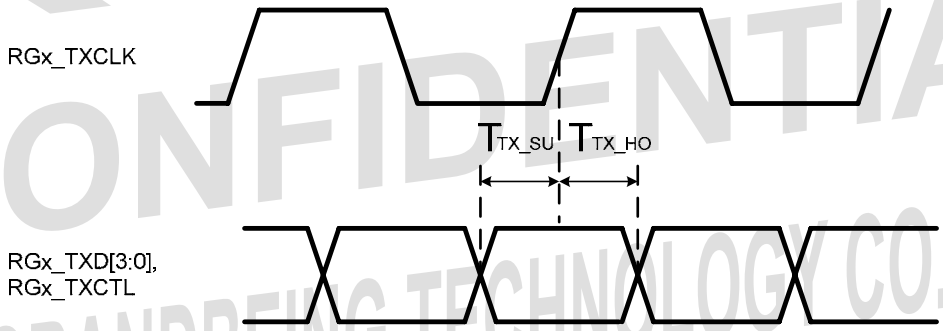


Figure 31. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=2ns)

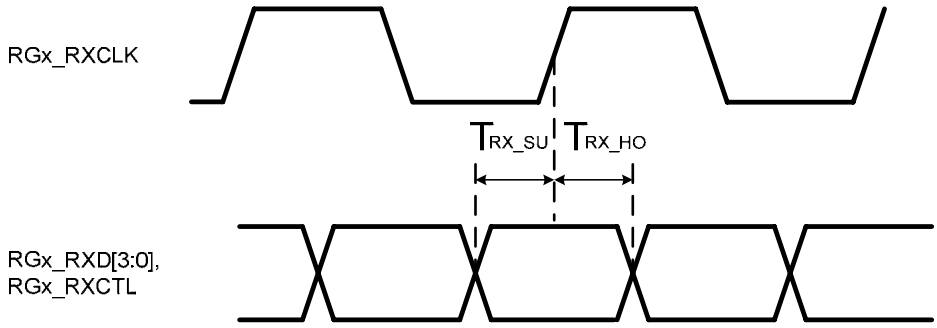


Figure 32. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=0)

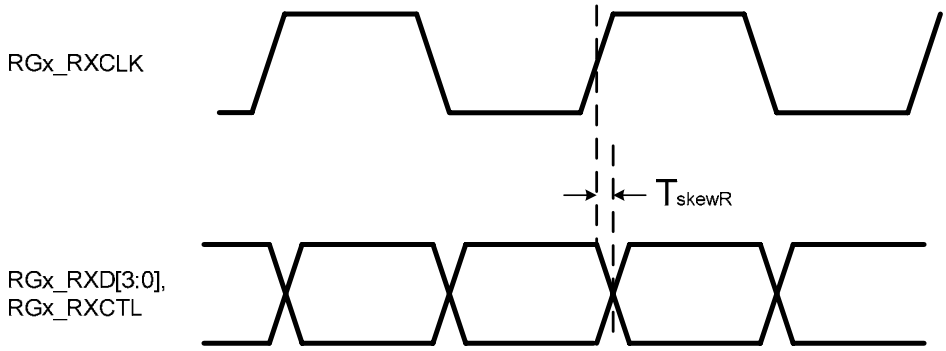


Figure 33. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=2ns)

Table 53. RGMII Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
1000M RGx_TXCLKc Output Cycle Time	T_{TX_CYC}	125MHz Clock Output. Refer to Figure 30, page 67.	O	7.6	8	8.6	ns
100M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	25MHz Clock Output. Refer to Figure 30, page 67.	O	38	40	42	ns
10M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	2.5MHz Clock Output. Refer to Figure 30, page 67.	O	380	400	420	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Skew	T_{skewT}	Disable Output Clock Delay. (RGx_TXCLK_DELAY=0). Refer to Figure 30, page 67.	O	-500	-	500	ps
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Setup Time	T_{TX_SU}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 31, page 67.	O	1.2	-	-	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Hold Time	T_{TX_HO}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 31, page 67.	O	1.2	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Setup Time	T_{RX_SU}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 32, page 67.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Hold Time	T_{RX_HO}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 32, page 67.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Skew	T_{skewR}	Enable Input Clock Delay. (RGx_RXCLK_DELAY=1). Refer to Figure 33, page 68.	I	-600	-	600	ps

12.5.8. HSGMII Characteristics

Table 54. HSGMII Differential Transmitter Characteristics

Parameter		SYM	Min	Typ	Max	Units	Notes
Unit Interval		UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask		T_X1	-	-	0.175	UI	-
Eye Mask		T_X2	-	-	0.39	UI	-
Eye Mask		T_Y1	400	-	-	mV	-
Eye Mask		T_Y2	-	-	800	mV	-
Output Differential Voltage		$V_{TX-DIFFp-p}$	500	700	1000	mV	-
Output Jitter	TJ	$T_{TX-JITTER}$	-	-	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.30UI
	DJ		-	-	0.165	UI	
Minimum TX Eye Width		T_{TX-EYE}	0.65	-	-	UI	-
Output Rise Time		$T_{TX-RISE}$	0.125	-	-	UI	20% ~ 80%
Output Fall Time		$T_{TX-FALL}$	0.125	-	-	UI	20% ~ 80%
Differential Resistance		R_{TX}	80	100	120	ohm	-
AC Coupling Capacitor		C_{TX}	80	100	120	nF	-
Transmit Length in PCB		L_{TX}	-	-	10	inch	-

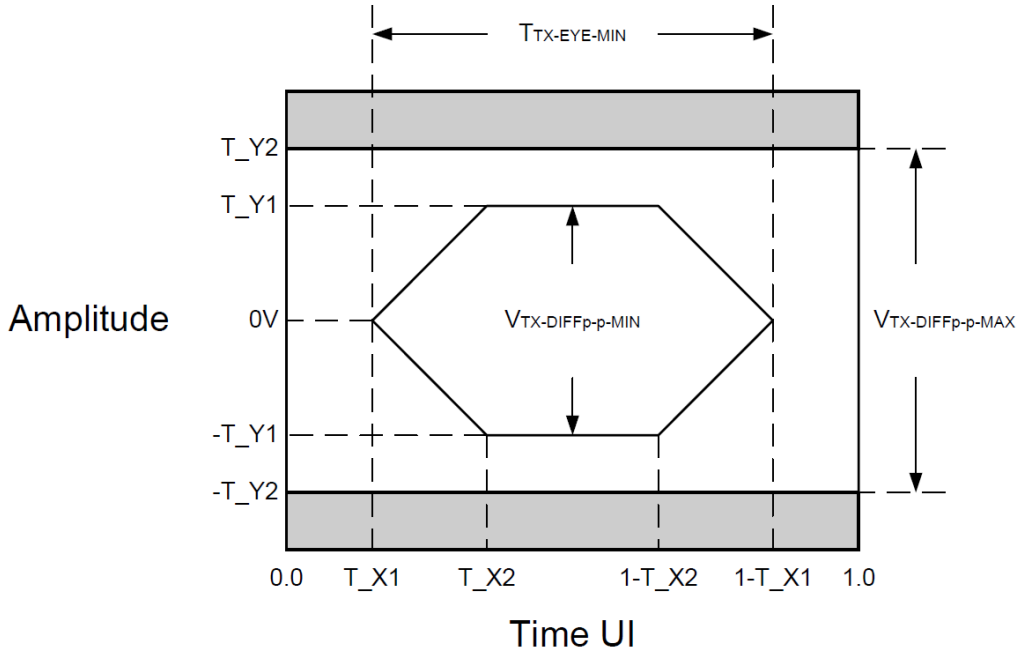


Figure 34. HSGMII Differential Transmitter Eye Diagram

Table 55. HSGMII Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask	R_X1	-	-	0.275	UI	-
Eye Mask	R_Y1	100		-	mV	
Eye Mask	R_Y2	-	-	800	mV	-
Input Differential Voltage	$V_{RX-DIFFp-p}$	200	-	1200	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-JITTER}$	-	-	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.6UI
Differential Resistance	R_{RX}	80	100	120	ohm	-

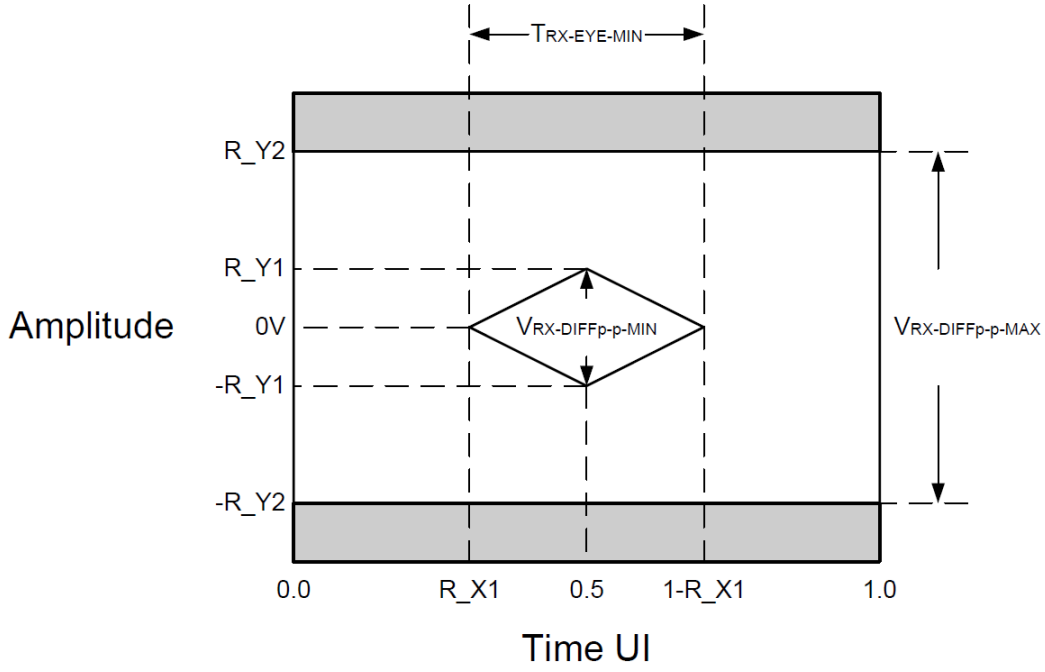


Figure 35. HSGMII Differential Receiver Eye Diagram

12.5.9. SGMII Characteristics

Table 56. SGMII Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.92	800	800.08	ps	800ps ± 100ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mV	-
Eye Mask	T_Y2	-	-	400	mV	-
Output Differential Voltage	$V_{TX-DIFFp-p}$	300	700	800	mV	-
Minimum TX Eye Width	T_{TX-EYE}	0.7	-	-	UI	-
Output Jitter	$T_{TX-JITTER}$	-	-	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.30UI
Data dependent jitter		-	70	-	ps	
Output Rise Time	$T_{TX-RISE}$	100	-	200	ps	20% ~ 80%
Output Fall Time	$T_{TX-FALL}$	100	-	200	ps	20% ~ 80%
Output impedance	R_{TX}	40	-	140	ohm	single-end
AC Coupling Capacitor	C_{TX}	80	100	120	nF	-
Transmit Length in PCB	L_{TX}	-	-	10	inch	-

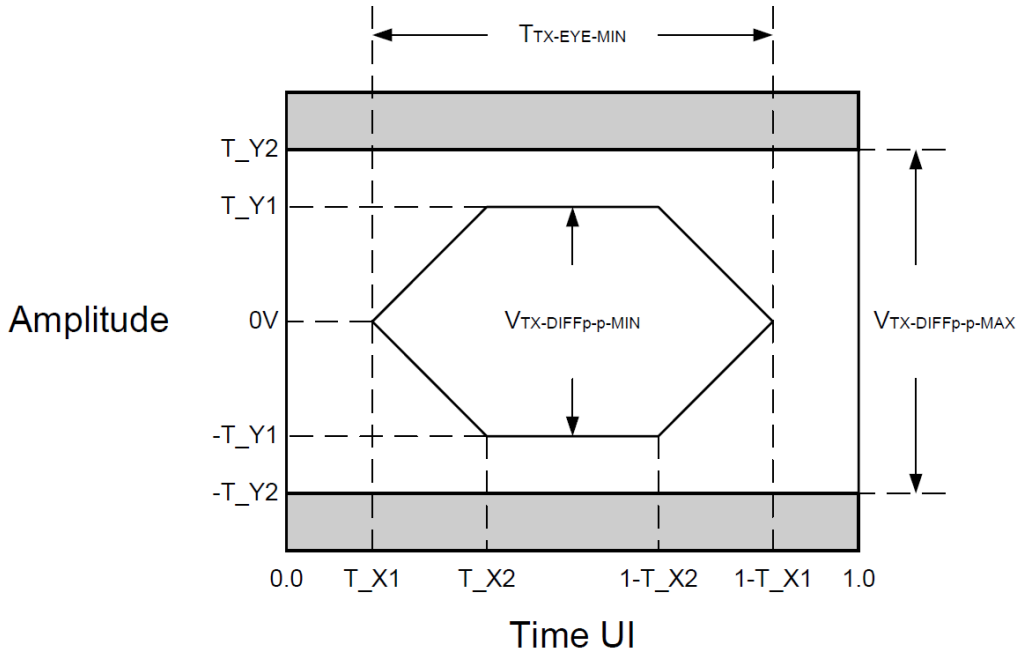


Figure 36. SGMII Differential Transmitter Eye Diagram

Table 57. SGMII Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.92	800	800.08	ps	800ps ± 100ppm
Eye Mask	R_X1	-	-	0.15	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	600	mV	-
Input Differential Voltage	$V_{RX-DIFFp-p}$	200	-	1200	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-JITTER}$	-	-	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.6UI
Differential Resistance	R_{RX}	80	100	120	ohm	-

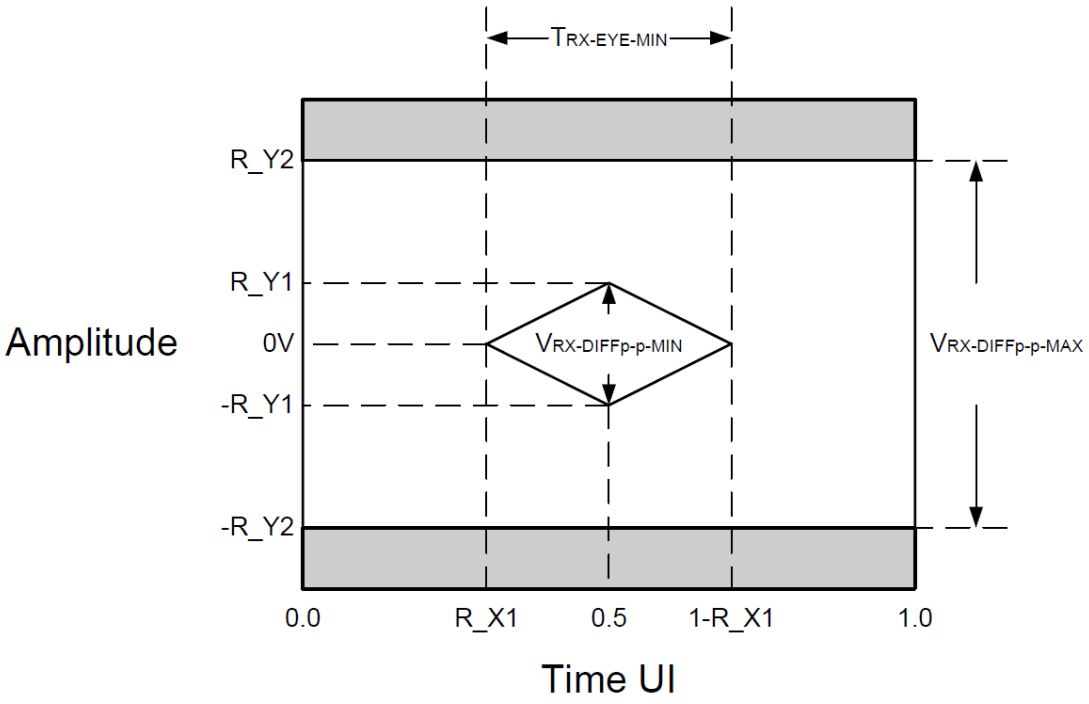


Figure 37. SGMII Differential Receiver Eye Diagram

12.6. Power and Reset Characteristics

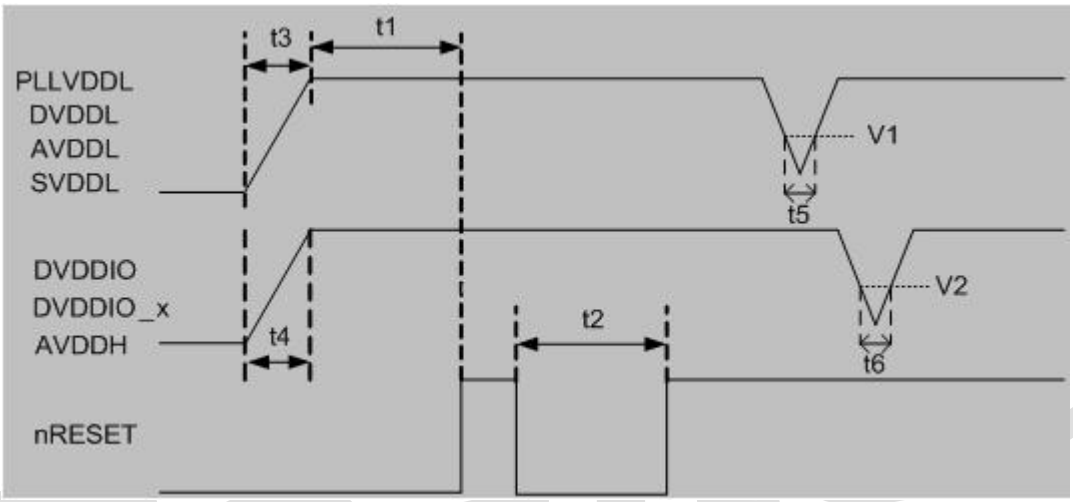


Figure 38. Power and Reset Characteristics

Table 58. Power and Reset Timing Requirements

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
Reset Delay Time	t1	The duration from 'all power steady' to the reset signal released to high	I	0	-	-	ms
Reset Low Time	t2	The duration of reset signal remaining low time before issuing a reset to the RTL8364NB	I	10	-	-	ms
VDDL Power Rise Time	t3	SVDDL, PLLVDDL, DVDDL and AVDDL power rise time.(10% ~90%)	I	0.5	-	10	ms
VDDH Power Rise Time	t4	DVDDIO, DVDDIO_x, and AVDDH power rise time.(10% ~90%)	I	0.5	-	10	ms

Table 59. Power Monitor Reset Characteristics

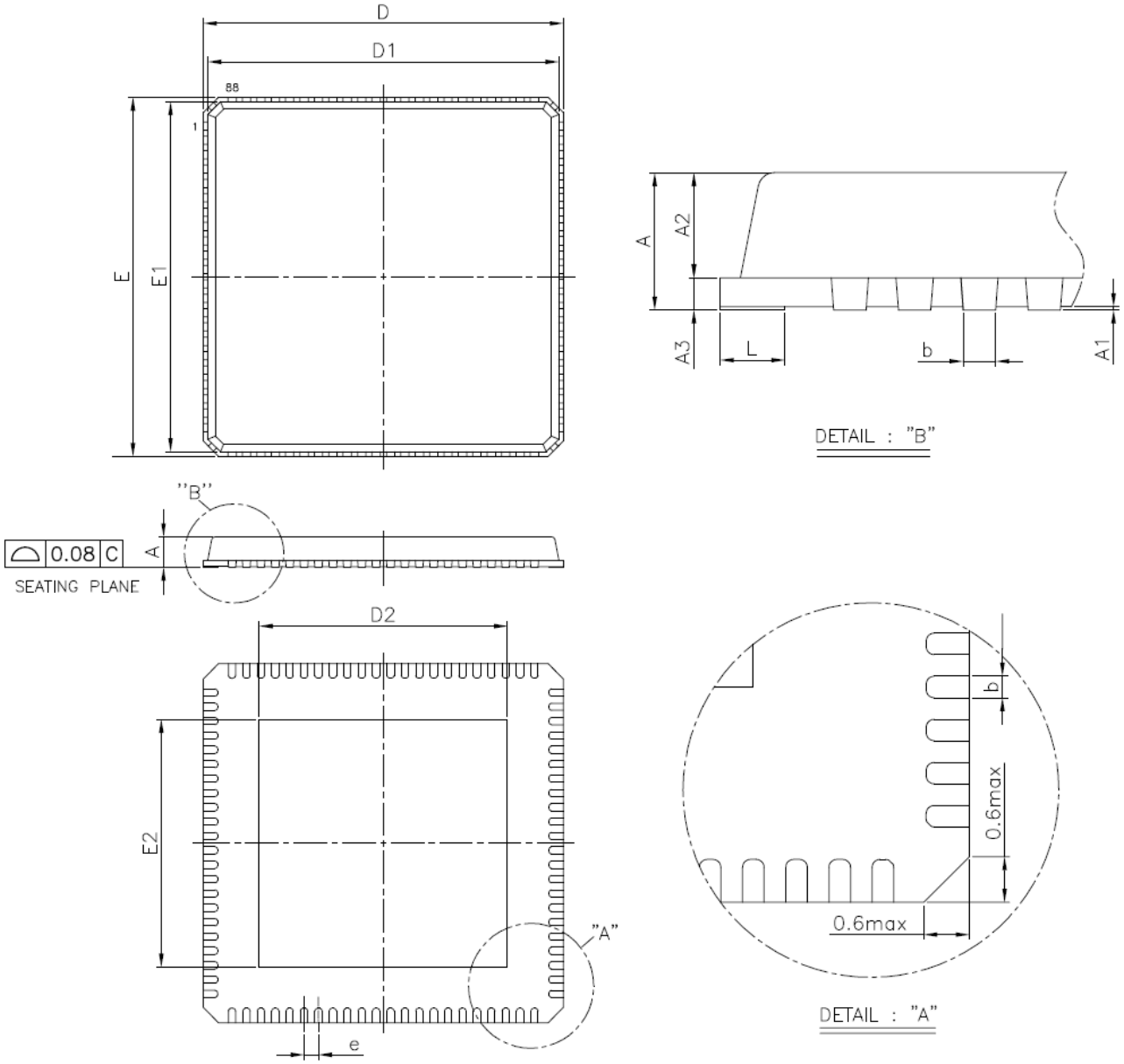
Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
Duration of VDDL power monitor reset	t5	The duration to issue power monitor reset when VDDL voltage drop lower than voltage threshold V1.	I	0.2	-	-	µs
Duration of VDDH power monitor reset	t6	The duration to issue power monitor reset when VDDH voltage drop lower than voltage threshold V2.	I	0.2	-	-	µs
Voltage drop threshold of VDDL power monitor reset	V1	The VDDL voltage drop threshold to issue power monitor reset.	I	0.5	-	0.99	V
Voltage drop threshold of VDDH power monitor reset	V2	The VDDH voltage drop threshold to issue power monitor reset.	I	1.65	-	2.97	V

Note 1: The VDDL power monitor reset will occur when VDDL voltage drops lower than V1 for a duration larger than t5. It will be in an unknown state when VDDL voltage drops to 0.99V~0.5V.

Note 2: The VDDH power monitor reset will occur when VDDH voltage drops lower than V2 for a duration larger than t6. It will be in an unknown state when VDDH voltage drops to 2.97V~1.65V.

13. Mechanical Dimensions

Thermally Enhanced Quad Flat Package (QFN) 88 Leads 10×10mm Outline.



13.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	-	0.65	0.70	-	0.026	0.028
A_3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		10.00BSC			0.394BSC	
D_1/E_1		9.75BSC			0.384BSC	
D_2/E_2	6.65	6.90	7.15	0.262	0.272	0.282
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

CONTROLLING DIMENSION: MILLIMETER (mm).
REFERENCE DOCUMENT: JEDEC MO-220.

14. Ordering Information

Table 60. Ordering Information

Part Number	Package	Status
RTL8364NB-CG	QFN 88-Pin 'Green' Package	-

Note: See page 7 for package identification.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com