RTL839x/RTL835x
CPU, Memory Controller, and Peripherals

DATASHEET
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8390 chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2012/12/14	Initial release
1.1	2014/06/25	Update CPU frequence

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RTL8390 CPU Specification

1.1. Features List

- MIPS 34Kc CPU Core at 700MHz
  - 9 stage-pipeline
  - MIPS32 instruction set
  - Additional MIPS16e instruction set support
  - 2 GPR set (one shadow set)
  - Vectored interrupts, Non-maskable interrupts (NMI) supports
- Cache Configuration:
  - I-Cache: 32KB, 4-way set associative, 32 byte line size
  - D-Cache: 32KB, 4-way set associative, 32 byte line size, write back policy
  - Virtually indexed, physically tagged
  - PREF instruction
- MMU Configuration
  - 4 entry ITLB
  - 4 entry DTLB
  - 32 entry JTLB
- Misc.
  - Power-down mode (WAIT instruction)
  - EJTAG support
  - Internal BIST
  - Internal real-time timer interrupts (Count/Compare registers)
  - CPU breakpoints

2. RTL8390 Memory Controller Specification

- Following types of memory devices are supported.
  - DDR1/DDR2/DDR3 SDRAM
  - SPI FLASH
- Boot up from SPI FLASH
  - Supports memory mapped I/O for read operation.

2.1. Memory Address Mapping

The following table only lists related memory address for memory controller's usage.

Table 1. Memory Address Mapping

Physical Memory Address Range	Size	Description
0x0000_0000 ~ 0x0FFF_FFFF	256 MB	DRAM Region *TLB map is used when more than 256MB
0x1400_0000 ~ 0x17FF_FFFF	64 MB	SPI Flash Region 1
0x1FC0_0000 ~ 0x1FFF_FFFF	4 MB	SPI Flash Region 2

- Due to the limitation of MIPS architecture, "SPI Flash Region 2"can only access the first 4MB of SPI flash. To access the full space of SPI flash, please use "SPI Flash Region 1"instead.

2.2. DDR SDRAM Controller

2.2.1. Feature lists

- Interface (Bus Width): 8 bit /16 bit
- Targeted DDR Frequency: up to 200MHz
- Targeted OCP Bus Frequency: up to 750MHz, synchronous with CPU
- Two chip selects (CS0# and CS1#)
- Supported DDR SDRAM chip spec
  - Bank counts: 4
  - Row counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9,A11), 4K (A0~A9,A11,A12)
- Programmable timing parameters
  - tRAS, tRP, tRCD, tCL, tREFI, …

2.3. DDR2 SDRAM Controller

2.3.1. Feature lists

- Interface (Bus Width): 8 bit / 16 bit
- Targeted DDR2 Frequency: up to 400MHz (DDR2-800)
- Targeted OCP Bus Frequency: up to 750 MHz, synchronous with CPU
- Two chip selects (CS0# and CS1#)
- Supported DDR2 SDRAM chip spec
  - Bank counts: 4, 8
  - Row counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9,A11), 4K (A0~A9,A11,A12)
- Programmable timing parameters
  - tRAS, tRP, tRCD, tCL, tREFI,…
- Fixed DDR2 parameters.
  - AL = 0.
  - Some DDR2 DRAM introduces tRPA timing parameter (in Micron chip). We merge tRPA with tRP into one parameter.
  - No tRTP. Need to check DDR2 Bus waveform to confirm there is no tRTP violation.

2.4. DDR3 SDRAM Controller

2.4.1. Feature lists

- Interface (Bus Width): 8 bit / 16 bit
- Targeted DDR3 Frequency: up to 400MHz (DDR3-800)
- Targeted OCP Bus Frequency: up to 750 MHz, synchronous with CPU
- Two chip selects (CS0# and CS1#)
- Supported DDR3 SDRAM chip spec
  - Bank counts: 4, 8
  - Row counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9,A11), 4K (A0~A9,A11,A12)
- Programmable timing parameters
  - tRAS, tRP, tRCD, tCL, tREFI,…

2.5. SPI FLASH Controller

2.5.1. Feature lists

- Targeted SPI flash frequency: up to 100MHz
- Four chip selects (CS0#, CS1#, CS2#, and CS1#)

- In addition to programmed I/O interface, memory-mapped I/O interface for read operation is also supported.
- In memory-mapped I/O mode, 8-bit command code is user-configurable in order to accommodate different commands of different vendors.
- In addition to preliminary serial I/O mode, new dual I/O and quad I/O modes are also supported.
- Supports cached read access for better performance.

2.6. Memory Cache Controller

2.6.1. Feature lists

- 4 cache lines; size of each line is 16 bytes.
- Every 4 byte has a valid bit.
- Cache association: Direct map.
- Only cached the SPI flash memory data in the current design.
- Read-only.
- OCP request only.
- Invalidate operation is supported.

2.7. SRAM Controller

2.7.1. Feature lists

- Dual interfaces: OCP and Lexra.
- Internal arbitration of requests between OCP and Lexra.
- Embedded SRAM size is 96KB.
- Supports size registers and base registers to further partition and allocate as many as 4 SRAM segments out of the total 96KB; Supports base registers to specify the host memory-mapped addresses of each SRAM segment.
- In external CPU mode, the SRAM controller runs on LX bus clock.

2.8. Software Register Definition

2.8.1. Memory Control Register (MCR) (0xB800_1000)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:28	DRAMTYPE	Report the hardware strapping initial value for DRAM type 0000: DDR1 0001: DDR2 0010: DDR3 Others: reserved	R	0000B (H/W Pin)
27:24	*reserved*		R	0
23	IPREF	Enable instruction prefetch function. 0: Disable prefetch. (also reset buffer status) 1: Enable prefetch (4 words)	R/W	0B
22	DPREF	Enable data prefetch function. 0: Disable prefetch. (also reset buffer status) 1: Enable prefetch (4 words)	R/W	0B
21	*reserved*		R	0
20	D_SIGNAL	Disable DRAM signal (Masked) 0: All DRAM signals are enabled 1: All DRAM signals are disabled	R	0B (H/W Pin)
19	FLASH_MAP0_DIS	Disable flash memory mapping SPI Flash Region 1. 0: Enable flash memory mapping SPI Flash Region 1. 1: Disable flash memory mapping SPI Flash Region 1.Note: It latches the HW strap pin status during the memory controller initialization. After the initialization, it only shows the value of the software modification not the HW strap pin status.	R/W	0B (H/W Pin)
18	FLASH_MAP1_DIS	Disable flash memory mapping SPI Flash Region 2. 0: Enable flash memory mapping SPI Flash Region 2. 1: Disable flash memory mapping SPI Flash Region 2. Note: It is also runtime configurable. It is disabled by default.	R/W	1B
17:15	*must_be_zero*	All bits must be 0.	R	00000B
14	D_INIT_TRIG	Write 1 to trigger the DRAM initialization procedure. Read 1: The DRAM initialization procedure is still on going. 0: The DRAM initialization procedure is completed. Note: It is required to enable the TX clock output before the triggering of DRAM initialization procedure. TX clock output control is integrated outside the SOC HS0.	R/W	0B

Reg.bit	Name	Description	Mode	Default
13	OCP1/LX0_FRQ_SLOWER	Report whether the OCP1 clock < Memory clock. 0: OCP1/LX0 clock >= Memory clock 1: OCP1/LX0 clock < Memory clock. Note: It is required to setup this strap pin statically for the running environment to keep the integrity of the memory operations. We also need to set proper value by software before the (OCP1/LX1)/Memory frequencies changes on runtime.	R/W	0B (System H/W Pin)
12	LX1_FRQ_SLOWER	Report whether the LX1 clock < Memory clock. 0: LX1 clock >= Memory clock 1: LX1 clock < Memory clock. Note: It is required to setup this strap pin statically for the running environment to keep the integrity of the memory operations. We also need to set proper value by software before the LX1/Memory frequencies changes on runtime.	R/W	0B (System H/W Pin)
11	LX2_FRQ_SLOWER	Report whether the LX2 clock < Memory clock. 0: LX2 clock >= Memory clock 1: LX2 clock < Memory clock. Note: It is required to setup this strap pin statically for the running environment to keep the integrity of the memory operations. We also need to set proper value by software before the LX2/Memory frequencies changes on runtime.	R/W	0B (System H/W Pin)
10	LX3_FRQ_SLOWER	Report whether the LX3 clock < Memory clock. 0: LX3 clock >= Memory clock 1: LX3 clock < Memory clock. Note: It is required to setup this strap pin statically for the running environment to keep the integrity of the memory operations. We also need to set proper value by software before the LX3/Memory frequencies changes on runtime.	R/W	0B (System H/W Pin)
9	OCP0_FRQ_SLOWER	Report whether the OCP0 clock < Memory clock. 0: OCP0 clock >= Memory clock 1: OCP0 clock < Memory clock. Note: It is required to setup this strap pin statically for the running environment to keep the integrity of the memory operations. We also need to set proper value by software before the OCP0/Memory frequencies changes on runtime.	R/W	0B (System H/W Pin)
8:0	*reserved*			

2.8.2. DRAM Configuration Register (DCR) (0xB800_1004)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:30	*must_be_zero*	All bits must be 0.	R	00B

Reg.bit	Name	Description	Mode	Default
29:28	BANKCNT	Bank counts 00: 2 banks 01: 4 banks 10: 8 banks Others: reserved	R/W	1B
27:26	*must_be_zero*	All bits must be 0.	R	00B
25:24	DBUSWID	DRAM bus width 00: 8 bit 01: 16 bit 10: 32 bit 11: reserved	R/W	01B
23:20	ROWCNT	Row counts 0000: 2K (A0~A10) 0001: 4K (A0~A11) 0010: 8K (A0~A12) 0011: 16K (A0~A13) 0100: 32K (A0~A14) 0101: 64K (A0~A15) Others: reserved	R/W	00B
19:16	COLCNT	Column counts 0000: 256 (A0~A7) 0001: 512 (A0~A8) 0010: 1K (A0~A9) 0011: 2K (A0~A9, A11) 0100: 4K (A0~A9, A11, A12) others: reserved	R/W	000B
15	DCHIPSEL	DRAM chip select 0: CS0# 1: CS0# and CS1#	R/W	1B
14	FAST_RX	If RX path turnaround delay is small enough, memory controller can return read data with reduced latency by 1 memory clock cycle. 0: Normal path 1: Fast path	R/W	0B
13	BSTREF	Bursted 8 auto-refresh commands. 0: Disable 1: Enable	R/W	0B
12:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.3. DRAM Timing Register 0 (DTR0) (0xB800_1008)

(This register does not provide byte access)
(This register takes effect after DMCR is updated)

Reg.bit	Name	Description	Mode	Default
31:28	T_CAS	CAS Latency 0000: Latency=2.5 0001: Latency=2 0010: Latency=3 0011: Latency=4 0100: Latency=5 0101: Latency=6 0110: Latency=7 0111: Latency=8 1000: Latency=9 1001: Latency=10 1010: Latency=11 Others: Latency = 11	R/W	0010B
27:24	T_WR	tWR timing parameter of DRAM. Write recovery time. Basic unit = 1* DRAM_CLK 0000:1 DRAM_CLK 0001:2 DRAM_CLK 0010:3 DRAM_CLK 0011:4 DRAM_CLK 0100:5 DRAM_CLK 0101:6 DRAM_CLK 0110:7 DRAM_CLK 0111:8 DRAM_CLK Others: 8 DRAM_CLK Note: Updating the tWR parameter requires to set the corresponding WR field of the mode register.	R/W	0011B
23:20	T_CWL	CAS Write latency 0000: 1 * DRAM_CLK 0001: 2 * DRAM_CLK 0010: 3 * DRAM_CLK 0011: 4 * DRAM_CLK 0100: 5 * DRAM_CLK 0101: 6 * DRAM_CLK 0110: 7 * DRAM_CLK 0111: 8 * DRAM_CLK Others: 8 * DRAM_CLK	R/W	0000B
19:16	T_RTP	Read To Precharge Command Delay 0000: 1* DRAM_CLK 0001: 2* DRAM_CLK … 1111: 16* DRAM_CLK	R/W	1111B

Reg.bit	Name	Description	Mode	Default
15:12	T_WTR	Internal write to read command delay 0000: 1* DRAM_CLK 0001: 2* DRAM_CLK … 1111: 16* DRAM_CLK	R/W	1111B
11:8	T_REFI	tREF timing parameter of DRAM. Refresh row interval time. Basic unit = T_REFI_UNIT 0000: 1 unit 0001: 2 units … 1111: 16 units	R/W	0000B
7:4	T_REFI_UNIT	Basic unit of T_REFI 0000: 32 DRAM_CLK 0001: 64 DRAM_CLK 0010: 128 DRAM_CLK 0011: 256 DRAM_CLK 0100: 512 DRAM_CLK 0101: 1024 DRAM_CLK 0110: 2048 DRAM_CLK 0111: 4096 DRAM_CLK Others: reserved Note: The DRAM periodic refresh operation could be disable through setting DIS_DRAM_REF field of DMCR register with 1. It is required to make sure that the value of DIS_DRAM_REF field of DMCR register equals zero before the normal usage of DRAM.	R/W	0100B
3:0	*must_be_zero*	All bits must be 0.	R	0000B

2.8.4. DRAM Timing Register 1 (DTR1) (0xB800_100C)

(This register does not provide byte access)

(This register takes effect after DMCR is updated)

Reg.bit	Name	Description	Mode	Default
31:29	reserved			
28:24	T_RP	tRP timing parameter of DRAM . Basic unit = 1* DRAM_CLK 0000 means 1 unit … 11111 means 32 units	R/W	11111B
23:21	*must_be_zero*	All bits must be 0.	R	000B
20:16	T_RCD	tRCD timing parameter of DRAM . Basic unit = 1* DRAM_CLK 0000 means 1 unit … 11111 means 32 units	R/W	11111B
15:13	*must_be_zero*	All bits must be 0.	R	000B

Reg.bit	Name	Description	Mode	Default
12:8	T_RRD	Activate to activate (different bank) command period 0000: 1* DRAM_CLK … 11111: 32* DRAM_CLK	R/W	11111B
7:5	*must_be_zero*	All bits must be 0.	R	000B
4:0	T_FAWG	Four activate window gap 00000: 1* DRAM_CLK 11111: 32* DRAM_CLK	R/W	11111B

2.8.5. DRAM Timing Register 2 (DTR2) (0xB800_1010)

(This register does not provide byte access)

(This register takes effect after DMCR is updated)

Reg.bit	Name	Description	Mode	Default
31:28	*must_be_zero*	All bits must be 0.	R	000B
27:20	T_RFC	tRFC timing parameter of DRAM. Refresh row cycle time. 0000_0000 means 1 DRAM_CLK 0000_0001 means 2 DRAM_CLK … 1111_1111 means 256 DRAM_CLK	R/W	FFH
19:18	*must_be_zero*	All bits must be 0.	R	00B
17:12	T_RAS	Minimum T_RAS timing parameter of DRAM. Basic unit = 1* DRAM_CLK 00_0000 means 1 unit … 11_1111 means 64units	R/W	3FH
11:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.6. DRAM Mode Control Register (DMCR) (0xB800_101C)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	DTR_UP_BUSY/MRS_BUSY	Indicate whether the memory controller is progressing DTR parameters updating or DRAM Mode register setting. The updating progress starts after write request to DMCR register. The DRAM MRS command configured with MR_MODE and MR_DATA is issued by the memory controller when MR_MODE_EN == 1. 1: On going. 0: Ready/Complete	R	0B
30:25	*must_be_zero*	All bits must be 0.	R	000000B

Reg.bit	Name	Description	Mode	Default
24	DIS_DRAM_REF	Disable DRAM periodic DRAM refresh operation. 0: Enable the periodic DRAM refresh operation. 1: Disable the periodic DRAM refresh operation. Note: Sometimes it is necessary to disable the DRAM refresh operation when performing some DRAM operation (for example, it is required that it is required that 200 clock cycles idle after the DLL reset.)	R/W	0B
23:21	*must_be_zero*	All bits must be 0.	R	00B
20	MR_MODE_EN	Enable MR_MODE and MR_DATA fields in DMCR register. Set mode register command with MR_DATA is issued one time when this bit is asserted. 0: No issue MRS command. 1: Issue MRS command after updating this register.	R/W	0B
19:18	*must_be_zero*	All bits must be 0.	R	00B
17:16	MR_MODE	Select the memory command that memory controller issues. 00: Mode Register 01: Extended Mode Register (EMR(1)) 10: EMR(2) 11: EMR(3)	R/W	0B
15:14	*must_be_zero*	All bits must be 0.	R	00B
13:0	MR_DATA	Mode register data for setting mode register. (A13~A0) Set mode register command is issued after DCR is updated.	R/W	00000000 000000B

[Notes]

1. Write DMCR register always trigger DRAM Mode register set command. MR_MODE and MR_DATA are critical for writing DMCR. If wrong data are applied into MR_MODE and MR_DATA fields, the memory controller issues MRS command with wrong data and it will lead to system error.

2.8.7. Global Interface Arbitration Register 0 (GIAR0) (0xB800_1020)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	OCP_REQ	OCP request allocation of 32 rotating slots. 0 means "allocated" 1 means "not allocated"	R/W	10101010 10101010 10101010 10101010 or 0xAAAAAAAA

2.8.8. Global Interface Arbitration Register 1 (GIAR1) (0xB800_1024)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	LX_REQ	LX request allocation of 32 rotating slots. 0 means "allocated" 1 means "not allocated"	R/W	01010101 01010101 01010101 01010101 or 0x55555555

2.8.9. LX Interface Arbitration Register 0 (LXIAR0)/OCP1 Interface Arbitration Register (0xB800_1028)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	LX0_REQ	LX0 request allocation of 32 rotating slots. 0 means "allocated" 1 means "not allocated" Note: OCP1 interface share the allocated rotating slots configured with LX_REQ in GIAR1.	R/W	11101101 11101101 11101101 11101101 or 0xEDEDEDED

2.8.10. LX Interface Arbitration Register 1 (LXIAR1) (0xB800_102C)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	LX1_REQ	LX1 request allocation of 32 rotating slots. 0 means "allocated" 1 means "not allocated" Note: The width of LX1 bus is 32 bits.	R/W	10110111 10110111 10110111 10110111 or 0xB7B7B7B7

2.8.11. LX Interface Arbitration Register 2 (LXIAR2) (0xB800_1030)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	LX2_REQ	LX2 request allocation of 32 rotating slots. 0 means "allocated" 1 means "not allocated" Note: The width of LX2 bus is 32 bits.	R/W	11011110 11011110 11011110 11011110 or 0xDEDEDEDE

2.8.12. LX Interface Arbitration Register 3 (LXIAR3) (0xB800_1034)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	LX3_REQ	LX3 request allocation of 32 rotating slots. 0 means "allocated" 1 means "not allocated" Note: The width of LX3 bus is 64 bits.	R/W	01111011 01111011 01111011 01111011 or 0x7B7B7B7B

2.8.13. Memory Special Request Register (MSRR) (0xB800_1038)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	FLUSH_OCP_CMD	Request memory controller to serve all current pending OCP requests as an atomic operation which cannot be intervened by LX request. ● Write '1' to make the request. ● Read '0' if request is completed ● Read '1' if request is still on-going	WC	0B
30	DRAM_CMD_GOING	Indicate whether there is any ongoing DRAM command. It is valid for all supported DRAM types. (Target for software DRAM calibration or frequency change) 0: DRAM command is ongoing. 1: No ongoing command.	R	1B
29:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.14. Memory Power Management Register 0 (MPMR0) (0xB800_1040)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:30	reserved		R	00B
29:28	PM_MODE	00: normal 01: Enable automatic power down 10: Enable self refresh 11: reserved	R/W	0B
27:24	T_CKE	Clock Enable minimum high/low time. Basic unit = 1 * DRAM_CLK 0000: 1 unit 0001: 1 units 0010: 2 units … 1111: 16 units	R/W	1111B
23:22	*must_be_zero*	All bits must be 0.		00B

Reg.bit	Name	Description	Mode	Default
21:12	TRSD	10 bit threshold for counting up before activating power down or self refresh. Basic unit = 1* DRAM_CLK. 0: reserved 1: 2 units 2: 3 units … Maximum is 1023: 1024 units	R/W	1111111111B
11:10	*must_be_zero*	All bits must be 0.	R	00B
9:0	T_XSREF	tXSR timing parameter of SDR-DRAM. tXSRD timing parameter of DDR-DRAM. Basic unit = 1 * DRAM_CLK 0 means 1 unit, 1 means 2 units, and so forth. Maximum is 1024 units.	R/W	1111111111B

2.8.15. Memory Power Management Register 1(MPMR1) (0xB800_1044)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:28	T_XARD (2 cycles in spec) (2~3 cycles in Micron)	tXARD timing parameter of DDR2-DRAM. Basic unit = 1 * DRAM_CLK 0 means 1 unit, 1 means 2 units, and so forth. Maximum is 16 units.	R/W	1111B
27:24	T_AXPD (8 cycles in spec) (8~11 cycles in Micron)	tAXPD timing parameter of DDR2-DRAM. Basic unit = 1 * DRAM_CLK 0 means 1 unit, 1 means 2 units, and so forth. Maximum is 16 units.	R/W	1111B
23:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.16. DRAM internal DQS Enable Register (DIDER) (0xB800_1050)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	DQS0_EN_HCLK	When running in high speed clock, the incoming DQS signal might delay over 1/2 memory clock cycle for the reason of pad delay (1ns possible) etc. Therefore we might need delay the internal DQS enable window for DQs signals' integrity 0: Delay 0 memory clock cycle for internal DQS0 enable window. 1: Delay 1/2 memory clock cycle for Internal DQS0 enable window.	R/W	0B
30:29	*must_be_zero*	All bits must be 0.	R	000B

Reg.bit	Name	Description	Mode	Default
28:24	DQS0_EN_TAP[4:0]	Selection of 32 taps delay line for the internal DQS0_EN window. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap Note: 32 tap is around 5 ns, which is chosen to be a 200MHz clock cycle. So 1 tap is around 156.25 ps.	R/W	00000B
23	DQS1_EN_HCLK	When running in high speed clock, the incoming DQS signal might delay over 1/2 memory clock cycle for the reason of pad delay (1ns possible) etc. Therefore we might need delay the internal DQS enable window for DQs signals' integrity 0: Delay 0 memory clock cycle for Internal DQS0 enable window. 1: Delay 1/2 memory clock cycle for Internal DQS0 enable window.	R/W	0B
22:21	*must_be_zero*	All bits must be 0.	R	000B
20:16	DQS1_EN_TAP[4:0]	Selection of 32 taps delay line for the internal DQS1_EN window. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap Note: 32 tap is around 5 ns, which is chosen to be a 200MHz clock cycle. So 1 tap is around 156.25 ps.	R/W	00000B
15:0	*must_be_zero*	All bits must be 0.	R	0000H

2.8.17. DRAM Clock Delay Register (DCDR) (0xB800_1060)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:29	*must_be_zero*	All bits must be 0	R	000B

Reg.bit	Name	Description	Mode	Default
28:24	TX_DELAY	Selection of 32 taps delay line for TX clock. It is used to adjust setup time/hold time for output signals. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap Note: 32 tap is around 5 ns, which is chosen to be a 200MHz clock cycle. So 1 tap is around 156.25 ps. Note: The default value is chosen to be 01000B according to designer's suggestion. Increment of taps will gain more setup time margin, while decrement of taps will gain more hold time margin.	R/W	01000B
23:21	*must_be_zero*	All bits must be 0.	R	000B
20:16	RX_DELAY	Selection of 32 taps delay line for RX clock. It is used to adjust setup time/hold time for input signals. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap Note: 32 tap is around 5 ns, which is chosen to be a 200MHz clock cycle. So 1 tap is around 156.25 ps.	R/W	00000B
15:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.18. DDR2 DRAM OCD Control Register (D2OCR) (0xB800_1070)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	OCD_READY	OCD impedance adjust operation is done. Write 1 to trigger OCD impedance adjust program. DT0, DT1, DT2 and DT3 are defined in D2ODR1 and D2ODR2. 0: busy 1: ready	R/W	1B
30:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.19. DDR2 DRAM OCD Data Register0 (D2ODR0) (0xB800_1074)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:16	OCD_DT1	DT1 OCD impedance adjust mode program data for DQ0 ~ DQ15 pins. Bit 16 is for DQ0, bit 17 is for DQ1 … and so on.	R/W	0B
15:0	OCD_DT0	DT0 OCD impedance adjust mode program data for DQ0 ~ DQ15 pins. Bit 0 is for DQ0, bit 1 is for DQ1 … and so on.	R/W	0B

2.8.20. DDR2 DRAM OCD Data Register1 (D2ODR1) (0xB800_1078)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:16	OCD_DT3	DT3 OCD impedance adjust mode program data for DQ0 ~ DQ15 pins. Bit 16 is for DQ0, bit 17 is for DQ1 … and so on.	R/W	0B
15:0	OCD_DT2	DT2 OCD impedance adjust mode program data for DQ0 ~ DQ15 pins. Bit 0 is for DQ0, bit 1 is for DQ1 … and so on.	R/W	0B

2.8.21. DDR23 DRAM ODT Signal Control Register (D23OSCR) (0xB800107C)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	ODT_ALWAYS_ON	Force DDR2/3 SDRAM ODT high (enable DRAM ODT). 1: Force ODT signal high (enable DRAM ODT). 0: ODT signal is driven depending on the operation state of the memory controller.	R/W	0B
30	TE_ALWAYS_ON	Force the local termination to always be enabled. (IC side) 1: The local termination is always on. 0: The memory controller controls the on/off states of the local termination circuit.	R/W	0B
29:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.22. DDR3 DRAM ZQ Calibration Control Register (D3ZQCCR) (0xB800_1080)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	ZQ_LONG_TRI	Write 1 to trigger ZQ long calibration. Read value 1: The ZQ long calibration is still going on. 0: The ZQ long calibration is completed. Note: t_ZQoper is set to 1024 DRAM clocks.	R/W	0B

Reg.bit	Name	Description	Mode	Default
30	ZQ_SHORT_EN	Enable periodic ZQ short calibration. The ZQ short calibration is issued before the generation of the silence pattern, therefore it's also required to enable the silence generation (AC_SILEN_PERIOD_EN == 1). 1: Enable 0: Disable Note: The short calibration is set by T_ZQCS and it is updated when updating DMCR.	R/W	0B
29:23	*must_be_zero*	All bits must be 0.	R	000B
22:16	T_ZQCS	ZQ short calibration time Minimum T_ZQCS timing parameter of DDR3 SDRAM. Basic unit = 1 x DRAM_CLK 000_0000 means 1 unit … 111_1111 means 128 units. Note: T_ZQCS is updated when DMCR is updated.	R/W	7FH
15:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.23. DDR DRAM ZQ Pad Calibration Register (DDZQPR) (0xB800_1090)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	ZQ_PAD_FORCE_ON	Force the ZQ pad to be always enabled. 0: HW control when to power-on ZQ pad calibration module. 1: Force ZQ pad always power-on.	R/W	0B
30:29	*must_be_zero*	All bits must be 0.	R	00B
28	ZCTRL_CLK_SEL	Clock divide select: 0: divide the input clock by 8 1: divide the input clock by 16	R/W	1B
27:24	TRIM_MODE	1: Remain the result of the calibration value. 0: Reduce 1 to the result of the calibration value. TRIM_MODE [3] for ODTP TRIM_MODE [2] for ODTN TRIM_MODE [1] for OCDP TRIM_MODE [0] for OCDN	R/W	1111B
23:0	*must_be_zero*	All bits must be 0.	R	0B

2.8.24. DDR DRAM ZQ Pad Calibration Control Register (DDZQPCR) (0xB800_1094)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	ZCTRL_START	Start ZQ pad calibration Write 1 to trigger the calibration. Read value 0: ZQ pad calibration idle. 1: ZQ pad calibration busy. Note: It is required to confirm the idle status (ZCTRL_START==0) before trigger the ZQ pad calibration.	WC	0b
30:14	*must_be_zero*	All bits must be 0.	R	0b
13:0	ZPROG	Set auto-calibration target impedance value [13:7]: ODTP and ODTN target impedance -[13]: PLSB -[12:10]: PT[2:0] -[9]: E2 -[8]: E -[7]: vpcalen [6:0]: OCDP and OCDN target impedance -[6]: PLSB -[5:3]: PT[2:0] -[2]: E2 -[1]: E -[0]: vpcalen	R/W	0B

2.8.25. DDR DRAM ZQ Pad Calibration Status Register (DDZQPSR) (0xB800_1098)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	*must_be_zero*	All bits must be 0.	R	0b

Reg.bit	Name	Description	Mode	Default
30:0	ZCTRL_STATUS	Calibration status: auto calibration information [30]-impedance calibration done: When high, indicates that auto calibration has completed or over-ride data is ready. Become low after zctrl_start or zctrl_ovrd_en is de-asserted [29]-impedance calibration error: When high, indicates that there was an error during auto calibration. [28:27]-ODTP pull-up calibration status: 00=completed with no error 01=code overflow error (reach the maximum value) 10=code underflow error (reach the minimum value) 11=calibration in progress [26:25]-ODTN pull-down calibration status 00=completed with no error 01=code overflow error (reach the maximum value) 10=code underflow error (reach the minimum value) 11=calibration in progress [24:23]-OCDP pull-up calibration status 00=completed with no error 01=code overflow error (reach the maximum value) 10=code underflow error (reach the minimum value) 11=calibration in progress [22:21]-OCDN pull-down calibration status 00=completed with no error 01=code overflow error (reach the maximum value) 10=code underflow error (reach the minimum value) 11=calibration in progress [20:14]:ODT pull-up impedance [20:18]:TTFP [17:15]:TTCP [14]: PLSB[1] (for ODTP) [13:8]:ODT pull-down impedance [13:11]:TTFN [10:8]:TTCN [7:4]:OCD pull-up impedance [7:5]:PT [4]: PLSB[0] (for OCDP) [3:0]:OCD pull-down impedance [3:1]:NT [0]:E2	R	0B

2.8.26. SPI Flash Configuration Register (SFCR) (0xB800_1200)

This configuration register is used both for PIO (programmed I/O) and MMIO (memory mapped I/O).

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:29	SPI_CLK_DIV	SPI operating clock rate selection. The value defines the divisor to generate SPI clock SPI Clock = (DRAM Clock) / (SPI_CLK_DIV) 000 : DIV = 2 001 : DIV = 4 010 : DIV = 6 011 : DIV = 8 100 : DIV = 10 101 : DIV = 12 110 : DIV = 14 111 : DIV = 16	R/W (pio) (mmio)	111B
28	RBO	Serial Flash Read Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	R/W (pio) (mmio)	1B
27	WBO	Serial Flash Write Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	R/W (pio) (mmio)	1B
26:22	SPI_TCS	SPI chip deselect time. Basic unit = 1 * DRAM clock cycle 00000 means 1 unit, 00001 means 2 units, etc.	R/W (pio) (mmio)	11111B
21	DIV	Disable the divisor 0: Divisor is enabled 1: Divisor is disabled	R/W (pio) (mmio)	0B
20:19	*reserved*			
18:16	SPI_RX_DLY	SPI data sample delay control 000: no delay 001: delay 1 unit (1 unit = 1.4ns) 010: delay 2 unit 011: delay 3 unit 100: delay 4 unit 101: delay 5 unit 110: delay 6 unit 111: delay 7 unit	R/W (pio) (mmio)	000B
15:8	*reserved*			
7:4	SPI_TCHSH	SPI CS# active hold time (relative to SCLK) Basic unit = 1 * DRAM clock cycle 00000 means 1 unit, 00001 means 2 units, etc.	R/W (pio) (mmio)	0100B
3:0	SPI_TSLCH	SPI CS# active setup time. Basic unit = 1 * DRAM clock cycle 00000 means 1 unit, 00001 means 2 units, etc.	R/W (pio) (mmio)	0100B

[Notes]

1. When booting up from SPI flash, memory mapped I/O interface accesses through to SPI Region 1, SPI Region 2.
2. SFSIZE is only useful in memory mapped read mode.
   1. CS0# is asserted when 0 * SFSIZE <= memory address < 1 * SFSIZE
   2. CS1# is asserted when 1 * SFSIZE <= memory address < 2 * SFSIZE
   3. CS2# is asserted when 2 * SFSIZE <= memory address < 3 * SFSIZE
   4. CS3# is asserted when 3 * SFSIZE <= memory address < 4 * SFSIZE
   5. Memory address exceeding 4 * SFSIZE will wrap back, and still map to CS0# and CS1#.
3. When RD_OPT is turned on in memory mapped read mode, CS is manipulated by SPI flash controller and may be left either in selected state or deselected state. In order to ensure correct program I/O operation at a later time, write SPI_ENTER_PIO = 1 by software and check SPI_RDY prior to any program I/O operation. A CS toggle (deselected->selected->deselected) must be issued by software prior to any program I/O operation. This applies even when debugging with ICE.

2.8.27. SPI Flash Configuration Register 2 (SFCR2) (0xB800_1204)

This configuration register is only used for memory mapped I/O.

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:24	SFCMD	SPI flash 8-bit command code of a read transaction. Ex. "Read Data" is 0x03. "Fast Read" is 0x0B.	R/W (mmio)	0x03H
23:21	SFSIZE	SPI flash size. **3-Byte Mode:** 000: 128Kbyte 001: 256Kbyte 010: 512Kbyte 011: 1Mbyte 100: 2Mbyte 101: 4Mbyte 110: 8Mbyte 111: 16Mbyte **4-Byte Mode:** 000: 512Kbyte 001: 1Mbyte 010: 2Mbyte 011: 4Mbyte 100: 8Mbyte 101: 16Mbyte 110: 32Mbyte 111: Reserved	R/W (mmio)	111B
20	RDOPT	SPI Flash sequential access optimization. 0: No optimization 1: Optimization for sequential access	R/W (mmio)	0B

Reg.bit	Name	Description	Mode	Default
19:18	CMD_IO	SPI Flash I/O mode selection for the command phase of a read transaction 00: Serial I/O (8 cycles) 01: Dual I/O (4 cycles) 10: Quad I/O (2 cycles) 11: reserved	R/W (mmio)	00B
17:16	ADDR_IO	SPI Flash I/O mode selection for the address phase of a read transaction 00: Serial I/O (24 cycles) 01: Dual I/O (12 cycles) 10: Quad I/O (6 cycles) 11: reserved	R/W (mmio)	00B
15:13	DUMMY_CYCLES	SPI Flash inserted dummy cycles for the dummy cycle phase of a read transaction 000: 0 cycle 001: 2 cycles 010: 4 cycles 011: 6 cycles 100: 8 cycles 101: 10 cycles 110: 12 cycles 111: 14 cycles	R/W (mmio)	000B
12:11	DATA_IO	SPI Flash I/O mode selection for the data phase of a read transaction (assume 8*N cycles) 00: Serial I/O (8*N cycles) 01: Dual I/O (4*N cycles) 10: Quad I/O (2*N cycles) 11: reserved	R/W (mmio)	00B
10	HOLD_TILL_SFDR2	If this bit is '1', it indicates the write operation to this register (SFCR2) will not take effect immediately but will be delayed until another write operation to SFDR2.	R/W (mmio)	0B

2.8.28. SPI Flash Control&Status Register (SFCSR) (0xB800_1208)

This configuration register is used both for PIO (programmed I/O) and MMIO (memory mapped I/O).

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31	SPI_CSB0	SPI flash Chip select 0 (CS0#) 0 = active 1 = not active	R/W (PIO)	1B
30	SPI_CSB1	SPI flash Chip select 1 (CS1#) 0 = active 1 = not active	R/W (PIO)	1B

Bit	Name	Description	Mode	Default
29:28	LEN	SPI read/write data length (unit = byte) 00: 1 byte 01: 2 byte 10: 3 byte 11: 4 byte	R/W (PIO) (MMIO)	11B
27	SPI_RDY	SPI flash operation Busy indication flag 0: Busy (operation in progress) 1: Ready (idle or SPI access command is ready)	R (PIO)	1B
26:25	IO_WIDTH	SPI Flash I/O mode selection of a transaction. 00: Serial I/O 01: Dual I/O 10: Quad I/O 11: reserved	R/W (MMIO)	00B
24	CHIP_SEL	Chip selection 0: CS0# 1: CS1# (CS2#/CS3# is not supported)	R/W (MMIO)	0B
23:16	CMD_BYTE	SPI flash 8-bit command code of a transaction. (This field is only used in MMIO mode, when a) Ex. "Read Data" is 0x03. "Read ID" is 0x9F.	R/W (MMIO)	0B
15	SPI_CSB2	SPI flash Chip select 2 (CS2#) 0 = active 1 = not active	R/W (PIO)	1B
14	SPI_CSB3	SPI flash Chip select 3 (CS3#) 0 = active 1 = not active	R/W (PIO)	1B

[Notes]

1. Software must ensure SPI_RDY indicate Ready before selecting SPI flash and before doing read/write transactions.
2. When software executes in SPI flash only mode by utilizing memory mapped I/O interface, no programmed I/O is allowed in order to prevent unexpected results.

2.8.29. SPI Flash Data Register (SFDR) (0xB800_120C)

This configuration register is used for PIO (programmed I/O).

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/write data byte 3	R/W	0B
23:16	Data2	Read/write data byte 2	R/W	0B
15:8	Data1	Read/write data byte 1	R/W	0B
7:0	Data0	Read/write data byte 0	R/W	0B

[Notes]

1. If the RBO (Read Byte Ordering) or the WBO (Write Byte Ordering) fields of SFCR (SPI Flash Configuration Register) are from high to low, memory controller shall do read/write

byte access in the order {Data3, Data2, Data1, Data0}. If low to high, the byte access order is {Data0, Data1, Data2, and Data3}.

2.8.30. SPI Flash Data Register 2 (SFDR2) (0xB800_1210)

This configuration register is intended to be used under MMIO.

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/write data byte 3	R/W	0B
23:16	Data2	Read/write data byte 2	R/W	0B
15:8	Data1	Read/write data byte 1	R/W	0B
7:0	Data0	Read/write data byte 0	R/W	0B

[Notes]

1. If the RBO (Read Byte Ordering) or the WBO (Write Byte Ordering) fields of SFCR (SPI Flash Configuration Register) are from high to low, memory controller shall do read/write byte access in the order {Data3, Data2, Data1, Data0}. If low to high, the byte access order is {Data0, Data1, Data2, and Data3}.

2.8.31. SPI Flash RX Delay Control Register (SFRDCR) (0xB800_1214)

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31:0	must_be_zero	All bits must be zero.	R	0B

2.8.32. SPI Flash RX Delay Register 0 (SFRDR) (0xB800_1218)

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31:29	must_be_zero	All bits must be zero.	R	0B
28:24	IO3_Delay	Selection of 32 taps delay line for SPI flash RX IO3 delay. 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap	R/W	0B
23:21	Must_be_zero	All bits must be zero.	R	0B
20:16	IO2_Delay	Selection of 32 taps delay line for SPI flash RX IO2 delay. 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap	R/W	0B
15:13	must_be_zero	All bits must be zero.	R	0B

Bit	Name	Description	Mode	Default
12:8	IO1_Delay	Selection of 32 taps delay line for SPI flash RX IO1 delay. 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap	R/W	0B
7:5	must_be_zero	All bits must be zero.	R	0B
4:0	IO0_Delay	Selection of 32 taps delay line for SPI flash RX IO0 delay. 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap	R/W	0B

2.8.33. Unmapped Memory Segment Address Register 0 ~ 3 (UMSAR0 ~ UMSAR3) (0xB800_1300, 0xB800_1310, 0xB800_1320, 0xB800_1330)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	*reserved*		R	0
30:8	ADDR[30:8]	Starting physical address of the unmapped segment. ADDR[7:0] is always zero.	R/W	0
7:1	*reserved*		R	0B
0	EnUNMAP	Enable memory segment unmapping. 0: Disable 1: Enable	R/W	0B

2.8.34. Unmapped Memory Segment Size Register 0 ~ 3 (UMSSR0 ~ UMSSR3) (0xB800_1304, 0xB800_1314, 0xB800_1324, 0xB800_1334)

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31:4	*reserved*		R	0B

Bit	Name	Description	Mode	Default
3:0	SIZE	Set unmapped segment size. 0000: reserved 0001: 256 bytes 0010: 512 bytes 0011: 1K bytes 0100: 2K bytes 0101: 4K bytes 0110: 8K bytes 0111: 16K bytes 1000: 32K bytes 1001: 64K bytes 1010: 128K bytes 1011: 256K bytes 1100: 512K bytes 1101: 1M bytes 1110~1111: *reserved*	R/W	0B

[Notes]

1. Unmapped memory segment address registers and unmapped memory segment size registers are paired. That is, UMSAR0 and UMSSR0 is one pair, UMSAR1 and UMSSR1 is one pair, and etc.
2. The 4 pairs of registers reside in the memory controller and are intended to be used for unmapping SRAM segments. That is, the memory controller would not respond to address range specified by these registers.
3. The specified segment is unmapped only when the corresponding EnUNMAP bit is set.

2.8.35. DDR Auto-Calibration Configuration Register (DACCR)(0xB300_1500)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31	AC_MODE	Enable auto-calibration on DQS0 rising edge for DQ0. 1: Digital delay line 0: Analog DLL	R/W	1
30	DQS_SE	Enable Single-End DQS signaling 1: Singled DQS Signal 0: Differential DQS Signal Note: 1. If DRAMTYPE of MCR register == 000b(DDR1), DQS signal is forced to be Single-End. 2. If DRAMTYE of MCR register == 010b(DDR3), DQS signal is forced to be Differential. 3. Only when DRAMTYPE of MCR register == 0001(DDR2) is DQS_SE field configurable. 4. Software need to issue MRS command to change A10 "DQS# configuration" value of DDR2 SDRAM EMR(1) by writing DMCR register when applying change to this field.	R/W	0

Bit	Bit Name	Description	R/W	InitVal
29:21	*reserved*	All bits must be all zero.		0
20:16	DQS0_GROUP_TAP	Selection of the tap delay line number of the auto-calibration delay line window with DQS0 for DQ(0~7). 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap	R/W	0
15:13	*reserved*	All bits must be all zero.	R	0
12:8	DQS1_GROUP_TAP	Selection of the tap delay line number of the auto-calibration delay line window with DQS1 for DQ(8~15). 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap	R/W	0
7:6	*reserved*	All bits must be all zero.	R	0
5	AC_DYN_BPTR_CLR_EN	Enable dynamic DDR PHY FIFO buffer pointer reset. 0: Disable dynamic DDR PHY FIFO buffer pointer reset. 1: Enable dynamic DDR PHY FIFO buffer pointer reset.	R/W	0
4:0	*reserved*			

2.8.36. DDR Auto-Calibration Silence Pattern Control Register (DACSPCR) (0xB8001504)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31	AC_SILEN_PERIOD_EN	Enable auto-calibration silence pattern generation. In case of no DRAM traffic for a long period of time while the system environment changes. We need to generate read pattern automatically to adjust tap delay between DQs and DQSs. 1: Enable periodic silence pattern generation. 0: Disable periodic silence pattern generation. Note: ZQ short calibration is also issued before the generation of the silence pattern when the field ZQ_SHORT_EN of D3ZQCCR equals 1.	R/W	0
30~21	*reserved*	All bits must be all zero.	R	0

Bit	Bit Name	Description	R/W	InitVal
20	AC_SILEN_TRIG	Write 1 to trigger silence pattern generation one time. Read value: 1: The silence pattern generation hasn't completed yet. 0: It completes the silence pattern generation. Note: The DDR Auto-Calibration Silence Pattern Status Register is reset to 0 before the beginning of the silence pattern generation by the memory controller.	R/W	0
19:16	AC_SILEN_PERIOD_UNIT[3:0]	Basic unit of T_REFI 0000: 64 DRAM refresh cycles. 0001: 128 DRAM refresh cycles 0010: 256 DRAM refresh cycles 0011: 512 DRAM refresh cycles 0100: 1024 DRAM refresh cycles 0101: 2048 DRAM refresh cycles 0110: 4096 DRAM refresh cycles 0111: 8192 DRAM refresh cycles Others: reserved	R/W	0000
15~8	AC_SILEN_PERIOD[7:0]	The DRAM silence generation interval for auto-calibration. Basic unit = AC_SILEN_PERIOD_UNIT 00000000: 64 units. 00000001: 128 units. .... 11111111: 16384 units.. Note: The controller synchronizes this field to the control logic after updating DCR register. It is valid only when AC_SILEN_PERIOD_EN == 1.	R/W	0
7~0	AC_SILEN_LEN[7:0]	The number of 4byte double word to be read during the generation of the silence pattern. 00000000: 1 x 4 bytes. 00000001: 2 x 4 bytes. .... 11111111: 256 x 4 bytes. Note: In case of exceeding the limitation of refresh periods, the periodic silence pattern is generated after the DRAM refresh command.	R/W	0

2.8.37. DDR Auto-Calibration Silence Pattern Address Register. (DACSPAR) (0xB8001508)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31~0	AC_SILEN_ADDR[31:0]	The starting address of the silence pattern.	R/W	0

2.8.38. DDR Auto-Calibration Silence Pattern Status Register. (DACSPSR) (0xB800150C)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31	AC_SPS_DQ15R	Indication of the comparison among max. taps delay, current taps delay and min. taps delay. 0: If all the data values of DQ15 on falling of DQS1 latched with DQ15F_AC_MAX_TAP equals all the data values of DQ15 on falling of DQS1 latched with DQ15F_AC_MIN_TAP and all the data values of DQ15 on falling of DQS1 latched with DQ15F_AC_CUR_TAP. 1: Otherwise. Note: it is set to 0 before starting the silence pattern generation by the memory controller. It is valid only when AC_SILEN_MODE is set to trigger mode.	R	0
30	AC_SPS_DQ14R	Similar with AC_SPS_DQ15R	R	0
29	AC_SPS_DQ13R	Similar with AC_SPS_DQ15R	R	0
28	AC_SPS_DQ12R	Similar with AC_SPS_DQ15R	R	0
27	AC_SPS_DQ11R	Similar with AC_SPS_DQ15R	R	0
26	AC_SPS_DQ10R	Similar with AC_SPS_DQ15R	R	0
25	AC_SPS_DQ9R	Similar with AC_SPS_DQ15R	R	0
24	AC_SPS_DQ8R	Similar with AC_SPS_DQ15R	R	0
23	AC_SPS_DQ7R	Similar with AC_SPS_DQ15R	R	0
22	AC_SPS_DQ6R	Similar with AC_SPS_DQ15R	R	0
21	AC_SPS_DQ5R	Similar with AC_SPS_DQ15R	R	0
20	AC_SPS_DQ4R	Similar with AC_SPS_DQ15R	R	0
19	AC_SPS_DQ3R	Similar with AC_SPS_DQ15R	R	0
18	AC_SPS_DQ2R	Similar with AC_SPS_DQ15R	R	0
17	AC_SPS_DQ1R	Similar with AC_SPS_DQ15R	R	0
16	AC_SPS_DQ0R	Similar with AC_SPS_DQ15R	R	0
15	AC_SPS_DQ15F	Similar with AC_SPS_DQ15R	R	0
14	AC_SPS_DQ14F	Similar with AC_SPS_DQ15R	R	0
13	AC_SPS_DQ13F	Similar with AC_SPS_DQ15R	R	0
12	AC_SPS_DQ12F	Similar with AC_SPS_DQ15R	R	0
11	AC_SPS_DQ11F	Similar with AC_SPS_DQ15R	R	0
10	AC_SPS_DQ10F	Similar with AC_SPS_DQ15R	R	0

Bit	Bit Name	Description	R/W	InitVal
9	AC_SPS_DQ9F	Similar with AC_SPS_DQ15R	R	0
8	AC_SPS_DQ8F	Similar with AC_SPS_DQ15R	R	0
7	AC_SPS_DQ7F	Similar with AC_SPS_DQ15R	R	0
6	AC_SPS_DQ6F	Similar with AC_SPS_DQ15R	R	0
5	AC_SPS_DQ5F	Similar with AC_SPS_DQ15R	R	0
4	AC_SPS_DQ4F	Similar with AC_SPS_DQ15R	R	0
3	AC_SPS_DQ3F	Similar with AC_SPS_DQ15R	R	0
2	AC_SPS_DQ2F	Similar with AC_SPS_DQ15R	R	0
1	AC_SPS_DQ1F	Similar with AC_SPS_DQ15R	R	0
0	AC_SPS_DQ0F	Similar with AC_SPS_DQ15R	R	0

2.8.39. DDR Auto-Calibration for DQ(0~7/8~15) on the Rising edge of DQS(0/1) Register(DACDQ(0/8)RR~DACD(Q7/15)RR) (0xB8001510~0xB800152C/0xB8001530~0xB800154C)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31	DQ(0~7/8~15)R_AC_EN	Enable digital delay line auto-calibration on DQS(0/1) rising edge for DQ(0~7/8~15). 1: Enable. 0: Disable. Note: it's valid only when CALI_MODE equals Digital delay line mode.	R/W	0
30~29	*Reserved*	All bits must be all zero.	R	00
28~24	DQ(0~7/8~15)_PHASE_SHIFT_90[4:0]	Selection of 32 taps delay line for 90 degree phase shifted clock from the main clock for DQ(0~7/8~15). 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap Note: 40ps per tap	R/W	00000
23~21	*Reserved*	All bits must be all zero.	R	000
20~16	DQ(0~7/8~15)R_AC_MAX_TAP[4:0]	Selection of the maximum tap delay line number of the auto-calibration delay line window with DQS(0/1) rising edge for DQ(0~7/8~15). 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap Note: it's valid only when AC_MODE equals Digital delay line mode. 40ps per tap	R/W	11111
15~13	*Reserved*	All bits must be all zero.	R	000

Bit	Bit Name	Description	R/W	InitVal
12-8	DQ(0~7/8~15)R_AC_CUR_TAP[4:0]	Selection of the current using tap delay number of the auto-calibration with DQS(0/1) rising edge for DQ(0~7/8~15). When AC_MODE is digital delay line mode, it is the value of the current digital delay tap on DQS(0/1) rising edge for DQ(0~7/8~15). The value may change according to the variation of the environment after enabling DQ(0~7/8~15)R_AC_EN. If we disable DQ(0~7/8~15)R_AC_EN, the current delay tap value keeps the value it is set originally. If we set AC_MODE to be analog PLL mode, it keeps what it is set by using analog PLL adjustment for the delay tap. 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap Note: Digital delay line: 40ps per tap Analog DLL: 1/32 clock cycle per tap.	R/W	01111
7~5	*Reserved*	All bits must be all zero.	R	000
4~0	DQ(0~7/8~15)R_AC_MIN_TAP[4:0]	Selection of the minimum tap delay line number of the auto-calibration delay line window with DQS(0/1) rising edge for DQ(0~7/8~15). 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap Note: it's valid only when AC_MODE equals Digital delay line mode. 40ps per tap	R/W	00000

2.8.40. DDR Auto-Calibration for DQ(0~7/8~15) on the Falling edge of DQS(0/1) Register. (DACDQ(0/8)FR~DACD(Q7~15)RR) (0xB8001550~0xB800156C/0xB8001570~0xB800158C)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31	DQ(0~7/8~15)F_AC_EN	Enable digital delay line auto-calibration on DQS(0/1) falling edge for DQ(0~7/8~15). 1: Enable. 0: Disable. Note: it's valid only when CALI_MODE equals Digital delay line mode.	R/W	0
30~21	*Reserved*	All bits must be all zero.	R	0

Bit	Bit Name	Description	R/W	InitVal
20~16	DQ(0~7/8~15)F_AC_MAX_TAP[4:0]	Selection of the maximum tap delay line number of the auto-calibration delay line window with DQS(0/1) falling edge for DQ(0~7/8~15). 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap Note: it's valid only when AC_MODE equals Digital delay line mode. 40ps per tap	R/W	11111
13~15	*Reserved*	All bits must be all zero.	R	000
15-8	DQ(0~7/8~15)F_AC_CUR_TAP[4:0]	Selection of the current using tap delay number of the auto-calibration with DQS(0/1) falling edge for DQ(0~7/8~15). When CALI_MODE is digital delay line mode, it is the value of the current digital delay tap on DQS(0/1) falling edge for DQ(0~7/8~15). The value may change according to the variation of the environment after enabling DQ(0~7/8~15)R_AC_EN. If we disable DQ(0~7/8~15)R_AC_EN, the current delay tap value keeps the value it is set originally. If we set AC_MODE to be analog DLL mode, it keeps what it is set by using analog DLL adjustment for the delay tap. 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap Digital delay line: 40ps per tap Analog DLL: 1/32 clock cycle per tap.	R/W	01111
7~5	*Reserved*	All bits must be all zero.	R	000
4~0	DQ(0~7/8~15)F_AC_MIN_TAP[4:0]	Selection of the minimum tap delay line number of the auto-calibration delay line window with DQS(0/1) falling edge for DQ(0~7/8~15). 00000: 1st tap 00001: 2nd tap .... 11111:32nd tap Note: it's valid only when CALI_MODE equals Digital delay line mode. 40ps per tap	R/W	00000

2.8.41. DDR Calibration for DQM Register (DCDQMR)(0xB8001590)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31~29	*reserved*	All bits must be all zero.	R	00
28~24	DQM0_PHASE_SHIFT_90[4:0]	Selection of 32 taps delay line for 90 degree phase shifted clock from the main clock for DQM0.	R/W	00000
23~21	*Reserved*	All bits must be all zero.	R	000

Bit	Bit Name	Description	R/W	InitVal
20~16	DQM1_PHASE_SHIFT_90[4:0]	Selection of 32 taps delay line for 90 degree phase shifted clock from the main clock for DQM1.	R/W	00000
15~0	*Reserved*	All bits must be all zero.	R	0

2.8.42. DDR Calibration FIFO Data on Rising edge Register 0. (DCFDRR0)(0xB8001594)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31~28	DQ7R_FIFO_D[3:0]	4bit FIFO data of DQ7 signal latched with the delay tap setting of DQ7R_AC_CUR_TAP.	R	0000
27~24	DQ6R_FIFO_D[3:0]	4bit FIFO data of DQ6 signal latched with the delay tap setting of DQ6R_AC_CUR_TAP.	R	0000
23~20	DQ5R_FIFO_D[3:0]	4bit FIFO data of DQ5 signal latched with the delay tap setting of DQ5R_AC_CUR_TAP.	R	0000
19~16	DQ4R_FIFO_D[3:0]	4bit FIFO data of DQ4 signal latched with the delay tap setting of DQ4R_AC_CUR_TAP.	R	0000
15~12	DQ3R_FIFO_D[3:0]	4bit FIFO data of DQ3 signal latched with the delay tap setting of DQ3R_AC_CUR_TAP.	R	0000
11~8	DQ2R_FIFO_D[3:0]	4bit FIFO data of DQ2 signal latched with the delay tap setting of DQ2R_AC_CUR_TAP.	R	0000
7~4	DQ1R_FIFO_D[3:0]	4bit FIFO data of DQ1 signal latched with the delay tap setting of DQ1R_AC_CUR_TAP.	R	0000
3~0	DQ0R_FIFO_D[3:0]	4bit FIFO data of DQ0 signal latched with the delay tap setting of DQ0R_AC_CUR_TAP.	R	0000

2.8.43. DDR Calibration FIFO Data on Rising edge Register 1. (DCFDRR1)(0xB8001598)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31~28	DQ15R_FIFO_D[3:0]	4bit FIFO data of the DQ15 signal latched with the delay tap setting of DQ15R_AC_CUR_TAP.	R	0000
27~24	DQ14R_FIFO_D[3:0]	4bit FIFO data of DQ14 signal latched with the delay tap setting of DQ14R_AC_CUR_TAP.	R	0000
23~20	DQ13R_FIFO_D[3:0]	4bit FIFO data of DQ13 signal latched with the delay tap setting of DQ13R_AC_CUR_TAP.	R	0000
19~16	DQ12R_FIFO_D[3:0]	4bit FIFO data of DQ12 signal latched with the delay tap setting of DQ12R_AC_CUR_TAP.	R	0000
15~12	DQ11R_FIFO_D[3:0]	4bit FIFO data of DQ11 signal latched with the delay tap setting of DQ11R_AC_CUR_TAP.	R	0000
11~8	DQ10R_FIFO_D[3:0]	4bit FIFO data of DQ10 signal latched with the delay tap setting of DQ10R_AC_CUR_TAP.	R	0000
7~4	DQ9R_FIFO_D[3:0]	4bit FIFO data of DQ9 signal latched with the delay tap setting of DQ9R_AC_CUR_TAP.	R	0000
3~0	DQ8R_FIFO_D[3:0]	4bit FIFO data of DQ8 signal latched with the delay tap setting of DQ8R_AC_CUR_TAP.	R	0000

2.8.44. DDR Calibration FIFO Data on Falling edge Register 0. (DCFDFR0)(0xB800159C)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31~28	DQ7F_FIFO_D[3:0]	4bit FIFO data of DQ7 signal latched with the delay tap setting of DQ7F_AC_CUR_TAP.	R	0000
27~24	DQ6F_FIFO_D[3:0]	4bit FIFO data of DQ6 signal latched with the delay tap setting of DQ6F_AC_CUR_TAP.	R	0000
23~20	DQ5F_FIFO_D[3:0]	4bit FIFO data of DQ5 signal latched with the delay tap setting of DQ5F_AC_CUR_TAP.	R	0000
19~16	DQ4F_FIFO_D[3:0]	4bit FIFO data of DQ4 signal latched with the delay tap setting of DQ4F_AC_CUR_TAP.	R	0000
15~12	DQ3F_FIFO_D[3:0]	4bit FIFO data of DQ3 signal latched with the delay tap setting of DQ3F_AC_CUR_TAP.	R	0000
11~8	DQ2F_FIFO_D[3:0]	4bit FIFO data of DQ2 signal latched with the delay tap setting of DQ2F_AC_CUR_TAP.	R	0000
7~4	DQ1F_FIFO_D[3:0]	4bit FIFO data of DQ1 signal latched with the delay tap setting of DQ1F_AC_CUR_TAP.	R	0000
3~0	DQ0F_FIFO_D[3:0]	4bit FIFO data of DQ0 signal latched with the delay tap setting of DQ0F_AC_CUR_TAP.	R	0000

2.8.45. DDR Calibration FIFO Data on Falling edge Register 1. (DCFDFR1)(0xB80015A0)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31~28	DQ15F_FIFO_D[3:0]	4bit FIFO data of the DQ15 signal latched with the delay tap setting of DQ15F_AC_CUR_TAP.	R	0000
27~24	DQ14F_FIFO_D[3:0]	4bit FIFO data of DQ14 signal latched with the delay tap setting of DQ14F_AC_CUR_TAP.	R	0000
23~20	DQ13F_FIFO_D[3:0]	4bit FIFO data of DQ13 signal latched with the delay tap setting of DQ13F_AC_CUR_TAP.	R	0000
19~16	DQ12F_FIFO_D[3:0]	4bit FIFO data of DQ12 signal latched with the delay tap setting of DQ12F_AC_CUR_TAP.	R	0000
15~12	DQ11F_FIFO_D[3:0]	4bit FIFO data of DQ11 signal latched with the delay tap setting of DQ11F_AC_CUR_TAP.	R	0000
11~8	DQ10F_FIFO_D[3:0]	4bit FIFO data of DQ10 signal latched with the delay tap setting of DQ10F_AC_CUR_TAP.	R	0000
7~4	DQ9F_FIFO_D[3:0]	4bit FIFO data of DQ9 signal latched with the delay tap setting of DQ9F_AC_CUR_TAP.	R	0000
3~0	DQ8F_FIFO_D[3:0]	4bit FIFO data of DQ8 signal latched with the delay tap setting of DQ8F_AC_CUR_TAP.	R	0000

2.8.46. DDR Calibration FIFO Data Debug Control Register. (DCFDDCR)(0xB80015A4)

(This register does not provide byte access)

Bit	Bit Name	Description	R/W	InitVal
31	FIFO_D_DEBUG_EN	Enable DDR Calibration FIFO buffer pointer data debugging. We should enable this bit before reading DCFDRR0/1 and DCFDFR0/1. 0: Disable 1: Enable	R	0000
30~1	*Reserved*	All bits must be all zero.	R	0
0	FIFO_D_SEL	This bit is used to select odd or even DDR calibration FIFO buffer data to be shown in DCFDRR0/1 and DCFDFR0/1 when we enable dynamic FIFO buffer pointer reset function. Note: When we disable dynamic FIFO buffer pointer reset (AC_DYN_BPTR_CLR_EN field in DACCR), it always shows the even FIFO buffer data in DCFDRR0/1 and DCFDFR0/1 registers. 0: Select even FIFO buffer. 1: Select odd FIFO buffer.	R	0000

2.8.47. Memory Cache Control&Configuration Register (MCCCR) (0xB800_1600)

(This register does not provide byte access)

Reg .bit	Name	Description	Mode	Default
31	ENABLE	Enable memory cache function 0: disable 1: enable	R/W	0B
30:28	CACHE_SRC	Cached Source Memory Type 000: SPI Flash Memory others: reserved	RW	000B
27:1	must_be_zero			
0	INVALIDATE	Invalidate all cache lines Write 1 to invalidate all cache lines	WC	0B

2.8.48. Memory Cache Base Address Register (MCBAR) (0xB800_1604)

(This register does not provide byte access)

Reg. bit	Name	Description	Mode	Default
31:0	MC_BADR	Cached base address	R/W	1FC0_0000H

[Notes]

1. The MC_BADR must align to cache line size. In 16 bytes line size configuration, the bit[3:0] is ignored.
2. The MC_BADR is physical address.

2.8.49. Memory Cache Mask Register (MCMR) (0xB800_1608)

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31:0	MC_MADR	Cached address mask	R/W	FFFE_0000H

[Notes]

1. If (RequestAddress&MC_MADR) == (MC_BADR&MC_MADR) then RequestAddress is in cacheable address.

2.8.50. Memory Cache Debug Control&Status Register (MCDCSR) (0xB800_160C)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	TRIGGER	Perform debug operation from MCDDR0/1	W	0B
30:25	TAG_INDEX	Tag index	R/W	000000B
24:19	DW_INDEX	Double word index	R/W	000000B
18:16	MODE	Debug operation 000: read cache data, tag, valid bit 001: write cache data, tag, valid bit	R/W	000B

2.8.51. Memory Cache Debug DATA Register0 (MCDDR0) (0xB800_1610)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:1	TAG	Tag value	R/W	0
0	DW_VALID	DW valid bit	R/W	0B

2.8.52. Memory Cache Debug DATA Register1 (MCDDR1) (0xB800_1614)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	DW_DATA	DW data	R/W	0

2.8.53. DRAM Offset Register of Zone 0 (DOR0) (0xB800_1700)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	*reserved*		R	0
30:20	OFFSET[30:20]	The address offset when CPU accesses the DRAM for logical address zone 0, which is between 0x0000_0000 and 0x0fff_ffff. The unit to offset is in Mega byte.	R/W	0
19:0	*reserved*		R	0

2.8.54. DRAM Maximal Address Register of Zone 0 (DMAR0) (0xB800_1704)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:28	*reserved*		R	0
27:20	MAX[27:20]	The maximal logical address of zone 0 for CPU. MAX[19:0]=0xFFFFF. When MAX[27:20] = 0xFF, it means the maximal logical address of zone 0 is 0x0FFF_FFFF.	R/W	0
19:0	*reserved*		R	0xFFFFF

2.8.55. DRAM Offset Register of Zone 2 (DOR2) (0xB800_1720)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	*reserved*		R	0
30:20	OFFSET[30:20]	The address offset when CPU accesses the DRAM for logical address zone 2, which is between 0x2000_0000 and 0x7fff_ffff. The unit to offset is in Mega byte.	R/W	0
19:0	*reserved*		R	0

2.8.56. DRAM Maximal Address Register of Zone 2 (DMAR2) (0xB800_1724)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	*reserved*		R	0
30:20	MAX[30:20]	The maximal logical address of zone 2 for CPU. MAX[19:0] is always 0xFFFFF.	R/W	0
19:0	*reserved*		R	0xFFFFF

2.8.57. Processor Range Control Register (PRCR) (0xB800_1730)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:2	*reserved*		R	0
1:0	RCR	CPU Range Control Register bit 0: ARCE bit 1: ILA_VALID	R/W	0

2.8.58. Processor Illegal Logical Address Register (PILAR) (0xB800_1734)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:0	ILA	The illegal logical address issued by CPU.	R/W	0

2.8.59. SRAM Segment Address Register 0 ~ 3 (SRAMSAR0 ~ SRAMSAR3) (0xB800_4000, 0xB800_4010, 0xB800_4020, 0xB800_4030)

(This register does not provide byte access)

Reg.bit	Name		Description	Mode	Default
31:8	LX_SA[31:8]		The starting address of this segment on LX bus.	R/W	0
	OCP_SA [31:8]	LA_MATCH [31]	When this bit is 1, the starting address of the segment on the OCP will be compared by its logical address and OCP_ADDR stores the logical address. Otherwise, the starting address on the OCP will be compared by its physical address and OCP_ADDR store the physical address.		
		OCP_ADDR [30:8]	The starting address of the segment on the OCP. OCP_ADDR[7:0] is always zero. OCP_ADDR should be an integral multiple of the segment size.		
7:1	*reserved*			R	0B
0	EnSRAM		Enable SRAM segment function. 0: Disable 1: Enable	R/W	0B

[Notes]

1. The case of LA_MATCH = 1 is designed only to map a SRAM segment to 0x1000_0000~0x1FFF_FFFF. Because the range has no zone translation, the LA is the only address the SRAM controller has. (SRAM controller has no idea about Zone 1).

2.8.60. SRAM Segment Size Register 0 ~ 3 (SRAMSSR0 ~ SRAMSSR3) (0xB800_4004, 0xB800_4014, 0xB800_4024, 0xB800_4034)

(This register does not provide byte access)

Bit	Name	Description	Mode	Default
31:4	*reserved*		R	0B
3:0	SIZE	Set SRAM segment size. 0000: *reserved* 0001: 256 bytes 0010: 512 bytes 0011: 1K bytes 0100: 2K bytes 0101: 4K bytes 0110: 8K bytes 0111: 16K bytes 1000: 32K bytes 1001: 64K bytes 1010: 128K bytes 1011~1111: *reserved*	R/W	0B

2.8.61. SRAM Segment Base Register 0 ~ 3 (SRAMSBR0 ~ SRAMSBR3) (0xB800_4008, 0xB800_4018, 0xB800_4028, 0xB800_4038)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31:16	*reserved*		R	0B
15:8	BASE[15:8]	BASE[7:0] is always 0. BASE[15:0] should be the integral multiple of the segment size.	R/W	0B
7:0	*reserved*		R	0B

[Notes]

1. SRAM segment address registers, SRAM segment size registers and SRAM segment base registers are grouped. That is, SRAMSAR0, SRAMSSR0 and SRAMSBR0 are one group; SRAMSAR1, SRAMSSR1 and SRAMSBR1 are one group, and etc. Four groups are supported, and therefore there are as many as four SRAM segments.
2. When either one of SRAM segment's EnSRAM bit is enabled, the SRAM controller will respond to read/write accesses within the specified segment's address range. For example, SRAMSAR0 == 0x0100_0001 and SRAMSSR0 == means segment 0 is 4KB and it maps to memory address 0x0100_0000. Therefore the SRAM controller will respond to requests ranged from 0x0100_0000 to 0x0100_0FFF. Also SRAMSBR0 equal to 0x0000_2000 means segment 0 occupies 8K ~ (12K-1) from the 32KB SRAM.
3. SRAM segments may fall within the decoding range of the memory controller, like DRAM Region, SPI Region 1, NOR Region 2 and etc. This will lead to multiple responses from

different OCP slaves. In order to avoid such case from happening, the memory controller shall provide software with corresponding registers to unmap SRAM segments. This is the reason Unmapped Memory Segment Address Register and Unmapped Memory Segment Size Register come to exist.

4. It is prohibited that the SRAM segment overlaps with regions that already belong to other OCP slaves. For example, 0x1800_0000 shall not be mapped to by SRAM segments since the range would overlap with memory controller registers such as MCR, DCR and etc. Also to be noted is that segments shall be discrete, that is, one segment shall not overlap with one another.

2.8.62. DRAM Offset Register of Zone 0 Mapping in SRAM (DORS0) (0xB800_4090)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	*reserved*		R	0
30:20	OFFSET[30:20]	The address offset when CPU accesses the DRAM for logical address zone 0, which is between 0x0000_0000 and 0x0fff_ffff. The unit to offset is in Mega byte.	R/W	0
19:0	*reserved*		R	0

2.8.63. DRAM Offset Register of Zone 2 Mapping in SRAM (DORS2) (0xB800_4094)

(This register does not provide byte access)

Reg.bit	Name	Description	Mode	Default
31	*reserved*		R	0
30:20	OFFSET[30:20]	The address offset when CPU accesses the DRAM for logical address zone 2, which is between 0x2000_0000 and 0x7fff_ffff. The unit to offset is in Mega byte.	R/W	0
19:0	*reserved*		R	0

3. RTL8390 Peripherals Specification

3.1. UART

3.1.1. Features

The RTL8390 provides two 16C550 compatible UARTs, and each one contains a 16-byte First In First Out (FIFO) buffer. In addition, auto flow control is provided, in which auto-CTS mode (CTS controls transmission) and auto-RTS mode (Receiver FIFO contents and threshold control RTS) are both supported. The baud rate can be up to 115200bps and a programmable baud rate generator allows division of any input reference clock by 1 to (2^16-1) and generates an internal 16x clock. The RTL8390 provides a fully programmable serial interface that can be configured to support 6, 7, or 8 bit characters, even, odd, no parity generation and detection, and 1 or 2 stop bit generation. Fully prioritized interrupt control and loopback functionality for diagnostic capability are also provided.

3.1.2. Interface Pins

The UART interface pins are shown in the following table. (Note: RTL8390 supports 2 UART interfaces)

Table. UART Control Interface Pins

Signal Name	Type	Function
TXD#	O	Transmit Data.
RXD#	I	Receive Data.
RTS#	O	Request To Send.
CTS#	I	Clear To Send.

3.1.3. Register Set (Base Address: 0xB800_2000)

Table. UART Control Register Set

Offset	Size (byte)	Name	Description	Access
000	1	UART0_RBR	Receiver buffer register (DLAB=0).	R
000	1	UART0_THR	Transmitter holding register (DLAB=0).	W
000	1	UART0_DLL	Divisor latch LSB (DLAB=1).	R/W
004	1	UART0_IER	Interrupt enable register (DLAB=0).	R/W
004	1	UART0_DLM	Divisor latch MSB (DLAB=1).	R/W
008	1	UART0_IIR	Interrupt identification register.	R
008	1	UART0_FCR	FIFO control register.	W
00c	1	UART0_LCR	Line control register.	R/W
010	1	UART0_MCR	Modem control register.	R/W
014	1	UART0_LSR	Line status register.	R/W
018	1	UART0_MSR	Modem status register.	R/W
01c	1	UART0_SCR	Scratch register.	R/W
100	1	UART1_RBR	Receiver buffer register (DLAB=0).	R

Offset	Size (byte)	Name	Description	Access
100	1	UART1_THR	Transmitter holding register (DLAB=0).	W
100	1	UART1_DLL	Divisor latch LSB (DLAB=1).	R/W
104	1	UART1_IER	Interrupt enable register (DLAB=0).	R/W
104	1	UART1_DLM	Divisor latch MSB (DLAB=1).	R/W
108	1	UART1_IIR	Interrupt identification register.	R
108	1	UART1_FCR	FIFO control register.	W
10c	1	UART1_LCR	Line control register.	R/W
110	1	UART1_MCR	Modem control register.	R/W
114	1	UART1_LSR	Line status register.	R/W
118	1	UART1_MSR	Modem status register.	R/W
11c	1	UART1_SCR	Scratch register.	R/W

3.1.4. UART0 Receiver Buffer Register (DLAB=0) (UART0_RBR) (0xB800_2000)

Table. UART Receiver Buffer Register (DLAB=0)

Bit	Bit Name	Description	R/W	InitVal
31:24	RBR[7:0]	Receiver buffer data.	R	00H

3.1.5. UART0 Transmitter Holding Register (DLAB=0) (UART0_THR) (0xB800_2000)

Table. UART Transmitter Holding Register (DLAB=0)

Bit	Bit Name	Description	R/W	InitVal
31:24	THR[7:0]	Transmitter holding data.	W	00H

3.1.6. UART0 Divisor Latch LSB (DLAB=1) (UART0_DLL) (0xB800_2000)

Table. UART Divisor Latch LSB (DLAB=1)

Bit	Bit Name	Description	R/W	InitVal
31:24	DLL[7:0]	Divisor latch LSB.	W/R	00H

3.1.7. UART0 Divisor Latch MSB (DLAB=1) (UART0_DLM) (0xB800_2004)

Table. UART Divisor Latch MSB (DLAB=1)

Bit	Bit Name	Description	R/W	InitVal
31:24	DLM[7:0]	Divisor latch MSB.	W/R	00H

3.1.8. UART0 Interrupt Enable Register (DLAB=0) (UART0_IER) (0xB800_2004)

Table. UART Interrupt Enable Register

Bit	Bit Name	Description	R/W	InitVal
24	ERBI	Enable received data available interrupt.	R/W	0
25	ETBEI	Enable transmitter holding register empty interrupt.	R/W	0
26	ELSI	Enable receiver line status interrupt.	R/W	0
27	EDSSI	Enable modem status register interrupt.	R/W	0
28	ESLP	Sleep mode enable.	R/W	0
29	ELP	Low power mode enable.	R/W	0
31:30		Reserved.		00

3.1.9. UART0 Interrupt Identification Register (UART0_IIR) (0xB800_2008)

Table. UART Interrupt Identification Register

Bit	Bit Name	Description	R/W	InitVal
24	IPND	Interrupt pending. 0=Interrupt pending	R	1
27:25	IID[2:0]	Interrupt ID. IID[1:0] indicates the interrupt priority.	R	000
29:28		Reserved.	R	00
31:30	FIFO16[1:0]	00=No FIFO 11=16-byte FIFO	R	11

3.1.10. UART0 FIFO Control Register (UART0_FCR) (0xB800_2008)

Table. UART FIFO Control Register

Bit	Bit Name	Description	R/W	InitVal
24	EFIFO	Enable FIFO. When this bit is set, enables the transmitter and receiver FIFOs. Changing this bit clears the FIFOs.	W	0
25	RFRST	Receiver FIFO Reset. Writes 1 to clear the receiver FIFO.	W	0
26	TFRST	Transmitter FIFO Reset. Writes 1 to clear the transmitter FIFO.	W	0
27	Reserved	Reserved. Should be '0'.		0
29:28		Reserved		00
31:30	RTRG[1:0]	Receiver Trigger level. Trigger level: 16-byte 00=01, 01=04, 10=08, 11=14	W	11

3.1.11. UART0 Line Control Register (UART0_LCR) (0xB800_200C)

Table. UART Line Control Register

Bit	Bit Name	Description	R/W	InitVal
25:24	WLS[1:0]	Word Length Select. 00=Reserved 01=6 bits 10=7 bits 11=8 bits	R/W	11
26	STB	Number of Stop Bits. 0=1 bit 1=2 bits	R/W	0
27	PEN	Parity Enable.	R/W	0
29:28	EPS[1:0]	Even Parity Select. 00=odd parity 01=even parity 10=mark parity 11=space parity	R/W	0
30	BRK	Break control. Set this bit force TXD to the spacing (low) state (break). Clear this bit to disable break condition.	R/W	0
31	DLAB	Divisor Latch Access Bit.	R/W	0

3.1.12. UART0 Modem Control Register (UART0_MCR) (0xB800_2010)

Table. UART Modem Control Register

Bit	Bit Name	Description	R/W	InitVal
24	DTR	Data Terminal Ready. 0=Set DTR# high 1=Set DTR# low	R/W	0
25	RTS	Request To Send. 0=Set RTS# high 1=Set RTS# low	R/W	0
26	OUT1	Out 1	R/W	0
27	OUT2	Out 2	R/W	0
28	LOOP	Loopback	R/W	0
29	AFE	Auto Flow control Enable	R/W	0

3.1.13. UART0 Line Status Register (UART0_LSR) (0xB800_2014)

Table. UART Line Status Register

Bit	Bit Name	Description	R/W	InitVal
24	DR	Data Ready. Character mode: Data ready in RBR FIFO mode: Receiver FIFO is not empty.	RC	0
25	OE	Overrun Error. An overrun occurs when the receiver FIFO is full and the next character is completely received in the receiver shift register. An OE is indicated. The character in the shift register will be overwritten.	R	0
26	PE	Parity Error.	R	0
27	FE	Framing Error.	R	0
28	BI	Break Interrupt indicator.	R	0
29	THRE	Transmitter Holding Register Empty. Character mode: THR is empty FIFO mode: Transmitter FIFO is empty	R	1
30	TEMT	Transmitter Empty. Character mode: Both THR and TSR are empty. FIFO mode: Both transmitter FIFO and TSR are empty	R	1
31	RFE	Receiver FIFO Error. Either a parity, framing, or break error in the FIFO.	R	0

3.1.14. UART0 Modem Status Register (UART0_MSR) (0xB800_2018)

Table. UART Modem Status Register

Bit	Bit Name	Description	R/W	InitVal
31	ΔCTS	Delta clear to send. CTS# signal transmits.	R	0
30	ΔDSR	Delta data set ready. DSR# signal transmits. Returns 0.	R	0
29	TERI	Trailing edge ring indicator. RI# signal changes from low to high. Returns 0.	R	0
28	ΔDCD	Delta data carrier detect. DCD# signal transmits. Returns 0.	R	1
27	CTS	Clear To Send. 0=CTS# detected high 1=CTS# detected low	R	0

26	DSR	Data Set Ready.
		0=DSR # detected high
		1=DSR# detected low
		In loopback mode, returns bit 0 of MCR
		In normal mode, returns 1.
			R	0

Bit	Bit Name	Description	R/W	InitVal
25	RI	Ring Indicator. 0=RI# detected high 1=RI# detected low In loopback mode, returns bit 3 of MCR. In normal mode, returns 0.	R	0
24	DCD	Data Carrier Detect. 0=DCD# detected high 1=DCD# detected low In loopback mode, returns bit 2 of MCR. In normal mode, returns 1.	R	0

3.1.15. UART1 Receiver Buffer Register (DLAB=0) (UART1_RBR) (0xB800_2100)

Table. UART Receiver Buffer Register (DLAB=0)

Bit	Bit Name	Description	R/W	InitVal
31:24	RBR[7:0]	Receiver buffer data.	R	00H

3.1.16. UART1 Transmitter Holding Register (DLAB=0) (UART1_THR) (0xB800_2100)

Table. UART Transmitter Holding Register (DLAB=0)

Bit	Bit Name	Description	R/W	InitVal
31:24	THR[7:0]	Transmitter holding data.	W	00H

3.1.17. UART1 Divisor Latch LSB (DLAB=1) (UART1_DLL) (0xB800_2100)

Table. UART Divisor Latch LSB (DLAB=1)

Bit	Bit Name	Description	R/W	InitVal
31:24	DLL[7:0]	Divisor latch LSB.	W/R	00H

3.1.18. UART1 Divisor Latch MSB (DLAB=1) (UART1_DLM) (0xB800_2104)

Table. UART Divisor Latch MSB (DLAB=1)

Bit	Bit Name	Description	R/W	InitVal
31:24	DLM[7:0]	Divisor latch MSB.	W/R	00H

3.1.19. UART1 Interrupt Enable Register (DLAB=0) (UART1_IER) (0xB800_2104)

Table. UART Interrupt Enable Register

Bit	Bit Name	Description	R/W	InitVal
24	ERBI	Enable received data available interrupt.	R/W	0
25	ETBEI	Enable transmitter holding register empty interrupt.	R/W	0
26	ELSI	Enable receiver line status interrupt.	R/W	0
27	EDSSI	Enable modem status register interrupt.	R/W	0
28	ESLP	Sleep mode enable.	R/W	0
29	ELP	Low power mode enable.	R/W	0
31:30		Reserved.		00

3.1.20. UART1 Interrupt Identification Register (UART1_IIR) (0xB800_2108)

Table. UART Interrupt Identification Register

Bit	Bit Name	Description	R/W	InitVal
24	IPND	Interrupt pending. 0=Interrupt pending	R	1
27:25	IID[2:0]	Interrupt ID. IID[1:0] indicates the interrupt priority.	R	000
29:28		Reserved.	R	00
31:30	FIFO16[1:0]	00=No FIFO 11=16-byte FIFO	R	11

3.1.21. UART1 FIFO Control Register (UART1_FCR) (0xB800_2108)

Table. UART FIFO Control Register

Bit	Bit Name	Description	R/W	InitVal
24	EFIFO	Enable FIFO. When this bit is set, enables the transmitter and receiver FIFOs. Changing this bit clears the FIFOs.	W	0
25	RFRST	Receiver FIFO Reset. Writes 1 to clear the receiver FIFO.	W	0
26	TFRST	Transmitter FIFO Reset. Writes 1 to clear the transmitter FIFO.	W	0
27	Reserved	Reserved. Should be '0'.		0
29:28		Reserved		00
31:30	RTRG[1:0]	Receiver Trigger level. Trigger level: 16-byte 00=01, 01=04, 10=08, 11=14	W	11

3.1.22. UART1 Line Control Register (UART1_LCR) (0xB800_210C)

Table. UART Line Control Register

Bit	Bit Name	Description	R/W	InitVal
25:24	WLS[1:0]	Word Length Select. 00=Reserved 01=6 bits 10=7 bits 11=8 bits	R/W	11
26	STB	Number of Stop Bits. 0=1 bit 1=2 bits	R/W	0
27	PEN	Parity Enable.	R/W	0
29:28	EPS[1:0]	Even Parity Select. 00=odd parity 01=even parity 10=mark parity 11=space parity	R/W	0
30	BRK	Break control. Set this bit force TXD to the spacing (low) state (break). Clear this bit to disable break condition.	R/W	0
31	DLAB	Divisor Latch Access Bit.	R/W	0

3.1.23. UART1 Modem Control Register (UART1_MCR) (0xB800_2110)

Table. UART Modem Control Register

Bit	Bit Name	Description	R/W	InitVal
24	DTR	Data Terminal Ready. 0=Set DTR# high 1=Set DTR# low	R/W	0
25	RTS	Request To Send. 0=Set RTS# high 1=Set RTS# low	R/W	0
26	OUT1	Out 1	R/W	0
27	OUT2	Out 2	R/W	0
28	LOOP	Loopback	R/W	0
29	AFE	Auto Flow control Enable	R/W	0

3.1.24. UART1 Line Status Register (UART1_LSR) (0xB800_2114)

Table. UART Line Status Register

Bit	Bit Name	Description	R/W	InitVal
24	DR	Data Ready. Character mode: Data ready in RBR FIFO mode: Receiver FIFO is not empty.	RC	0

Bit	Bit Name	Description	R/W	InitVal
25	OE	Overrun Error. An overrun occurs when the receiver FIFO is full and the next character is completely received in the receiver shift register. An OE is indicated. The character in the shift register will be overwritten.	R	0
26	PE	Parity Error.	R	0
27	FE	Framing Error.	R	0
28	BI	Break Interrupt indicator.	R	0
29	THRE	Transmitter Holding Register Empty. Character mode: THR is empty FIFO mode: Transmitter FIFO is empty	R	1
30	TEMT	Transmitter Empty. Character mode: Both THR and TSR are empty. FIFO mode: Both transmitter FIFO and TSR are empty	R	1
31	RFE	Receiver FIFO Error. Either a parity, framing, or break error in the FIFO.	R	0

3.1.25. UART1 Modem Status Register (UART1_MSR) (0xB800_2118)

Table. UART Modem Status Register

Bit	Bit Name	Description	R/W	InitVal
31	ΔCTS	Delta clear to send. CTS# signal transmits.	R	0
30	ΔDSR	Delta data set ready. DSR# signal transmits. Returns 0.	R	0
29	TERI	Trailing edge ring indicator. RI# signal changes from low to high. Returns 0.	R	0
28	ΔDCD	Delta data carrier detect. DCD# signal transmits. Returns 0.	R	1
27	CTS	Clear To Send. 0=CTS# detected high 1=CTS# detected low	R	0

26	DSR	Data Set Ready.
		0=DSR # detected high
		1=DSR# detected low
		In loopback mode, returns bit 0 of MCR
		In normal mode, returns 1.
			R	0

25	RI	Ring Indicator. 0=RI# detected high 1=RI# detected low In loopback mode, returns bit 3 of MCR. In normal mode, returns 0.	R	0

Bit	Bit Name	Description	R/W	InitVal
24	DCD	Data Carrier Detect. 0=DCD# detected high 1=DCD# detected low In loopback mode, returns bit 2 of MCR. In normal mode, returns 1.	R	0

3.1.26. Baud Rate

Value of divisor latch = [System Clock / (16 * Baud Rate)] - 1
System Clock = Lexra Bus Clock

Example of the Divisor Latch value:

System CLK	2400 bps	4800 bps	9600 bps	19200 bps	38400 bps	57600 bps	115200 bps
200MHz	5207	2603	1301	650	325	162	80

3.1.27. Time-out Interrupt

A time-out interrupt occurs when the following conditions exists in at least one byte in the active descriptor buffer or receiver FIFO.

The most recent serial character was received more than four character times ago.

3.1.28. Auto-flow Control

Auto-RTS When the receiver FIFO reaches the trigger level, the RTS# is de-asserted. RTS# is automatically re-asserted once the FIFO is emptied. If RTS# is de-asserted, the UART must receive the incoming data until the FIFO is full.

Auto-CTS The transmitter checks CTS# before sending the next data byte. When CTS# is active, the transmitter sends the next data byte, otherwise it stops the transmission.

3.1.29. Loopback Diagnostic

When the LOOP bit is set, the following occurs.
TXD# is asserted high
RXD# is disconnected.
CTS#, DSR#, DCD#, and RI# are disconnected.
The output of the transmitter shift register is looped back into the input of the receiver shift register.
The MCR's DTR, RTS, OUT1, and OUT2 bits are internally connected to CTS#, DSR#, DCD#, and RI# respectively.
The DTR#, RTS#, OUT1#, and OUT2# pins are forced high.

3.1.30. Interrupt Priority

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Method
Bit3	Bit2	Bit1	Bit0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun, parity, framing errors or break	Read LSR
0	1	0	0	2	Received data available	DR bit is set	Read RBR
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to FIFO during the last character times and at 1 character in it.	Read RBR
0	0	1	0	3	Transmitter holding register empty	THRE bit set	Reading IIR or write THR
0	0	0	0	4	Modem status	CTS#, DSR#, RI#, DCD#	Reading MSR

3.1.31. Loopback Diagnostic

A break characters is an all-zero character whose length is start bit (1) + word length (7 or 8) + parity bit (0 or 1) + stop bits (1 or 2). The break event occurs after the first break character is received.

3.2. Interrupt Controller

3.2.1. Features

The RTL8390 provides a programmable interrupt controller. The Global Interrupt Mask Register (GIMR) is a global switch that can enable/disable each interrupt source. The GISR Interrupt Mask Register (GISR) shows the interrupt pending status of each source. The Interrupt Routing Register (IRR) maps each interrupt source onto CPU interrupt signal pins.

3.2.2. Register Set (Base Address: 0xB800_3000)

Table. Interrupt Control Register Set

Offset	Size (byte)	Name	Description
0x00	4	VPE0_GIMR	Global interrupt mask register for VPE0.
0x04	4	VPE0_GISR	Global interrupt status register for VPE0.
0x08	4	VPE0_IRR0	Interrupt routing register 0 for VPE0
0x0C	4	VPE0_IRR1	Interrupt routing register 1 for VPE0

Offset	Size (byte)	Name	Description
0x10	4	VPE0_IRR2	Interrupt routing register 2 for VPE0
0x14	4	VPE0_IRR3	Interrupt routing register 3 for VPE0
0x18	4	VPE1_GIMR	Global interrupt mask register for VPE1.
0x1C	4	VPE1_GISR	Global interrupt status register for VPE1.
0x20	4	VPE1_IRR0	Interrupt routing register 0 for VPE1
0x24	4	VPE1_IRR1	Interrupt routing register 1 for VPE1
0x28	4	VPE1_IRR2	Interrupt routing register 2 for VPE1
0x2C	4	VPE1_IRR3	Interrupt routing register 3 for VPE1

3.2.3. Global Interrupt Mask Register for VPE0 (VPE0_GIMR) (0xB800_3000)

Table. Global Interrupt Mask Register for VPE0 (VPE0_GIMR)

Bit	Bit Name	Description	R/W	InitVal
31	UART0_IE	UART0 interrupt enable	R/W	0
30	UART1_IE	UART1 interrupt enable	R/W	0
29	TC0_IE	Timer/Counter #0 interrupt enable	R/W	0
28	TC1_IE	Timer/Counter #1 interrupt enable	R/W	0
27	OCPTO_IE	OCP bus Timeout interrupt enable	R/W	0
26	HLXTO_IE	High speed Lexra bus interrupt enable	R/W	0
25	SLXTO_IE	Slave Lexra bus interrupt enable	R/W	0
24	NIC_IE	NIC interrupt enable	R/W	0
23	GPIO_ABC_IE	GPIO_ABC interrupt enable	R/W	0
22	USB_IE	USB interrupt enable	R/W	0
21	*reserved*		R	0
20	SWCORE_IE	Switch core interrupt enable	R/W	0
19	WDT_IE	Watchdog timer interrupt enable	R/W	0
18	*reserved*		R	0
17	TC2_IE	Timer/Counter #2 interrupt enable	R/W	0
16	TC3_IE	Timer/Counter #3 interrupt enable	R/W	0
15	TC4_IE	Timer/Counter #4 interrupt enable	R/W	0
14	TC2_DELAY_INT_IE	Delayed interrupt with Timer/Counter 2 interrupt enable.	R/W	0
13	TC3_DELAY_INT_IE	Delayed interrupt with Timer/Counter 3 interrupt enable	R/W	0
12	TC4_DELAY_INT_IE	Delayed interrupt with Timer/Counter 4 interrupt enable	R/W	0
11:0	*Reserved*		R	0

3.2.4. Global Interrupt Status Register for VPE0 (VPE0_GISR) (0xB800_3004)

Table. Global Interrupt Status Register for VPE0 (VPE0_GISR)

Bit	Bit Name	Description	R/W	InitVal
31	UART0_IP	UART0 interrupt pending flag	R	0
30	UART1_IP	UART1 interrupt pending flag	R	0
29	TC0_IP	Timer/Counter #0 interrupt pending flag	R	0
28	TC1_IP	Timer/Counter #1 interrupt pending flag	R	0
27	OCPTO_IP	OCP bus Timeout interrupt pending flag	R	0
26	HLXTO_IP	High speed Lexra bus interrupt pending flag	R	0
25	SLXTO_IP	Slave Lexra bus interrupt pending flag	R	0
24	NIC_IP	NIC interrupt pending flag	R	0
23	GPIO_ABC_IP	GPIO_ABC interrupt pending flag	R	0
22	USB_IP	USB interrupt pending flag	R	0
21	*reserved*		R	0
20	SWCORE_IP	Switch core interrupt pending flag	R	0
19	WDT_IP	Watchdog timer interrupt pending flag	R	0
18	*reserved*		R	0
17	TC2_IP	Timer/Counter #2 interrupt pending flag	R	0
16	TC3_IP	Timer/Counter #3 interrupt pending flag	R	0
15	TC4_IP	Timer/Counter #4 interrupt pending flag	R	0
14	TC2_DELAY_INT_IP	Delayed interrupt with Timer/Counter 2 interrupt pending flag.	R	0
13	TC3_DELAY_INT_IP	Delayed interrupt with Timer/Counter 3 interrupt pending flag.	R	0
12	TC4_DELAY_INT_IP	Delayed interrupt with Timer/Counter 4 interrupt pending flag.	R	0
11:0	*Reserved*		R	0

3.2.5. Interrupt Routing Register 0 for VPE0 (VPE0_IRR0) (0xB800_3008)

Table. Interrupt Routing Register 0 for VPE0 (VPE0_IRR0)

Bit	Bit Name	Description	R/W	InitVal
31:28	UART0_RS[3:0]	UART0 interrupt route select 0: N.C. (Not Connected) 1: INT#0 (Lower Priority) 2: INT#1 3: INT#2 4: INT#3 5: INT#4 6: INT#5 (Higher Priority) 7: NMI (Non-Maskable Interrupt) 8~15: N.C. Note: CPU internal timer is viewed as high priority and therefore fixed to be routed to INT#5	R/W	0
27:24	UART1_RS[3:0]	UART1 interrupt route select	R/W	0
23:20	TC0_RS[3:0]	Timer/Counter #0 interrupt route select	R/W	0
19:16	TC1_RS[3:0]	Timer/Counter #1 interrupt route select	R/W	0
15:12	OCPTO_RS[3:0]	OCP bus Timeout interrupt route select	R/W	0
11:8	HLXTO_RS[3:0]	High speed Lexra bus interrupt route select	R/W	0
7:4	SLXTO_RS[3:0]	Slave Lexra bus interrupt route select	R/W	0
3:0	NIC_RS[3:0]	NIC interrupt route select	R/W	0

3.2.6. Interrupt Routing Register 1 for VPE0 (VPE0_IRR1) (0xB800_300C)

Table. Interrupt Routing Register 1 for VPE0 (VPE0_IRR1)

Bit	Bit Name	Description	R/W	InitVal
31:28	GPIO_ABC_RS[3:0]	GPIO port A,B,C interrupt route select	R/W	0
27:24	USB_RS[3:0]	USB interrupt route select	R/W	0
23:20	*reserved*		R	0
19:16	SWCORE_RS[3:0]	Switch core interrupt route select	R/W	0
15:12	WDT_RS[3:0]	Watchdog timer interrupt route select	R/W	0
11:0	Reserved		R	0

[Notes]
When used to issue alarms, watchdog is generally treated as the highest priority, and therefore WDT_RS[3:0] is suggested to be set to 7 (NMI) by software. However, it must be noted that the exception vector of NMI is 0xBFC00000, unlike that of INT#0~INT#5.

3.2.7. Interrupt Routing Register 2 for VPE0 (VPE0_IRR2) (0xB800_3010)

Table. Interrupt Routing Register 2 for VPE0 (VPE0_IRR2)

Bit	Bit Name	Description	R/W	InitVal
31:28	TC2_RS[3:0]	Timer/Counter #2 route select	R/W	0
27:24	TC3_RS[3:0]	Timer/Counter #3 route select	R/W	0
23:20	TC4_RS[3:0]	Timer/Counter #4 route select	R/W	0
19:16	TC2_DELAY_INT_RS[3:0]	Delayed interrupt with Timer/Counter 2 interrupt route select	R/W	0
15:12	TC3_DELAY_INT_RS[3:0]	Delayed interrupt with Timer/Counter 3 interrupt route select	R/W	0
11:8	TC4_DELAY_INT_RS[3:0]	Delayed interrupt with Timer/Counter 4 interrupt route select	R/W	0
7:0	Reserved		R	0

3.2.8. Interrupt Routing Register 3 for VPE0 (VPE0_IRR3) (0xB800_3014)

Table. Interrupt Routing Register 3 for VPE0 (VPE0_IRR3)

Bit	Bit Name	Description	R/W	InitVal
31:0	Reserved		R	0

3.2.9. Global Interrupt Mask Register for VPE1 (VPE1_GIMR) (0xB800_3018)

Table. Global Interrupt Mask Register for VPE1 (VPE1_GIMR)

Bit	Bit Name	Description	R/W	InitVal
31	UART0_IE	UART0 interrupt enable	R/W	0
30	UART1_IE	UART1 interrupt enable	R/W	0
29	TC0_IE	Timer/Counter #0 interrupt enable	R/W	0
28	TC1_IE	Timer/Counter #1 interrupt enable	R/W	0
27	OCPTO_IE	OCP bus Timeout interrupt enable	R/W	0
26	HLXTO_IE	High speed Lexra bus interrupt enable	R/W	0
25	SLXTO_IE	Slave Lexra bus interrupt enable	R/W	0
24	NIC_IE	NIC interrupt enable	R/W	0
23	GPIO_ABC_IE	GPIO_ABC interrupt enable	R/W	0
22	USB_IE	USB interrupt enable	R/W	0
21	*reserved*		R	0
20	SWCORE_IE	Switch core interrupt enable	R/W	0
19	WDT_IE	Watchdog timer interrupt enable	R/W	0
18	*reserved*		R	0
17	TC2_IE	Timer/Counter #2 interrupt enable	R/W	0
16	TC3_IE	Timer/Counter #3 interrupt enable	R/W	0
15	TC4_IE	Timer/Counter #4 interrupt enable	R/W	0

Bit	Bit Name	Description	R/W	InitVal
14	TC2_DELAY_INT_IE	Delayed interrupt with Timer/Counter 2 interrupt enable.	R/W	0
13	TC3_DELAY_INT_IE	Delayed interrupt with Timer/Counter 3 interrupt enable	R/W	0
12	TC4_DELAY_INT_IE	Delayed interrupt with Timer/Counter 4 interrupt enable	R/W	0
11:0	*Reserved*		R	0

3.2.10. Global Interrupt Status Register for VPE1 (VPE1_GISR) (0xB800_301C)

Table. Global Interrupt Status Register for VPE1 (VPE1_GISR)

Bit	Bit Name	Description	R/W	InitVal
31	UART0_IP	UART0 interrupt pending flag	R	0
30	UART1_IP	UART1 interrupt pending flag	R	0
29	TC0_IP	Timer/Counter #0 interrupt pending flag	R	0
28	TC1_IP	Timer/Counter #1 interrupt pending flag	R	0
27	OCPTO_IP	OCP bus Timeout interrupt pending flag	R	0
26	HLXTO_IP	High speed Lexra bus interrupt pending flag	R	0
25	SLXTO_IP	Slave Lexra bus interrupt pending flag	R	0
24	NIC_IP	NIC interrupt pending flag	R	0
23	GPIO_ABC_IP	GPIO_ABC interrupt pending flag	R	0
22	USB_IP	USB interrupt pending flag	R	0
21	*reserved*		R	0
20	SWCORE_IP	Switch core interrupt pending flag	R	0
19	WDT_IP	Watchdog timer interrupt pending flag	R	0
18	*reserved*		R	0
17	TC2_IP	Timer/Counter #2 interrupt pending flag	R	0
16	TC3_IP	Timer/Counter #3 interrupt pending flag	R	0
15	TC4_IP	Timer/Counter #4 interrupt pending flag	R	0
14	TC2_DELAY_INT_IP	Delayed interrupt with Timer/Counter 2 interrupt pending flag.	R	0
13	TC3_DELAY_INT_IP	Delayed interrupt with Timer/Counter 3 interrupt pending flag.	R	0
12	TC4_DELAY_INT_IP	Delayed interrupt with Timer/Counter 4 interrupt pending flag.	R	0
11:0	*Reserved*		R	0

3.2.11. Interrupt Routing Register 0 for VPE1 (VPE1_IRR0) (0xB800_3020)

Table. Interrupt Routing Register 0 for VPE1 (VPE1_IRR0)

Bit	Bit Name	Description	R/W	InitVal
31:28	UART0_RS[3:0]	UART0 interrupt route select 0: N.C. (Not Connected) 1: INT#0 (Lower Priority) 2: INT#1 3: INT#2 4: INT#3 5: INT#4 6: INT#5 (Higher Priority) 7: NMI (Non-Maskable Interrupt) 8~15: N.C. Note: CPU internal timer is viewed as high priority and therefore fixed to be routed to INT#5	R/W	0
27:24	UART1_RS[3:0]	UART1 interrupt route select	R/W	0
23:20	TC0_RS[3:0]	Timer/Counter #0 interrupt route select	R/W	0
19:16	TC1_RS[3:0]	Timer/Counter #1 interrupt route select	R/W	0
15:12	OCPTO_RS[3:0]	OCP bus Timeout interrupt route select	R/W	0
11:8	HLXTO_RS[3:0]	High speed Lexra bus interrupt route select	R/W	0
7:4	SLXTO_RS[3:0]	Slave Lexra bus interrupt route select	R/W	0
3:0	NIC_RS[3:0]	NIC interrupt route select	R/W	0

3.2.12. Interrupt Routing Register 1 for VPE1 (VPE1_IRR1) (0xB800_3024)

Table. Interrupt Routing Register 1 for VPE1 (VPE1_IRR1)

Bit	Bit Name	Description	R/W	InitVal
31:28	GPIO_ABC_RS[3:0]	GPIO port A, B, C interrupt route select	R/W	0
27:24	USB_RS[3:0]	USB interrupt route select	R/W	0
23:20	*reserved*		R	0
19:16	SWCORE_RS[3:0]	Switch core interrupt route select	R/W	0
15:12	WDT_RS[3:0]	Watchdog timer interrupt route select	R/W	0
11:0	Reserved		R	0

3.2.13. Interrupt Routing Register 2 for VPE1 (VPE1_IRR2) (0xB800_3028)

Table. Interrupt Routing Register 2 for VPE1 (VPE1_IRR2)

Bit	Bit Name	Description	R/W	InitVal
31:28	TC2_RS[3:0]	Timer/Counter #2 interrupt pending flag	R/W	0
27:24	TC3_RS[3:0]	Timer/Counter #3 interrupt pending flag	R/W	0
23:20	TC4_RS[3:0]	Timer/Counter #4 interrupt pending flag	R/W	0

Bit	Bit Name	Description	R/W	InitVal
19:16	TC2_DELAY_INT_RS[3:0]	Delayed interrupt with Timer/Counter 2 interrupt route select	R/W	0
15:12	TC3_DELAY_INT_RS[3:0]	Delayed interrupt with Timer/Counter 3 interrupt route select	R/W	0
11:8	TC4_DELAY_INT_RS[3:0]	Delayed interrupt with Timer/Counter 4 interrupt route select	R/W	0
7:0	Reserved		R	0

3.2.14. Interrupt Routing Register 3 for VPE1 (VPE1_IRR3) (0xB800_302C)

Table. Interrupt Routing Register 3 for VPE1 (VPE1_IRR3)

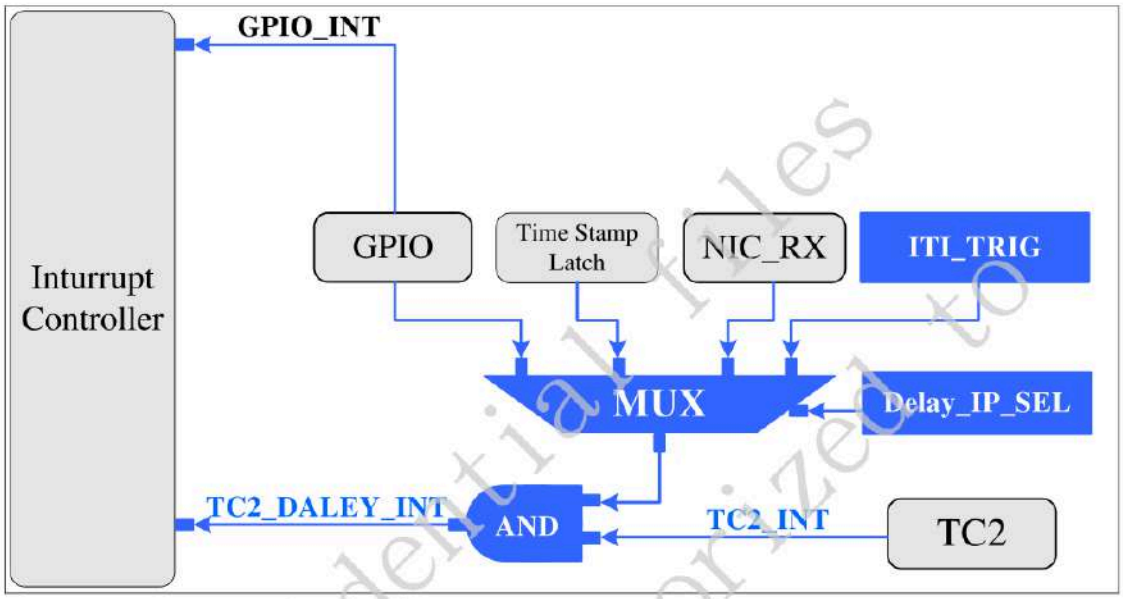
Bit	Bit Name	Description	R/W	InitVal
31:0	Reserved		R	0

3.3. Delayed Interrupt Controller

3.3.1. Feature

Delayed interrupt control integrates timers and built-in IP's interrupts to provide interrupts aggregation functionality. Any incoming interrupt is pending until the expiration of the timer. The delayed interrupt function benefits the system with more efficient interrupt handling.

The interrupts signals of built-in IP are the input of DELAY_IP_SEL configurable MUX. The output signal of the MUX then is ANDed with the timer interrupt signal to form an input interrupt signal of the interrupt controller. Users can choose built-in IPs listed in the DELAY_IP_SEL field in the Delayed interrupt Configuration Register to cooperate with the selected timer. There are up to 3 delayed interrupts in RTL8390 project possibly. The following diagram illustrates interconnection of the built-in IPs, timer 2, interrupt controller and delayed interrupt control.



3.3.2. Register Set (Base Address: 0xB800_3080)

TABLE 3-1 Delayed Interrupt Control Register Address Mapping (Base=0xB8003080)

Offset	Size (byte)	Name	Description
00	4	TC2DICR	TC2 Delayed Interrupt Configuration Register.
04	4	TC3DICR	TC3 Delayed Interrupt Configuration Register.
08	4	TC4DICR	TC4 Delayed Interrupt Configuration Register.

3.3.3. TC2 Delayed Interrupt Configuration Register (TC2DICR) (0xB800_3080)

TABLE 3-2 TC2 Delayed Interrupt Configuration Register (TC2DICR) (0xB800_3080)

Bit	Bit Name	Description	R/W	InitVal
31	ITI_TRIG	Trigger internal test interrupt.	R/W	0
30:4	*Reserved*		R/W	0
3:0	DELAYED_IP_SEL	Select the delayed interrupt source of TC2 delayed interrupt. 0000: NIC RX done interrupt 0001: TX/RX Time Stamp Latch (SWCORE) 0010: GPIO 1111:Internal test interrupt (internal use only) Others: reserved.	R/W	0x0

3.3.4. TC3 Delayed Interrupt Configuration Register (TC3DICR) (0xB800_3084)

TABLE 3-3 TC3 Delayed Interrupt Configuration Register (TC3DICR) (0xB800_3084)

Bit	Bit Name	Description	R/W	InitVal
31	ITI_TRIG	Trigger internal test interrupt.	R/W	0
30:4	*Reserved*		R/W	0
3:0	DELAYED_IP_SEL	Select the delayed interrupt source of TC3 delayed interrupt. 0000: NIC RX done interrupt 0001: TX/RX Time Stamp Latch (SWCORE) 0010: GPIO 1111:Internal test interrupt (internal use only)Others: reserved.	R/W	0x1

3.3.5. TC4 Delayed Interrupt Configuration Register (TC4DICR) (0xB800_3088)

TABLE 3-4 TC4 Delayed Interrupt Configuration Register (TC4DICR) (0xB800_3088)

Bit	Bit Name	Description	R/W	InitVal
31	ITI_TRIG	Trigger internal test interrupt.	R/W	0
30:4	*Reserved*		R/W	0
3:0	DELAYED_IP_SEL	Select the delayed interrupt source of TC4 delayed interrupt. 0000: NIC RX done interrupt 0001: TX/RX Time Stamp Latch (SWCORE) 0010: GPIO 1111:Internal test interrupt (internal use only) Others: reserved.	R/W	0x2

[Notes]

1. When the built-in IP is selected as the delayed interrupt source, software should disable the IP interrupt configuration in GIMR or the interrupt signal of the IP still propagates into CPU which leading to no delay effect.

3.4. Timer

3.4.1. Features

The RTL8390 provides 5 sets of hardware timers and one watchdog timer. Each timer can be configured as timer mode or counter mode. Counter mode means the timer only times-out once. The initial time-out values are configured via TC*n*DATA. The current count values are shown in TC*n*CNT. TC*n*CTL defines the base clock for counting, which is based on a multiple of the system clock. TCIR controls the interrupt resulting from timer time-out. The Watchdog timer is controlled by WDTCNR.

3.4.2. Register Set (Base Address: 0xB800_3100)

TABLE 3-5 Timer Control Register Set

Offset	Size (byte)	Name	Description
0x00	4	TC0DATA	Timer/Counter 0 data register. It specifies the time-out duration.
0x04	4	TC0CNT	Timer/Counter 0 counter register.
0x08	4	TC0CTL	Timer/Counter 0 control register.
0x0C	4	TC0INT	Timer/Counter 0 interrupt register
0x10	4	TC1DATA	Timer/Counter 1 data register. It specifies the time-out duration.
0x14	4	TC1CNT	Timer/Counter 1 counter register.
0x18	4	TC1CTL	Timer/Counter 1 control register.
0x1C	4	TC1INT	Timer/Counter 1 interrupt register
0x20	4	TC2DATA	Timer/Counter 2 data register. It specifies the time-out duration.
0x24	4	TC2CNT	Timer/Counter 2 counter register.
0x28	4	TC2CTL	Timer/Counter 2 control register.
0x2C	4	TC2INT	Timer/Counter 2 interrupt register
0x30	4	TC3DATA	Timer/Counter 3 data register. It specifies the time-out duration.
0x34	4	TC3CNT	Timer/Counter 3 counter register.
0x38	4	TC3CTL	Timer/Counter 3 control register.
0x3C	4	TC3INT	Timer/Counter 3 interrupt register
0x40	4	TC4DATA	Timer/Counter 4 data register. It specifies the time-out duration.
0x44	4	TC4CNT	Timer/Counter 4 counter register.
0x48	4	TC4CTL	Timer/Counter 4 control register.
0x4C	4	TC4INT	Timer/Counter 4 interrupt register
0x50	4	WDTCNTRR	Watchdog timer counter register.
0x54	4	WDTINTRR	Watchdog timer interrupt register.
0x58	4	WDTCTRLR	Watchdog timer control register.

3.4.3. Timer/Counter 0 Data Register (TC0DATA) (0xB800_3100)

TABLE 3-6 Timer/Counter 0 Data Register (0xB800_3100)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC0Data[27:0]	The timer or counter initial value. 0 and 1 not allowed	R/W	0

3.4.4. Timer/Counter 0 Counter Register (TC0CNT) (0xB800_3104)

TABLE 3-7 Timer/Counter 0 Counter Register (0xB800_3104)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC0Value[27:0]	The timer or counter value	R	0

3.4.5. Timer/Counter 0 Control Register (TC0CTL) (0xB800_3108)

TABLE 3-8 Timer/Counter 0 Control Register (0xB800_3108)

Bit	Bit Name	Description	R/W	InitVal
31:29	MUST_BE_ZERO		R	0
28	TC0En	Timer/Counter 0 enable	R/W	0
27:25	MUST_BE_ZERO		R	0
24	TC0Mode	Timer/Counter 0 mode 0=counter mode 1=timer mode	R/W	0
23:16	MUST_BE_ZERO		R	0
15:0	TC0DivFactor[15:0]	The divide factor of clock source. Assume DivFactor = N, then Base clock = System_clock /N. Both values 0x0000 and 0x0001 disable the clock. The TC0DivFactor[15:0] field defines the clock base for Timer/Counter 0 counting which is based on the input clock source (Normally Lexra bus clock) which is reflect on the clock control of the whole system.	R/W	0x0000

3.4.6. Timer/Counter 0 Interrupt Register (TC0INT) (0xB800_310C)

TABLE 3-9 Timer/Counter 0 Interrupt Register (0xB800_310C)

Bit	Bit Name	Description	R/W	InitVal
31:24	*Reserved*		R	0
23:21	MUST_BE_ZERO		R	0
20	TC0IE	Timer/Counter 0 interrupt enable.	R/W	0
19:17	MUST_BE_ZERO		R	0
16	TC0IP	Timer/Counter 0 interrupt pending. Write '1' to clear the interrupt.	R/WC	0
15:0	MUST_BE_ZERO		R	0

3.4.7. Timer/Counter 1 Data Register (TC1DATA) (0xB800_3110)

TABLE 3-10 Timer/Counter 1 Data Register (0xB800_3110)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC1Data[27:0]	The timer or counter initial value. 0 and 1 not allowed	R/W	0

3.4.8. Timer/Counter 1 Counter Register (TC1CNT) (0xB800_3114)

TABLE 3-11 Timer/Counter 1 Counter Register (0xB800_3114)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC1Value[27:0]	The timer or counter value	R	0

3.4.9. Timer/Counter 1 Control Register (TC1CTL) (0xB800_3118)

TABLE 3-12 Timer/Counter 1 Control Register (0xB800_3118)

Bit	Bit Name	Description	R/W	InitVal
31:29	MUST_BE_ZERO		R	0
28	TC1En	Timer/Counter 1 enable	R/W	0
27:25	MUST_BE_ZERO		R	0
24	TC1Mode	Timer/Counter 1 mode 0=counter mode 1=timer mode	R/W	0
23:16	MUST_BE_ZERO		R	0
15:0	TC1DivFactor[15:0]	The divide factor of clock source. Assume DivFactor = N, then Base clock = System_clock /N. Both values 0x0000 and 0x0001 disable the clock. The TC1DivFactor[15:0] field defines the clock base for Timer/Counter 0 counting which is based on the input clock source (Normally Lexra bus clock) which is reflect on the clock control of the whole system.	R/W	0x0000

3.4.10. Timer/Counter 1 Interrupt Register (TC1INT) (0xB800_311C)

TABLE 3-13 Timer/Counter 1 Interrupt Register (0xB800_311C)

Bit	Bit Name	Description	R/W	InitVal
31:24	*Reserved*		R	0
23:21	MUST_BE_ZERO		R	0
20	TC1IE	Timer/Counter 1 interrupt enable.	R/W	0
19:17	MUST_BE_ZERO		R	0
16	TC1IP	Timer/Counter 1 interrupt pending. Write '1' to clear the interrupt.	R/WC	0
15:0	MUST_BE_ZERO		R	0

3.4.11. Timer/Counter 2 Data Register (TC2DATA) (0xB800_3120)

TABLE 3-14 Timer/Counter 2 Data Register (0xB800_3120)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC2Data[27:0]	The timer or counter initial value. 0 and 1 not allowed	R/W	0

3.4.12. Timer/Counter 2 Counter Register (TC2CNT) (0xB800_3124)

TABLE 3-15 Timer/Counter 2 Counter Register (0xB800_3124)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC2Value[27:0]	The timer or counter value	R	0

3.4.13. Timer/Counter 2 Control Register (TC2CTL) (0xB800_3128)

TABLE 3-16 Timer/Counter 2 Control Register (0xB800_3128)

Bit	Bit Name	Description	R/W	InitVal
31:29	MUST_BE_ZERO		R	0
28	TC2En	Timer/Counter 2 enable	R/W	0
27:25	MUST_BE_ZERO		R	0
24	TC2Mode	Timer/Counter 2 mode 0=counter mode 1=timer mode	R/W	0
23:16	MUST_BE_ZERO		R	0
15:0	TC2DivFactor[15:0]	The divide factor of clock source. Assume DivFactor = N, then Base clock = System_clock /N. Both values 0x0000 and 0x0001 disable the clock. The TC2DivFactor[15:0] field defines the clock base for Timer/Counter 0 counting which is based on the input clock source (Normally Lexra bus clock) which is reflect on the clock control of the whole system.	R/W	0x0000

3.4.14. Timer/Counter 2 Interrupt Register (TC2INT) (0xB800_312C)

TABLE 3-17 Timer/Counter 2 Interrupt Register (0xB800_312C)

Bit	Bit Name	Description	R/W	InitVal
	Reserved		R	0
23:21	MUST_BE_ZERO		R	0
20	TC2IE	Timer/Counter 0 interrupt enable.	R/W	0
19:17	MUST_BE_ZERO		R	0
16	TC2IP	Timer/Counter 0 interrupt pending. Write '1' to clear the interrupt.	R/WC	0
15:0	MUST_BE_ZERO		R	0

3.4.15. Timer/Counter 3 Data Register (TC3DATA) (0xB800_3130)

TABLE 3-18 Timer/Counter 3 Data Register (0xB800_3130)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0

Bit	Bit Name	Description	R/W	InitVal
27:0	TC3Data[27:0]	The timer or counter initial value. 0 and 1 not allowed	R/W	0

3.4.16. Timer/Counter 3 Counter Register (TC3CNT) (0xB800_3134)

TABLE 3-19 Timer/Counter 3 Counter Register (0xB800_3134)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC3Value[27:0]	The timer or counter value	R	0

3.4.17. Timer/Counter 3 Control Register (TC3CTL) (0xB800_3138)

TABLE 3-20 Timer/Counter 3 Control Register (0xB800_3138)

Bit	Bit Name	Description	R/W	InitVal
31:29	MUST_BE_ZERO		R	0
28	TC3En	Timer/Counter 3 enable	R/W	0
27:25	MUST_BE_ZERO		R	0
24	TC3Mode	Timer/Counter 3 mode 0=counter mode 1=timer mode	R/W	0
23:16	MUST_BE_ZERO		R	0
15:0	TC3DivFactor[15:0]	The divide factor of clock source. Assume DivFactor = N, then Base clock = System_clock /N. Both values 0x0000 and 0x0001 disable the clock. The TC3DivFactor[15:0] field defines the clock base for Timer/Counter 0 counting which is based on the input clock source (Normally Lexra bus clock) which is reflect on the clock control of the whole system.	R/W	0x0000

3.4.18. Timer/Counter 3 Interrupt Register (TC3INT) (0xB800_313C)

TABLE 3-21 Timer/Counter 3 Interrupt Register (0xB800_313C)

Bit	Bit Name	Description	R/W	InitVal
31:24	*Reserved*		R	0
23:21	MUST_BE_ZERO		R	0
20	TC3IE	Timer/Counter 3 interrupt enable.	R/W	0
19:17	MUST_BE_ZERO		R	0
16	TC3IP	Timer/Counter 3 interrupt pending. Write '1' to clear the interrupt.	R/WC	0
15:0	MUST_BE_ZERO		R	0

3.4.19. Timer/Counter 4 Data Register (TC4DATA) (0xB800_3140)

TABLE 3-22 Timer/Counter 4 Data Register (0xB800_3140)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC4Data[27:0]	The timer or counter initial value. 0 and 1 not allowed	R/W	0

3.4.20. Timer/Counter 4 Counter Register (TC4CNT) (0xB800_3144)

TABLE 3-23 Timer/Counter 4 Counter Register (0xB800_3144)

Bit	Bit Name	Description	R/W	InitVal
31:28	MUST_BE_ZERO		R	0
27:0	TC4Value[27:0]	The timer or counter value	R	0

3.4.21. Timer/Counter 4 Control Register (TC4CTL) (0xB800_3148)

TABLE 3-24 Timer/Counter 4 Control Register (0xB800_3148)

Bit	Bit Name	Description	R/W	InitVal
31:29	MUST_BE_ZERO		R	0
28	TC4En	Timer/Counter 4 enable	R/W	0
27:25	MUST_BE_ZERO		R	0
24	TC4Mode	Timer/Counter 4 mode 0=counter mode 1=timer mode	R/W	0
23:16	MUST_BE_ZERO		R	0
15:0	TC4DivFactor[15:0]	The divide factor of clock source. Assume DivFactor = N, then Base clock = System_clock /N. Both values 0x0000 and 0x0001 disable the clock. The TC4DivFactor[15:0] field defines the clock base for Timer/Counter 0 counting which is based on the input clock source (Normally Lexra bus clock) which is reflect on the clock control of the whole system.	R/W	0x0000

3.4.22. Timer/Counter 4 Interrupt Register (TC4INT) (0xB800_314C)

TABLE 3-25 Timer/Counter 4 Interrupt Register (0xB800_314C)

Bit	Bit Name	Description	R/W	InitVal
31:24	*Reserved*		R	0
23:21	MUST_BE_ZERO		R	0
20	TC4IE	Timer/Counter 4 interrupt enable.	R/W	0
19:17	MUST_BE_ZERO		R	0
16	TC4IP	Timer/Counter 4 interrupt pending. Write ‘1’ to clear the interrupt.	R/WC	0
15:0	MUST_BE_ZERO		R	0

3.4.23. Watchdog Timer Counter Register (WDTCNTRR) (0xB800_3150)

TABLE 3-26 Watch Dog Counter Register (0xB800_3150)

Bit	Bit Name	Description	R/W	InitVal
31	WDT_KICK	Watch Dog "KICK" register. Write "1" to clear (reset) WDT_TO_CNTR. ***Note***: The counter is only clearable in PH1, so that this bit is actually effective only when "WDT_KICK_ALLOW=1". ***Note***: "WDT_KICK_ALLOW" is the H/W signal used to judge whether WDT_TO_CNTR .is clearable.	WC	0
30:0	RESERVED		R	0

3.4.24. Watchdog Timer Interrupt Register (WDTINTRR) (0xB800_3154)

TABLE 3-27 Watch Dog Interrupt Register (0xB800_3154)

Bit	Bit Name	Description	R/W	InitVal
31	PH1_IP	PH1 interrupt pending flag. [R] 0: Normal 1: Interrupt pending [WC] Write "1" to clear	R/WC	0
30	PH2_IP	PH1 interrupt pending flag. [R] 0: Normal 1: Interrupt pending [WC] Write "1" to clear	R/WC	0
29:0	RESERVED		R	0

3.4.25. Watchdog Timer Control Register (WDTCTRLR) (0xB800_3158)

TABLE 3-28 Watch Dog Control Register (0xB800_3158)

Bit	Bit Name	Description	R/W	InitVal
31	WDT_E	Watch dog timer enable 0: Disable WDT 1: Enable WDT and cause a system reset in PH2 when an overflow signal occurs.	R/W	0
30:29	WDT_CLK_SC	WDT_CLK_CNTR overflow scale. These bits specify the overflow condition when WDT_CLK_CNTR counts to the value, which will trigger WDT_TO_CNTR to count one. $00_B = 2^{25}$ $01_B = 2^{26}$ $10_B = 2^{27}$ $11_B = 2^{28}$	R/W	00_B

28:27	RESERVED		R	00_B
26:22	PH1_TO	PH1 timeout threshold: 00000_B = 1 … 11111_B = 32 ***Note***: This is the overflow threshold for WDT_TO_CNTR in PH1.	R/W	00000_B
21:20	RESERVED		R	00_B
19:15	PH2_TO	PH2 timeout threshold: 00000_B = 1 … 11111_B = 32 ***Note***: This is the overflow threshold for WDT_TO_CNTR in PH2.	R/W	00000_B
14:2	RESERVED		R	0
1:0	WDT_RESET_MODE	Select WDOG reset mode when it is in PH2 timeout. 00_B: H/W Full Chip Reset (Do full reset at PH2_IP rising edge); 01_B: H/W CPU (Only reset CPU) 10_B: S/W Reset 11_B: Reserved	R/W	01_B

[Notes]

2. If WDT_RESET_MODE = 01_B or 10_B: WDOG IP will not be reset in these cases, so that the setting of this register will not be changed.
3. If WDT_RESET_MODE = 00_B: When doing full chip reset, WDOG IP will also be reset.
4. WDT_CLK_CNTR is an internal 28-bit auto up-counter, which will add one based on the LX bus clock domain. When WDT_CLK_CNTR counts to the overflow threshold (WDT_CLK_SC), it will trigger another internal counter, WDT_TO_CNTR, to add one.
5. When WDT_TO_CNTR counts to the overflow threshold in PH1 (PH1_TO), WDT will enter PH2 and not allow "KICK" anymore.
6. When WDT_TO_CNTR counts to the overflow threshold in PH2 (PH2_TO), it will do "RESET" according to WDT_RESET_MODE.
7. The results of different timeout threshold combinations:

LX Bus	WDT_CLK_SC	$Timeout_{min}$	$Timeout_{Max}$
200MHz	2^{28}	1.34s	42.88s
	2^{27}	0.67s	21.44s
	2^{26}	0.34s	10.88s
	2^{25}	0.17s	5.44s

   - Since the "RESET" should be done after all the jobs on LX bus are finished, the total timeout period in PH2 will a little bit more than the value in the above table.
8. This IP can also support only one phase WDOG timeout mechanism, when user enables "WDT_PH1TO_IE" and sets "WDT_PH1TO_RS" to NMI mode. Then if PH1 timeout happens, PH1_IP will trigger S/W and so that WDOG will not enter PH2 stage.
9. After reset, software can check WDT_RESET_MODE for knowing which reset was did last time.
   - WDT_RESET_MODE=00_B: It was doing full chip reset.
   - WDT_RESET_MODE≠00_B: Referring to this register setting for the reset mode.

3.5. Lexra Bus Timeout Monitor

3.5.1. Features

If an undefined address access occurs, the associated Lexra bus will cause the system hang since no devices respond. This bus timeout mechanism is provided to avoid this situation from happening. When the bus timer times out, it shall release the bus and may generate interrupt signal to interrupt controller for software to appropriately handle this unexpected exception. The function can help software development and debugging.

3.5.2. Register Set (Base Address: 0xB800_3400)

Table. Lexra Bus Timeout Monitor Set

Offset	Size (byte)	Name	Description
0x00	4	HLBTCR	High-speed Lexra Bus Timeout Control Register
0x04	4	HLBTIR	High-speed Lexra Bus Timeout Interrupt Register
0x08	4	HLBTMAR	High-speed Lexra Bus Timeout Monitored Address Register
0x10	4	SLBTCR	Slave Lexra Bus Timeout Control Register
0x14	4	SLBTIR	Slave Lexra Bus Timeout Interrupt Register
0x18	4	SLBTMAR	Slave Lexra Bus Timeout Monitored Address Register
0x20	4	HLBDBG	High-speed Lexra Bus Debug Register
0x24	4	SLBDBG	Slave Lexra Bus Debug Register

3.5.3. High-speed Lexra Bus Timeout Control Register (HLBTCR) (0xB800_3400)

Table. High-speed Lexra Bus Timeout Control Register

Bit	Bit Name	Description	R/W	InitVal
31	HLX_TCEN	High-speed Lexra Bus Timeout Control Enable 0: Disable 1: Enable	R/W	1
30-28	HLX_TCT	High-speed Lexra Bus Timeout Control Threshold Basic Unit = Bus Clock 000: 512 units 001: 1024 units 010: 2048 units 011: 4096 units 100: 8192 units 101: 16384 units 110: 32768 units 111: 65536 units	R/W	111

3.5.4. High-speed Lexra Bus Timeout Interrupt Register (HLBTIR) (0xB800_3404)

Table. High-speed Lexra Bus Timeout Interrupt Register

Bit	Bit Name	Description	R/W	InitVal
31	HLX_IP	High-speed Lexra Bus Interrupt Pending 0: Nothing 1: Interrupt Pending Write '1' to clear the interrupt.	R/W	0

3.5.5. High-speed Lexra Bus Timeout Monitored Address Register (HLBTMAR) (0xB800_3408)

Table. High-speed Lexra Bus Timeout Monitored Address Register

Bit	Bit Name	Description	R/W	InitVal
31-0	HLX_ADDR	High-speed Lexra Bus Timeout Monitored Address	R	0

3.5.6. Slave Lexra Bus Timeout Control Register (SLBTCR) (0xB800_3410)

Table. Slave Lexra Bus Timeout Control Register

Bit	Bit Name	Description	R/W	InitVal
31	SLX_TCEN	Slave Lexra Bus Timeout Control Enable 0: Disable 1: Enable	R/W	1
30-28	SLX_TCT	High-speed Lexra Bus Timeout Control Threshold Basic Unit = Bus Clock 000: 512 units 001: 1024 units 010: 2048 units 011: 4096 units 100: 8192 units 101: 16384 units 110: 32768 units 111: 65536 units	R/W	111

3.5.7. Slave Lexra Bus Timeout Interrupt Register (SLBTCR) (0xB800_3414)

Table. Slave Lexra Bus Timeout Interrupt Register

Bit	Bit Name	Description	R/W	InitVal
31	SLX_IP	Slave Lexra Bus Interrupt Pending 0: Nothing 1: Interrupt Pending Write '1' to clear the interrupt.	R/W	0

3.5.8. Slave Lexra Bus Timeout Monitored Address Register (SLBTMAR) (0xB800_3418)

Table. Slave Lexra Bus Timeout Monitored Address Register

Bit	Bit Name	Description	R/W	InitVal
31-0	SLX_ADDR	Slave Lexra Bus Timeout Monitored Address	R	0

[Notes]

- If Lexra bus timeout monitor detects a bus timeout, it shall save the requesting bus address to this register. This could help software debugging.

3.5.9. High-speed Lexra Bus Debug Register (HLBDBG) (0xB800_3420)

Table. High-Speed Lexra Bus Debug Register

Bit	Bit Name	Description	R/W	InitVal
31-0	DBG_DATA	Write 0xDeadC0D1 to generate High-speed Lexra Bus Interrupt The read back data will be 1's complement of the previous write data	R/W	0

3.5.10. Slave Lexra Bus Debug Register (SLBDBG) (0xB800_3424)

Table. Slave Lexra Bus Debug Register

Bit	Bit Name	Description	R/W	InitVal
31-0	DBG_DATA	Write 0xDeadC0D1 to generate Slave Lexra Bus Interrupt The read back data will be 1's complement of the previous write data	R/W	0

3.6. GPIO

3.6.1. Features

The RTL8390 provides 3 sets of General Purpose Input/Output (GPIO) pins (GPIO A, B, C Total 24 pins). Each GPIO pin might either be bidirectional (input/output), input only or output only. The GPIO Data registers can be used to control the signals of GPIO pins. Each GPIO pin can be used to generate interrupts. The corresponding interrupt masks and status registers are also provided. All GPIO related registers are defined as following table.

Note: GPIO A maps to GPIO[7:0], GPIO B maps to GPIO[15:8], and GPIO C maps to GPIO[23:16].

3.6.2. Register Set (Base Address: 0xB800_3500)

Table. GPIO Register Set

Offset	Size (byte)	Name	Description
0x00	4	PABC_CNR	Port A,B,C control register
0x04	4	*reserved*	
0x08	4	PABC_DIR	Port A,B,C direction register
0x0C	4	PABC_DAT	Port A,B,C data register
0x10	4	PABC_ISR	Port A,B,C interrupt status register
0x14	4	PAB_IMR	Port A,B interrupt mode register
0x18	4	PC_IMR	Port C interrupt mode register
0x1C	4	*reserved*	
0x20	4	*reserved*	
0x24	4	*reserved*	
0x28	4	*reserved*	
0x2C	4	*reserved*	
0x30	4	*reserved*	
0x34	4	*reserved*	

3.6.3. GPIO Port A, B, C Control Register (PABC_CNR) (0xB800_3500)

Table. GPIO Port A,B,C Control Register (PABC_CNR) (0xB800_3500)

Bit	Bit Name	Description	R/W	InitVal
31:24	PFC_A[7:0]	Pin function configuration of Port A. Bit value : 0=Configured as GPIO pin 1=Configured as dedicated peripheral pin	R/W	FFH
23:16	PFC_B[7:0]	Pin function configuration of Port B.	R/W	FFH
15:8	PFC_C[7:0]	Pin function configuration of Port C.	R/W	FFH
7:0	reserved			

3.6.4. GPIO Port A, B, C Direction Register (PABC_DIR) (0xB800_3508)

Table. GPIO Port A, B, C Direction Register (PABC_DIR)

Bit	Bit Name	Description	R/W	InitVal
31:24	DRC_A[7:0]	Pin direction configuration of Port A. 0=Configured as input pin 1=Configured as output pin	R/W	00H
23:16	DRC_B[7:0]	Pin direction configuration of Port B.	R/W	00H
15:8	DRC_C[7:0]	Pin direction configuration of Port C.	R/W	00H
7:0	*reserved*			

3.6.5. GPIO Port A, B, C Data Register (PABC_DAT) (0xB800_350C)

Table. Port A,B,C Data Register (PABC_DAT)

Bit	Bit Name	Description	R/W	InitVal
31:24	PD_A[7:0]	Pin data of Port A. 0 : Data=0 1 : Data=1	Input pin: R Output pin: R/W	00H
23:16	PD_B[7:0]	Pin data of Port B.	Input pin: R Output pin: R/W	00H
15:8	PD_C[7:0]	Pin data of Port C.	Input pin: R Output pin: R/W	00H
7:0	*reserved*			

3.6.6. GPIO Port A, B, C Interrupt Status Register (PABC_ISR) (0xB800_3510)

Table. Port A,B,C Interrupt Status Register (PABC_ISR)

Bit	Bit Name	Description	R/W	InitVal
31:24	IPS_A[7:0]	Interrupt pending status of port A. Write '1' to clear the interrupt	R/WC	00H
23:16	IPS_B[7:0]	Interrupt pending status of port B. Write '1' to clear the interrupt	R/WC	00H
15:8	IPS_C[7:0]	Interrupt pending status of port C. Write '1' to clear the interrupt	R/WC	00H
7:0	*reserved*			

3.6.7. GPIO Port A,B Interrupt Mode Register (PAB_IMR) (0xB800_3514)

Table. Port A,B Interrupt Mode Register (PAB_IMR)

Bit	Bit Name	Description	R/W	InitVal
31:30	PA7_IM[1:0]	PortA.7 interrupt mode. 00=Disable interrupt 01=Enable falling edge interrupt 10=Enable rising edge interrupt 11=Enable both falling or rising edge interrupt	R/W	00B
29:28	PA6_IM[1:0]	PortA.6 interrupt mode.	R/W	00B
27:26	PA5_IM[1:0]	PortA.5 interrupt mode.	R/W	00B
25:24	PA4_IM[1:0]	PortA.4 interrupt mode.	R/W	00B
23:22	PA3_IM[1:0]	PortA.3 interrupt mode.	R/W	00B
21:20	PA2_IM[1:0]	PortA.2 interrupt mode.	R/W	00B
19:18	PA1_IM[1:0]	PortA.1 interrupt mode.	R/W	00B
17:16	PA0_IM[1:0]	PortA.0 interrupt mode.	R/W	00B
15:14	PB7_IM[1:0]	PortB.7 interrupt mode.	R/W	00B
13:12	PB6_IM[1:0]	PortB.6 interrupt mode	R/W	00B
11:10	PB5_IM[1:0]	PortB.5 interrupt mode.	R/W	00B

Bit	Bit Name	Description	R/W	InitVal
9:8	PB4_IM[1:0]	PortB.4 interrupt mode.	R/W	00B
7:6	PB3_IM[1:0]	PortB.3 interrupt mode.	R/W	00B
5:4	PB2_IM[1:0]	PortB.2 interrupt mode.	R/W	00B
3:2	PB1_IM[1:0]	PortB.1 interrupt mode.	R/W	00B
1:0	PB0_IM[1:0]	PortB.0 interrupt mode.	R/W	00B

3.6.8. GPIO Port C Interrupt Mode Register (PC_IMR) (0xB800_3518)

Table. Port C Interrupt Mode Register (PC_IMR)

Bit	Bit Name	Description	R/W	InitVal
31:30	PC7_IM[1:0]	PortC.7 interrupt mode. 00=Disable interrupt 01=Enable falling edge interrupt 10=Enable rising edge interrupt 11=Enable both falling or rising edge interrupt	R/W	00B
29:28	PC6_IM[1:0]	PortC.6 interrupt mode.	R/W	00B
27:26	PC5_IM[1:0]	PortC.5 interrupt mode.	R/W	00B
25:24	PC4_IM[1:0]	PortC.4 interrupt mode.	R/W	00B
23:22	PC3_IM[1:0]	PortC.3 interrupt mode.	R/W	00B
21:20	PC2_IM[1:0]	PortC.2 interrupt mode.	R/W	00B
19:18	PC1_IM[1:0]	PortC.1 interrupt mode.	R/W	00B
17:16	PC0_IM[1:0]	PortC.0 interrupt mode.	R/W	00B
15:0	*reserved*			

3.7. LX Clock Frequency Controller

3.7.1. Features

The LX Clock Frequency Controller can make clk_lx < clk_m after boot-up.

3.7.2. Register Set (Base Address: 0xB800_3600)

Table. LX Clock Frequency Controller Register Set

Offset	Size (byte)	Name	Description
0x00	4	LXCFS	LX Clock Frequency Slow Register

3.7.3. LX Clock Frequency Slow Register (LXCFS) (0xB800_3600)

Table. LX Clock Frequency Slow Register

Bit	Bit Name	Description	R/W	InitVal
31	LX_CLK_SLOW	0: clk_lx > clk_m 1: clk_lx < clk_m	R/W	0
30-0	*reserved*		R	0

3.8. OCP Bus Timeout Monitor

3.8.1. Features

If an undefined address access occurs, the associated OCP bus will cause the system hang since no devices respond. This bus timeout mechanism is provided to avoid this situation from happening. When the bus timer times out, it shall release the bus and may generate interrupt signal to interrupt controller for software to appropriately handle this unexpected exception. The function can help software development and debugging.

3.8.2. Register Set (Base Address: 0xB800_5100)

Table. Bus Timeout Monitor Register Set

Offset	Size (byte)	Name	Description
0x00	4	OBTCR	OCP Bus Timeout Control Register
0x04	4	OBTIR	OCP Bus Timeout Interrupt Register
0x08	4	OBTMAR	OCP Bus Timeout Monitored Address Register

3.8.3. OCP Bus Timeout Control Register (OBTCR) (0xB800_5100)

Table. OCP Bus Timeout Control Register

Bit	Bit Name	Description	R/W	InitVal
31	OCP_TCEN	OCP Bus Timeout Control Enable 0: Disable 1: Enable	R/W	1
30	OCP_BERR	OCP Bus Error Indication 0: Disable 1: Enable	R/W	0

Bit	Bit Name	Description	R/W	InitVal
29-26	OCP_TCT	OCP Bus Timeout Control Threshold Basic Unit = Bus Clock (CPU Clock) 0000: 512 units (2^9) 0001: 1024 units (2^{10}) 0010: 2 * 1024 units (2^{11}) 0011: 4 * 1024 units (2^{12}) 0100: 8 * 1024 units (2^{13}) 0101: 16 * 1024 units (2^{14}) 0110: 32 * 1024 units (2^{15}) 0111: 64 * 1024 units (2^{16}) 1000: 128 * 1024 units (2^{17}) 1001: 256 * 1024 units (2^{18}) 1010: 512 * 1024 units (2^{19}) 1011: 1024 * 1024 units (2^{20}) 1100: 2 * 1024 * 1024 units (2^{21}) 1101: 4 * 1024 * 1024 units (2^{22}) 1110: 8 * 1024 * 1024 units (2^{23}) 1111: 16 * 1024 * 1024 units (2^{24})	R/W	1111

[Notes]

- MIPS 34Kc may issue more OCP transaction requests than OCP slaves in our system can afford, and therefore the maximum legal command accept latency is not easy to be measured. Since the bus timeout function is mainly for software debugging, it is acceptable to accommodate a fairly large timeout threshold.
- Also a large timeout threshold will naturally ensure read transaction ordering. That is, when the bus timeout monitor have to response to a read transaction, all prior read transactions must have already completed.

3.8.4. OCP Bus Timeout Interrupt Register (OBTIR) (0xB800_5104)

Table. OCP Bus Timeout Interrupt Register

Bit	Bit Name	Description	R/W	InitVal
31	OCP_IP	OCP Bus Timeout Interrupt Pending. 0: Nothing 1: Interrupt Pending Write '1' to clear the interrupt.	R/WC	0

3.8.5. OCP Bus Timeout Interrupt Register (OBTMAR) (0xB800_5108)

Table. OCP Bus Timeout Monitored Address Register

Bit	Bit Name	Description	R/W	InitVal
31-0	OCP_ADDR	OCP Bus Timeout Monitored Address	R	0

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