RTL9607C

SINGLE-CHIP PON

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CPU NIC Application Note

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for use by the system engineer when integrating with Realtek Managedd Switch Software. Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

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Revision History

Revision	Release Date	Summary
1.0.0	2017/05/30	First release

Table of Contents

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1 Overview

The CPU NIC (GMAC) HW use to interface CPU and switch on RTL9607C. This application note descripts how to control GMAC for packet TX/RX process.

For CPU NIC Rx, switch can pass the additional RX information to the CPU NIC via insert Realtek proprietary CPU-Tag. CPU NIC will parse CPU-TAG and translate to “rx_info” that software can get this information from “rx_info”. For CPU NIC Tx, software can modify “tx_info” then pass to CPU NIC, it will insert Realtek CPU-Tag and fill tag information according to software “tx_info”.

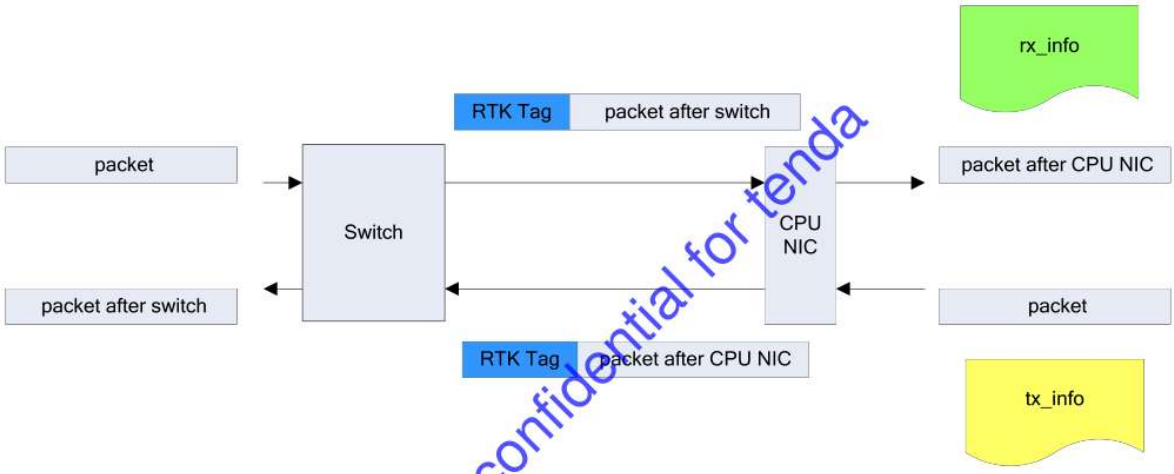

Figure 1 CPU NIC parsing flow

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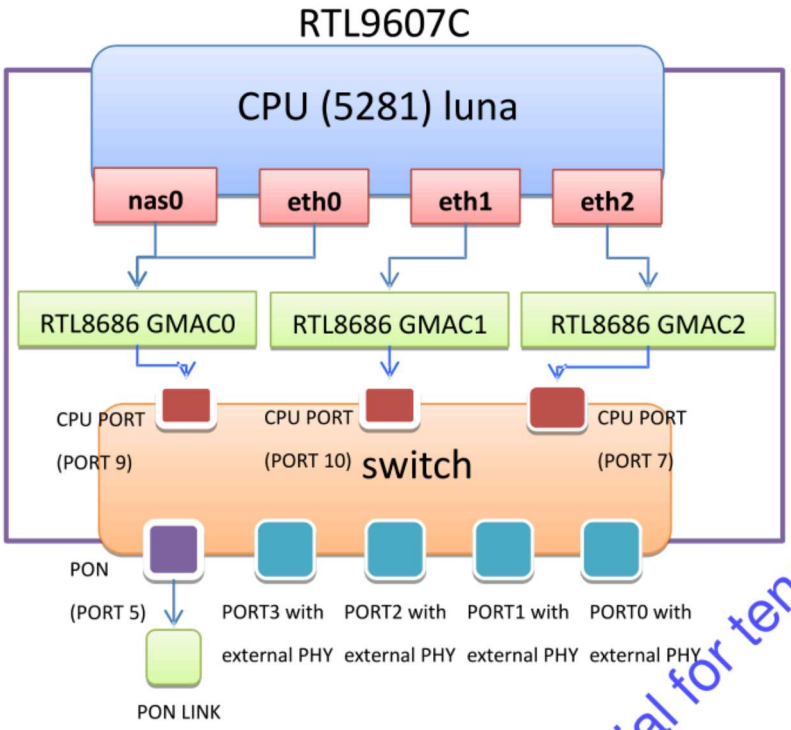
2 CPU NIC Driver

CPU NIC driver for RTL9607C, which reside in re8686_rtl9607c.c and re8686_rtl9607c.h, are located at luna/linux-3.18/drivers/net/Ethernet/realtek.



User can get physical port and Linux logical interface mapping from proc file.

```
# cat /proc/rtl8686gmac/dev_port_mapping
PON PORT 5, CPU PORT 9
DEV ability: eth0 eth1 eth2 eth0.2 eth0.3 eth0.4 eth0.5 nas0 pon0
rx: phyPort -> dev[the packet rx from phyPort will send to kernel using dev]
port0 -> eth0.2
port1 -> eth0.3
port2 -> eth0.4
port3 -> eth0.5
port4 -> eth0
port5 -> nas0
port6 -> eth0
port7 -> eth0
port8 -> eth0
port9 -> eth0
port10 -> eth0
tx:dev -> txPortMask[when tx from dev, we will use this txPortMask]
eth0 -> 0x0
eth1 -> 0x0
eth2 -> 0x0
```

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```
eth0.2 -> 0x1
eth0.3 -> 0x2
eth0.4 -> 0x4
eth0.5 -> 0x8
nas0 -> 0x20
pon0 -> 0x20
```

The mapping table would be chaged by seeting this proc file.

```
# echo "1 nas0">/proc/rtl8686gmac/dev_port_mapping

nas0 -> 0x02

rtl8686gmac/dev_port_mapping
```

Customer can read/write above of GMAC1 and GMAC2 by /proc/rtl8686gmac1/dev_port_mapping and /proc/rtl8686gmac2/dev_port_mapping respectively.

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3 TX procedure

CPU NIC Tx will modify packet content and add CPU tag according to TX descriptor.
TX part hook to linux device driver is “re8670_start_xmit”.

```
dev->hard_start_xmit = re8670_start_xmit
```

GMAC provide some advanced features, user can give more information to TX descriptor in “tx_info”. If user need to do customize please modify tx_info in re8670_start_xmit. Customers can reference function “tx_additional_setting()”.

3.1 tx_info structure

Table 1 Tx info structure

Field Name	Bits	Description
own	1	Don’t care and do not modify
eor	1	Don’t care and do not modify
fs	1	Don’t care and do not modify
ls	1	Don’t care and do not modify
ipcs	1	Set to 0 for jumbo frames, otherwise set to 1
l4cs	1	Set to 0 for jumbo frames, otherwise set to 1
tpid_sel	1	Select tpid which used to insert/ remark S-tag

		0b0: use stag_pid 0b1: use stag_pid1
stag_aware	1	Aware S-tag or not 0b0: Only aware C-tag 0b1: Aware S-tag and C-tag
crc	1	If this bit is set then append CRC at the end of Ethernet frame. For short packet (<64B), this bit must set to 1.
data_tength	17	Tx buffer packet size
cputag	1	Force CPU NIC generate Realteck CPU-tag Always set to 1
tx_svlan_action	2	CPU NIC VLAN tx action. SVLAN action for this egress frame 0b00: intact, 0b01: insert SVLAN header, 0b10: remove SVLAN hdr, 0b11: remarking SVID The command action is executed by CPU NIC module. VLAN header information is {svlan_vidl, svlan_vidh, svlan_prio, svlan_cfi} VLAN tag maybe modify again by switch decision.
tx_cvlan_action	2	CPU NIC CVLAN tx action. CVLAN action for this egress frame 0b00: intact, 0b01: insert CVLAN header, 0b10: remove CVLAN hdr, 0b11: remarking CVID The command action is executed by CPU NIC module.

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		VLAN header information is {cvlan_vidl,cvlan_vidh,cvlan_prio cvlan_cfi} VLAN tag maybe modify again by switch decision.
tx_portmask	11	(add information to CPU-tag) Command switch force forwarding using this tx_portmask.
cvlan_vidl	8	CVLAN tag vid[7:0]
cvlan_vidh	4	CVLAN tag vid[11:8]
cvlan_prio	3	CVLAN tag priority
cvlan_cfi	1	CVLAN tag CFI
aspri	1	(add information to CPU-tag) Turn on CPU force priority for this packet
cputag_pri	3	(add information to CPU-tag) CPU force priority (for switch internal priority) This field valid when aspri =1
keep	1	(add information to CPU-tag) Commands switch do keep original packet do not modify packet (remarking, VLAN translation …).
dislrn	1	(add information to CPU-tag) Command switch to disable switch l2 learning for this packet
cputag_psel	1	(add information to CPU-tag) For PON stream id (for GPON)/LLID index(for EPON) selections. This bit valid only tx_portmask including PON port. The stream id/LLID index is assign by “tx_dst_stream_id”
extspa	3	(add information to CPU-tag) Source extension port.

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tx_pppoe_action	2	Egress action for PPPoE header whose Ether Type = 0x8864. 0b00: intact, 0b01: Add PPPoE header, 0b10: remove PPPoE hdr, 0b11: remarking PPPoE switch Tx mac action This field should be set to 0b00 by software if "HW Lookup" = 0.
tx_pppoe_idx	4	PPPoE index pointed to an entry of the pppoe table in switch. Switch TX-MAC look PPPoE table up by this index to get PPPoE session ID. This field is valid only if "TX PPPoE Present" = 0x01 or 0x11.
tx_dst_stream_id	7	(add information to CPU-tag) If cputag_psel=1: PON stream id(for GPON)/LLID index(for EPON) If ptp=1: PON Queue id Priroty PTP > PSEL
lgsen	1	Large send offload enable. SW only sets lgsen to high when the egress must be fragmented. For single egress packet, lgsen must be low.
lgmtu	11	Large send max transmit unit value. Lgmtu minus IP header length should be 8n.
svlan_vidl	8	SVLAN tag vid[7:0]
svlan_vidh	4	SVLAN tag vid[11:8]
svlan_prio	3	SVLAN tag priority
svlan_cfi	1	SVLAN tag CFI

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4 Rx procedure

ASIC forward or trap to CPU port will add a CPU-Tag, CPU NIC parsing CPU-tag and packet content translate information into RX descriptor. Software can get some extra information from descriptor. CPU NIC will remove CVLAN tag, and keep VLAN tag information in descriptor.

4.1 Rx Hook

For packet Rx, system provided hook function, the hook API. Here list the hook API.

```
/* Purpose: Used for hook rx callback function
* Parameters:
*  gmac - GMAC index, 0 for GMAC0, 1 for GMAC1 and 2 for GMAC2
*  port - this callback function want to receive from which ports
*  pfunc  - callback function
*/
int re8686_register_rxfunc_by_port(unsigned int gmac, unsigned int port,
p2rfunc_t pfunc)
```

Customer can process packet in rx callback. Here lsit rx callback prototype.

```
typedef int (*p2rfunc_t)(struct re_private *cp, struct sk_buff *skb, struct
rx_info *pRxInfo)
```

The CPU NIC parsing info will keep in rx_info.

The return code of callback function would be follows.

RE8670_RX_STOP	packet have handled and occupied by this callback do not call other callback function
RE8670_RX_CONTINUE	continue to call other callback
RE8670_RX_STOP_SKBNOFREE	stop call other callback and do not free skb

Customer can unregister rx callback by `re8686_reset_rxfunc_to_default(unsigned int gmac)` API.

4.2 RX Ring configuration

CPU NIC provide 6 RX ring, customer can configured ring size in re8686_9607c.h. Each ring had its own ring size definition, if set to 0 means do not using this ring. Please set the size in order of 2. Here list an example set GMAC0 and GMAC1 RX ring size of ring1 to 1024, ring2~ring3 set to 256, ring4~ring6 set to 64, and do not use all RX rings of GMAC2.

```
#define GMAC0_RX1_SIZE 1024
```

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```
#define GMAC0_RX2_SIZE 256
#define GMAC0_RX3_SIZE 256
#define GMAC0_RX4_SIZE 64
#define GMAC0_RX5_SIZE 64
#define GMAC0_RX6_SIZE 64

#define GMAC1_RX1_SIZE 1024
#define GMAC1_RX2_SIZE 256
#define GMAC1_RX3_SIZE 256
#define GMAC1_RX4_SIZE 64
#define GMAC1_RX5_SIZE 64
#define GMAC1_RX6_SIZE 64

#define GMAC2_RX1_SIZE 0
#define GMAC2_RX2_SIZE 0
#define GMAC2_RX3_SIZE 0
#define GMAC2_RX4_SIZE 0
#define GMAC2_RX5_SIZE 0
#define GMAC2_RX6_SIZE 0
```

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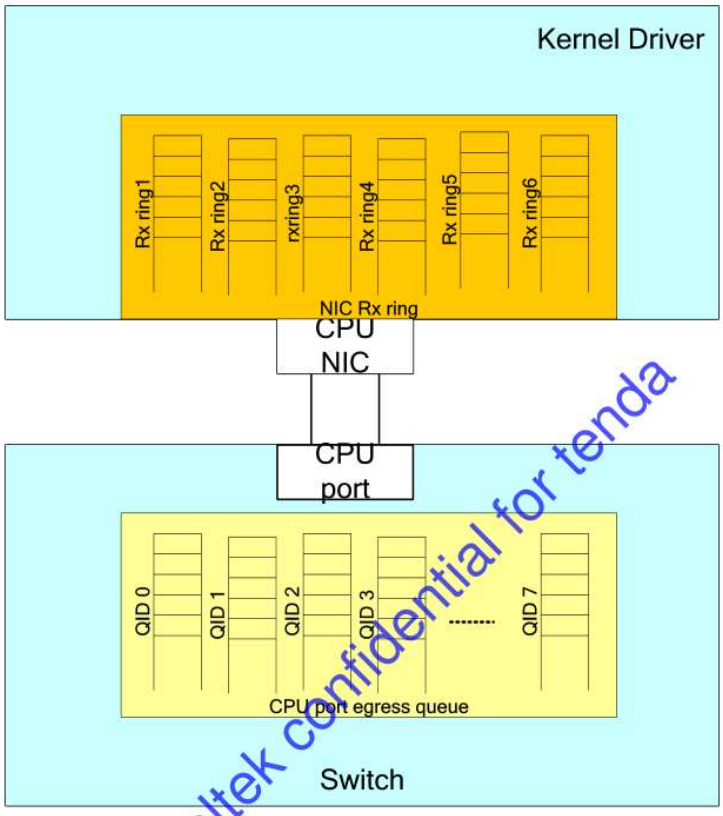
The packet internal priority and RX_RING mapping would be configured by RRING_ROUTING1 register.

RRING_ROUTING1 [3:0]	ring assignment for internal priority 0
RRING_ROUTING1 [7:4]	ring assignment for internal priority 1
RRING_ROUTING1 [11:8]	ring assignment for internal priority 2
RRING_ROUTING1 [15:12]	ring assignment for internal priority 3
RRING_ROUTING1 [19:16]	ring assignment for internal priority 4
RRING_ROUTING1 [23:20]	ring assignment for internal priority 5
RRING_ROUTING1 [27:24]	ring assignment for internal priority 6
RRING_ROUTING1 [31:28]	ring assignment for internal priority 7

The RX_RING value 0, 1 and 7 are means mapping to RING1
2 mapping RING2
3 mapping RING3
4 mapping RING4
5 mapping RING5
6 mapping RING6
For example mapping internal priority 7 to RX_RING6, priority 6 to RX_RING5, priority 5 to

RX_RING4, priority 4 to RX_RING3, priority 3 to RX_RING2, priority 2~2 to RX_RING1 we can set RRING_ROUTING1 to 0x65432000.

RRING_ROUTING1= 0x65432000



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By defaut, Queue0~2 mapping to Rx ring1

Queue3 mapping to Rx ring2

Queue4 mapping to Rx ring3

Queue5 mapping to Rx ring4

Queue6 mapping to Rx ring5

Queue7 mapping to Rx ring6

4.3 rx_info structure

Table 2 rx_info structure

Field Name	Bits	Description
own	1	Don’t care and do not modify
eor	1	Don’t care and do not modify
fs	1	Don’t care and do not modify
ls	1	Don’t care and do not modify
crcerr	1	CRC error. When set, indicates that a CRC error has

		occurred on the received packet.
ipv4csf	1	When set, indicates L3 checksum failure in IPv4 packet . This field is valid for PktType is equal to 1, 2, 3, 4, 5 and 6. This field is 1 for PktType is equal to 0, 7, 8, 9 and a.
l4csf	1	When set, indicates UDP/TCP/ICMP/IGMP checksum failure in IPv4/IPv6 packet . This field is valid for PktType is equal to 3, 4, 5, 6, 8, 9 and a. This field is 1 for pkttype is equal to 0, 1, 2 and 7.
rcdf	1	Indicates rx close dma fail.
ipfrag	1	Indicates this is a IP fragment packet
pppoetag	1	Have PPPoE tag
rwt	1	When set, indicates that the received packet length exceeds 1536(0x600) bytes, and stop receive engine.
data_length	14	This indicates the number of bytes of data on the page pointed by the descriptor. The content of the page should start with no reserve at the start of the page.
cputag	1	Tag Available. When set, the received packet is cputag packet.
ptp_in_cpu_tag_exist	1	Ethenet AV information exists in CPU tag header, GMAC will not remove CPU tag in this case
svlan_tag_exist	1	It indicates the frame format received by NIC. 0b0: SVLAN header is inexistent SVLAN TPID current is 0x88a8 0b1: SLAN header exists
reason	8	Trap Reason
ctagva	1	Tag Available. When set, the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.
cvlan_tag	1	If the packet ‘s TAG (etherType field) is 0x8100, The Ethernet module’ s MAC extracts four bytes from after source ID, sets TAVA bit to1, and moves the TAG value to this field in Rx descriptor.

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		VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canoethernetal Format Indicator.
internal_priority	3	NIC get this field from CPU tag header and uses it to make a RX ring# mapping.
pon_sid_or_extspa	7	When cputag.spa = r_spa_pon(5), this field is cputag.pon_stream_id. When cputag.spa = r_spa_cpu(9/10/7),[6:4] of this field is cputag.ExtSpa. Otherwise, this field is deem as reserved.
l3routing	1	This frame is an intended routed frames.
origformat	1	The received frame by NIC is the original packet's format before switch lookup, switch do not do any modified
src_port_num	4	Receive sourse port number
fb_hash_or_dst_portmask	15	When cputag.reason=FB, this field is flow-based hash index. When cputag.reason!=FB,[6:0] of this field is destination portmask. Switch lookup destination port mask. includes 5 extension ports and 1 CPU bit0 : CPU , bit1~5: extension port 0~4

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4.4 Rx reason code

proc	reason	item	subitem	comment
L2+FB	0	ERR		illegal reason
	1~63	NAT	X	refer L34's document
	64	NAT forward	X	
	65	Invalid ARP	X	
	66~102	reserved	X	

	103	da_mtr	X	host da policing
	104	cvlan_eg	X	cvlan egress filter
	105	svlan_eg	X	svlan egress filter
	106~107	reserved	X	
	108	piso	X	port isolation
	109	mspt_tx	X	spanning tree tx state
	110	da_blk	X	da block function
	111~115	reserved	X	
	116	localpkt	X	local packet filter
	117	cf_permit	X	classification unmatch permit
	118~119	reserved	X	
	120	mirr_iso	X	mirror isolation
	121	mirr_tx	X	mirror tx
	122	mirr_rx	X	mirror rx
	123	to_dspbo_ovr	X	To DSPBO but DSPBO over
	124	reserved	X	
	125	tx_len	X	ingress packet exceed egress length limiation
	126	ep_drop	X	egress drop
	127	link	X	
L2 only	128	ERR		illegal reason
	129~197	reserved	X	
	198	invalid_dualip	X	
	199	err_len_nhs	X	
	200	reserved	X	
	201	unmat_vlan	X	
	202	flood	X	
	203	bc	X	
	204	lut	X	
	205	cvlan_ig	X	
	206	svlan_ig	X	
	207	storm	X	
	208	mspt_rx	X	
	209	lutfull	X	
	210	lrnovr	X	
	211	un_da	X	
	212	unmatch_sa	X	
	213	unknown_sa	X	
	214	mcdata	X	

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	215	resv_trap	X	
	216	v6_icmp_dhcp	X	
	217	dos	X	
	218	illegal_c	X	
	219	igmp	X	
	220	rma	X	
	221	sa_blk	X	source mac blocking
	222	sa_mtr	X	host sa policing
	223	acl mtr	X	
	224	acl permit	X	
	225	oam	X	
	226	rldp	X	rldp forward mask
	227	acl	X	acl rules
	228	cf	X	classification action
	229	mpcp_omci	X	mpcp or omci trap
	230	myrldp	X	rldp from local switch
	231	da_mtr	X	host da policing
	232	cvlan_eg	X	cvlan egress filter
	233	svlan_eg	X	svlan egress filter
	234~235	reserved	X	
	236	piso	X	port isolation
	237	mspt_tx	X	spanning tree tx state
	238	da_blk	X	da block function
	239	reserved	X	
	240	PTP	X	PTP trap/PTP forward
	241		X	PTP rx mirror
	242		X	PTP egress drop/transparent portmask
	243		X	PTP tx mirror
	244	localpkt	X	local packet filter
	245	cf_permit	X	classification unmatch permit
	246	cputag_force	X	
	247	force	X	
	248	mirr_iso	X	mirror isolation
	249	mirr_tx	X	mirror tx
	250	mirr_rx	X	mirror rx
	251	to_dspbo_ovr	X	To DSPBO but DSPBO over
	252	frm_dspbo	X	From DSPBO redirect decision
	253	tx_len	X	ingress packet exceed egress length limiation

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	254	ep_drop	X	egress drop
	255	link	X	

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