RTL9311-CG

LAYER 3 STACKABLE 48*10/100/1000M + 6*10G PORT SWITCH CONTROLLER

DESIGN GUIDE

(CONFIDENTIAL: Development Partners Only)

Rev. 0.3
3 May 2018
Track ID: JATRxxxx-xxxx-xx

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1. General Description

This document provides detailed design and layout guidelines to achieve the best performance when implementing a board design with the RTL9311.

The RTL9311-CG is a layer 3 Stackable Gigabit Ethernet switch device with 108Gbps forwarding bandwidth. The RTL9311-CG is a cost-effective solution for Small-Medium Business (SMB) and Carrier Ethernet Access/Edge applications with wire-speed performance for 48GE+6*10GE platforms.

The device integrates a Dual-Core 1GHz MIPS InterAptive CPU subsystem. It supports a 32-bit data bus. 32M-Byte SPI flash (3-byte mode) or, 64MB SPI flash (4-byte mode), and 2G-Byte DDR3/DDR4 SDRAMs (maximum). An embedded 64KB SRAM can be used for time-sensitive applications. For external CPU connection, PCIe Gen2 is supported.

Notice: Please contact Realtek FAE or Agent FAE before you design the RTL9311. We will help you to review your schematic and layout in sure minimum hardware revision number.

2. General Design and Layout

In order to achieve maximum performance with the RTL9311, good design attention is required throughout the design and layout process. The following recommendations will help implement a high performance system.

2.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits. The following criteria are recommended; power noise of DVDDH/SVDDH/AVDDH/MVDDH/USB_VDDH should be under 30mV and power noise of SVDDL should be under 20mV and AVDDL/DVDDL/DVDDL_CPU/USB_VDDL/PCIE_VDDL/MVDD should be under 30mV.
- Use bulk capacitors (4.7µF-47µF) between each power and ground plane.
- Use 0.1µF decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep decoupling capacitors as close as possible to the RTL9311.
- Fill in unused areas of component side and solder side with solid copper and attach them with vias to the ground plane.
- The IBREF pin of the RTL9311 must connect to GND via a 12K +/- 1% ohm resistor. This resistor must be placed as close as possible to the RTL9311.
- Avoid right angle turns on all traces.
- Recommend using the transformer with common mode chock at IC side for better EMI / ESD performance (see Figure 1).

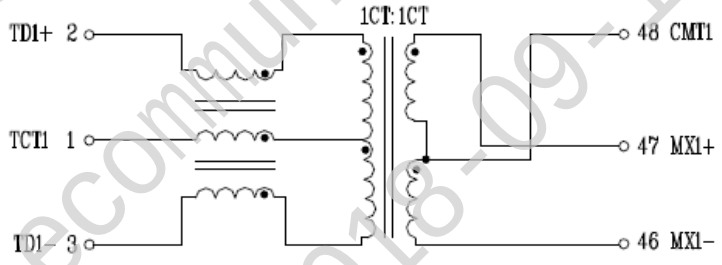

Figure 1. The Transformer with Common Mode chock at IC Side

2.2. Clock Circuits

- Place the crystal as close to the RTL9311 as possible.
- Surround clock traces with ground trace to minimize high-frequency emissions.
- Use a 1.5K pull up external resistor to DVDDH for MDIO.
- Keep the MDC traces away from other signals.
- Keep a clear area under the crystal or OSC component.
- Ensure clock traces have an unbroken reference ground plane.
- All clock traces should use a source termination scheme to reduce the signal reflection and EMI radiation.
- Termination resistors must be as close to the driver side as possible.

2.3. Power Planes

- Divide the power plane into 3.3V, 0.9V, 1.5V (for DDR3) and 1.2V (for DDR4). The details please refer the reference design.
- Use 0.1μF decoupling capacitors and bulk capacitors between each power plane and ground plane.
- Use PI filter circuit for Serdes SVDDCMU, SVDDCK, USB_VDDL and PCIE_VDDL power pins.

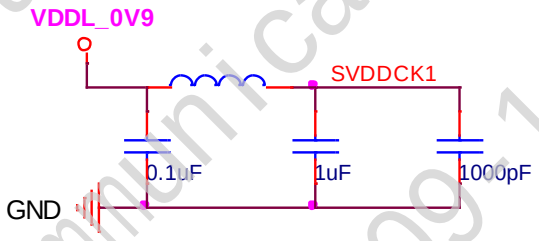

Figure 2 PI Filter Circuit for SVDDCK Power Pins

2.4. Ground Planes

- Keep the ground region under the RTL9311. Avoid too many breaches to achieve good heat conductive ability and a good signal return path.
- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.

2.5. Reset Circuit

At RTL9311, SPI flash and PHY side, we place a circuit of pull-high R 220K and 0.1uF to ground near the reset input pin to avoid noise trigger reset during system ESD test.

But if reset circuit design used AND-gate logic to implement combinational reset, it needs to take care the C load of AND-gate output if meets the AND-gate datasheet requirement. Normal C load requirement of AND-gate is pF order.

For example, if C load used 0.1uF will cause the AND-gate (74LVC08A) output has glitch signal, and has the risk of system boot-up fail.

3. SERDES Layout Guidelines

As the SFI/XSGMII/QSGMII transmits over 10.3125Gbps/10.3125Gbps/5Gbps differential signal pairs, the PCB layout needs some attention in order to meet layout guidelines. The following lists some important guidelines for layout of the SFI/XSGMII/QSGMII.

3.1. General Guide

- All Serdes trace must be laid on the top side of a 4-layer PCB, and cannot pass through via.
- Recommend ground shielding for Serdes TX & RX differential pairs. Clearance between signal and ground least 30 mils in a 4-layer PCB.
- As possible to space to all other signals is at least 30 mils in order to avoid harmful coupling issues in a 4-layer PCB.

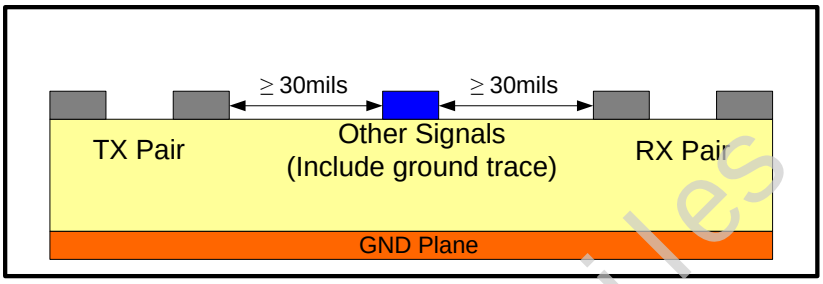

Figure 3. Trace Spacing Recommendation for a 4-Layer PCB

- Differential pairs should maintain symmetry between the two signals of a differential pair whenever possible.

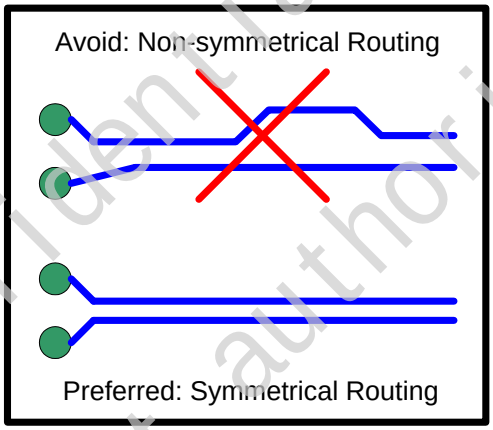

Figure 4 Symmetrical Routing

- Trace routes over long distances should be routed at an off-angle to the X-Y axis of a PCB layer to distribute the effects of fiber glass bundle weaves and resin-rich areas of the dielectric.

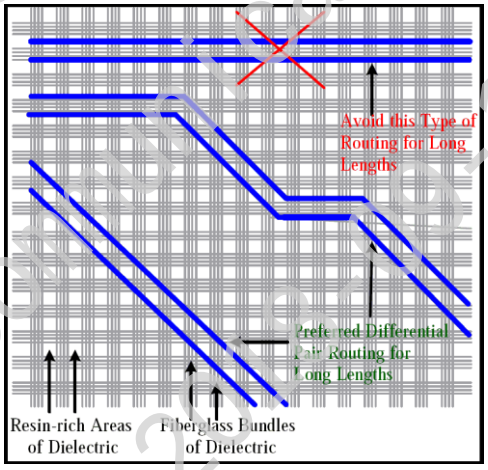

Figure 5 Long Trace Layout for Serdes

- Differential pairs should have a continuous reference plane, and avoid via.
- Size 0402 AC coupling capacitors are strongly encouraged as the smaller the package size, the less ESL.
- Place AC coupling capacitors near output pins of differential pairs.
- Locate capacitors for coupled traces at the same location along the differential traces.

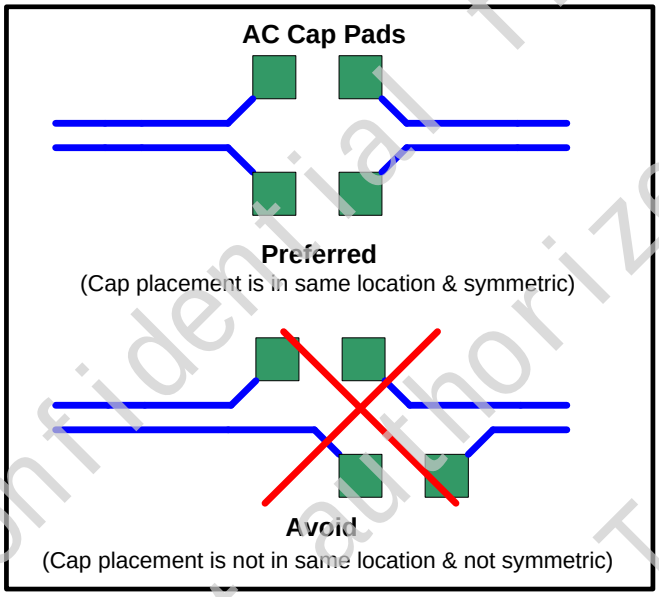

Figure 6 Symmetrical Routing Into AC Capacitors

3.2. QSGMII Layout Guide

- Differential pair impedance for QSGMII is 100Ω ± 10%.
- QSGMII trace length not over 20-inch in a 4-layer of normal FR4 PCB.
- QSGMII differential pairs P/N trace in PCB mismatch cannot over 60 mils. If in-pair length matching is not possible, serpentine routing (zig-zag of a shorter trace) is acceptable.

3.3. SFI/XSGMII Layout Guide

- Differential pair impedance for SFI/XSGMII is 100Ω ± 10%.
- SFI trace length is required to follow below rules for SFF-8431 testing:
  - SFI host interconnect budget SDD21 at 5.5GHz is between -6.5dB and -2.5dB (SDD21 is defined from chip pads to SFP+ connector). The minimum channel transfer SDD21 (maximum

loss) is given by:

$$SDD21(dB) = -0.73 \quad \text{f from 0.01 GHz to 0.25 GHz}$$

$$SDD21(dB) = (-0.108 - 0.845 \times \sqrt{f} - 0.802 \times f) \quad \text{f from 0.25 GHz to 7 GHz}$$

$$SDD21(dB) = 20 - 4 \times f \quad \text{f from 7 GHz to 8 GHz}$$

$$SDD21(dB) \geq -16 \quad \text{f from 8 GHz to 11.1 GHz}$$

where *f* is the frequency in GHz.

- The reflection coefficients, SDD11 and SDD22, of the SFI channel are recommend to meet following equations:

The reflection coefficients, SDD11 and SDD22, of the SFI channel are recommended to meet the following equations:

$$SDDxx(dB) \leq -14.5 \quad \text{f from 0.01 to 5 GHz}$$

$$SDDxx(dB) \leq -23.25 + 8.75 \times \left(\frac{f}{5}\right) \quad \text{f from 5 to 11.1 GHz}$$

where *f* is the frequency in GHz and SDDxx is either SDD11 or SDD22.

- Recommend SFI PCB trace length maximum is 2.5-inch in a 4-layer of normal FR4 PCB when using 2x2 or 2x1 SFP+ cage for SFF-8431 testing.
- Recommend SFI PCB trace length maximum is 3.5-inch in a 4-layer of normal FR4 PCB when using single SFP+ cage for SFF-8431 testing.
- Recommend SFI PCB trace length minimum is 1.5-inch in a 4-layer of normal FR4 PCB when using 2x2 or 2x1 or single SFP+ cage for SFF-8431 testing.

- XSGMII trace length minimum is 1.5-inch, and maximum is 15-inch in a 4-layer of normal FR4 PCB.
- SFI differential pairs P/N trace in PCB mismatch cannot over 10 mils. If in-pair length matching is not possible, serpentine routing (zig-zag of a shorter trace) is acceptable. The length matching compensation should be made as close as possible to the point where the length variation occurs. The serpentine routing trace cannot over 100 mils. Recommend circular arc bend for serpentine routing trace.
- XSGMII differential pairs P/N trace in PCB mismatch cannot over 30 mils. If in-pair length matching is not possible, serpentine routing (zig-zag of a shorter trace) is acceptable. The length matching compensation should be made as close as possible to the point where the length variation occurs. The serpentine routing trace cannot over 100 mils. Recommend circular arc bend for serpentine routing

trace.

- Recommend arc turn and oblique line for SFI/XSGMII trace.
- Minimize impedance mismatch between transmission lines & mounting pads for SFI/XSGMII PCB layout:
  - ➢ Use smallest mounting pad size if possible.
  - ➢ Partially void the reference layer (~60%) to reduce the capacitance.

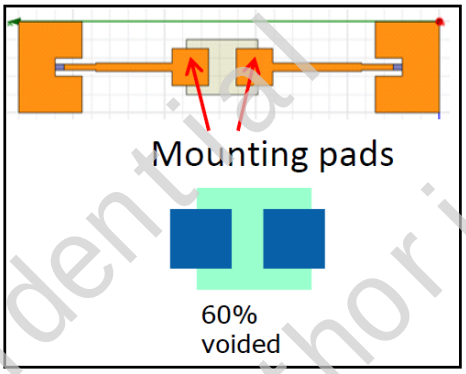

Figure 7 SFI/XSGMII Layout Rules for AC Coupling Capacitors

- The biggest discontinuity of impedance occurs at the connector; use ground voiding under the connector footprint to mitigate the effect. The void for Tx & Rx differential pair pins of SFP+ connector is shown below.

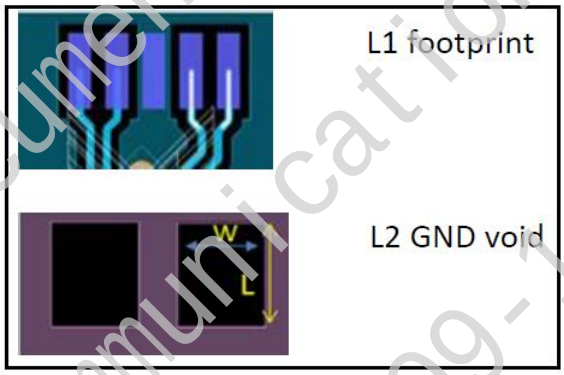

Figure 8 SFP+ Connector Footprint Voiding

3.4. USB Layout Guide

- Each differential pair traces should be routed with 90 Ω ±10 % differential impedance.
- The intra-pair skew of each pair, including Package and PCB, should be less than 30mil and serpentine line is

NOT allowed.

- USB trace length no longer than 12inches.

3.5. PCIE Layout Guide

- Differential pair impedance for PCIE is 100Ω ± 10%.

4. DRAM Layout Guidelines

DDR3 and DDR4 will run up to 1600Mbps. The following PCB layout guidelines should be followed.

- DRAM signal traces should be kept as short as possible and no more than 2 vias.
- The suggested longest trace length for D0-D31 / DM0-DM3 / DQS_P/N0-3 is not over 1100 mils, allowing no more than a 300-mil delta between the lengths of per-DRAM.
- The suggested longest trace length for all Address/Command is not over 5000 mils, allowing no more than a 2500-mil delta between the lengths of per-DRAM.
- Match the length of both sets of the differential pairs (CK_P/N, DQS_P/N0-3), allowing no more than a 50-mil delta between the lengths of the two signals.
- For all address/command signals should use a source termination resistor and must be as close to the driver side as possible.
- Source termination resistors must be as close to the driver side as possible.
- The layout topology of CLKP/N, CSN and CKE signals are Fly-by topology.
- Differential-pair impedance is 100Ω±10%, single-ended impedance is 55Ω±10% in 4-layer PCB.
- Only DDR chip need a 240 ohm+/-1% resistor and must be connected between the ZQ pin and ground.
- RTL9311 ZQ , ZQ_VREF and DQ_VREF pins must be floating.
- For all add/cmd and DQx signals traces must be refer to GND plane, not PWR plane.
- For all add/cmd and DQx signals layout topology is GSSG, the spacing between two signals must be larger 3 times of signal width.

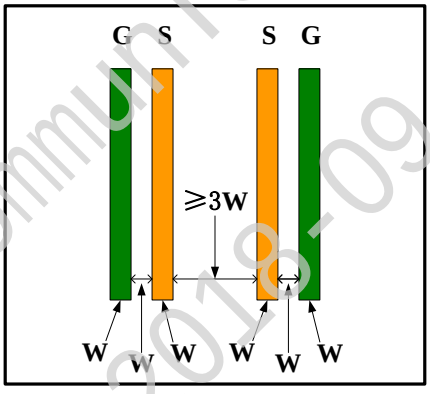

Figure 9 The spacing between two signals must be larger 3W

- DRAM VREF pins must be dealt as following figure to reduce the ripple of voltage.

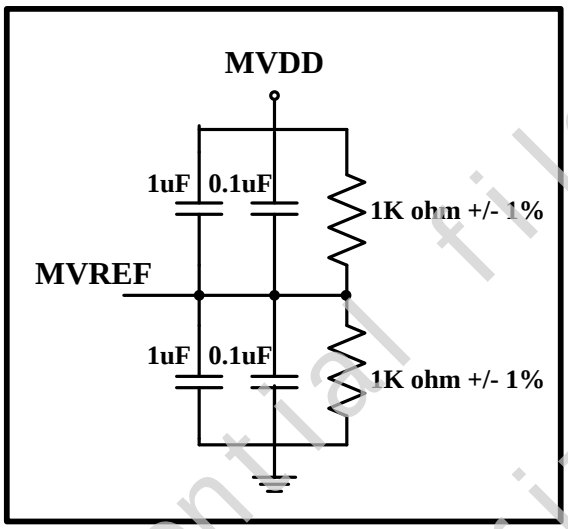

Figure 10 The Scheme for DRAM VREF Pins

- The MCK_P/N pins must be dealt as following figure to adjust the amplitude of MCK_P/N and filter noise.

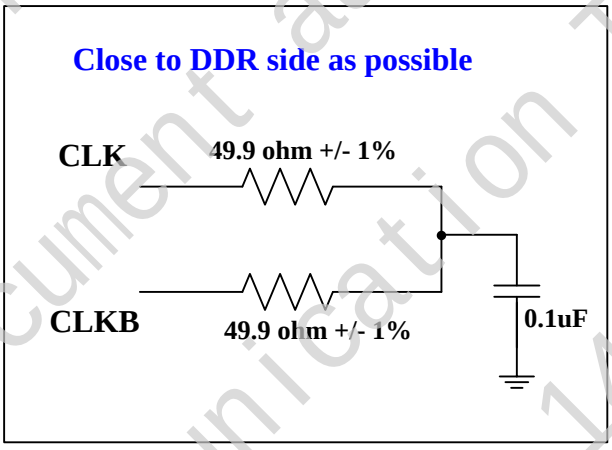

Figure 11 The Scheme for CLK/CLKB Pins

5. SPI Flash Interface

The SPI Flash interface will run up to 100MHz. The following PCB layout guidelines should be followed.

- SPI Flash clock trace should avoid passing through via if possible.
- SPI Flash signal trace should be kept as short as possible.

- Surround the SPI Flash clock traces with ground trace to minimize high-frequency emissions if possible.
- Use the termination resistors for EMI, and the termination resistors must be as close to the driver side as possible.

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