RTL9301-CG

LAYER 3 MANAGED 24*10/100/1000M + 4*10G PORT SWITCH CONTROLLER

DESIGN GUIDE

(CONFIDENTIAL: Development Partners Only)

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REVISION HISTORY

Revision	Release Date	Summary
0.1	2017-11-27	Draft

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1. General Description

This document provides detailed design and layout guidelines to achieve the best performance when implementing a 4-layer board design with the RTL9301.

The Realtek RTL9301 is a highly integrated Layer3 switch supporting Energy Efficient Ethernet (EEE). It has up to 24-port Gigabit and 4-port 10G Ethernet MAC. It also provides 4 pairs of 8Gbps SerDes interface to connect with another RTL9301 to extend to 48 ports Gigabit UTP and 4 ports 10G FIB Ethernet transceivers. There are two mode selections in the RTL9301. One is 24*10/100/1000Base-T + 4*10G Base-R; the other is 48*10/100/1000Base-T + 4*10G Base-R.

The RTL9301 is embedded with an up to 800MHz MIPS-34Kc CPU. It supports a 32-bit data bus, 32M-Byte SPI flash (3-byte mode) or, 64MB SPI flash (4-byte mode), and 1G-Byte DDR3 SDRAMs (maximum). An embedded 64KB SRAM can be used for time-sensitive applications. For connecting to an external CPU, it supports the SGMII interface.

Notice: Please contact Realtek FAE or Agent FAE before you design the RTL9301. We will help you to review your schematic and layout in sure minimum hardware revision number.

2. General Design and Layout

In order to achieve maximum performance with the RTL9301, good design attention is required throughout the design and layout process. The following recommendations will help implement a high performance system.

2.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits. The following criteria are recommended; power noise of DVDDH/DVDDIO_Gx(x=0,1,2,3)/DVDD_MDXx(x=0,1,2,3)/AVDDH_USB/AVDDH_PLLx(x=0,1,2)/AVDDH_CEN/AVDDH_XTAL/SVDDH should be under 100mV and power noise of SVDDL/AVDDL_USB/AVDDL_DLL/AVDDL_CK/AVDDL_PLLx(x=0,1,2)/AVDDL_CEN/DVDDL/MDVDDH should be under 50mV
- Verify the critical components, such as clock source and transformer, to meet the application requirements
- Use bulk capacitors (4.7μF-47μF) between each power and ground plane
- Use 0.1μF decoupling capacitors to reduce high-frequency noise on the power and ground planes
- Keep decoupling capacitors as close as possible to the RTL9301
- Fill in unused areas of component side and solder side with solid copper and attach them with vias to the ground plane
- The IBREF pin of the RTL9301 must connect to GND via a 2.49K +/- 1% ohm resistor. This resistor must be placed as close as possible to the RTL9301
- Avoid right angle turns on all traces
- Recommend using the transformer with common mode chock at IC side for better EMI / ESD performance (see Figure 1)

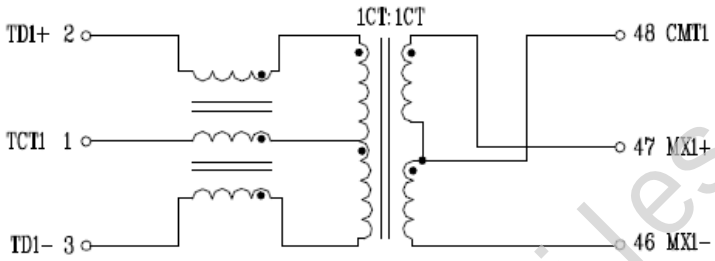

Figure 1. The Transformer with Common Mode chock at IC Side

2.2. Clock Circuits

- Place the crystal as close to the RTL9301 as possible
- Surround clock traces with ground trace to minimize high-frequency emissions
- Use a 1.5K pull up external resistor to DVDD_MDXx for MDIO.
- Keep the MDC traces away from other signals
- Keep a clear area under the crystal or OSC component
- Ensure clock traces have an unbroken reference ground plane
- All clock traces should use a source termination scheme to reduce the signal reflection and EMI radiation
- Termination resistors must be as close to the driver side as possible

2.3. Power Planes

- Divide the power plane into 3.3V, 1.1V and 1.5V, 3.3V power plane for DVDDH/DVDDIO_Gx(x=0,1,2,3)/DVDD_MDXx(x=0,1,2,3)/AVDDH_USB/AVDDH_PLLx(x=0,1,2)/AVDDH_CEN/AVDDH_XTAL/SVDDH. 1.1V power plane for SVDDL/AVDDL_USB/AVDDL_DLL/AVDDL_CK/AVDDL_PLLx(x=0,1,2)/AVDDL_CEN/DVDDL. 1.5V power plane for MDVDDH
- Use 0.1μF decoupling capacitors and bulk capacitors between each power plane and ground plane
- Use Pi filter for the power of AVDDL_CK

2.4. Ground Planes

- Keep the ground region under the RTL9301. Avoid too many breaches to achieve good heat conductive ability and a good signal return path
- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board
- Place a moat (gap) between the system ground and chassis ground

2.5. Reset Circuit

At RTL9301 and SPI flash side, we place a circuit of pull-high R 220K and 0.1uF to ground near the reset input pin to avoid noise trigger reset during system ESD test.

But if reset circuit design used AND-gate logic to implement combinational reset, it needs to take care the C load of AND-gate output if meets the AND-gate datasheet requirement. Normal C load requirement of AND-gate is pF order.

For example, if C load used 0.1uF will cause the AND-gate(74LVC08A) output has glitch signal, and has the risk of system boot-up fail.

2.6. Reserved GPIO for SFP+

While planning the RTL9301 system design with SFP+, the LOS/SDA/SCL/MOD_ABS pins of SFP+ connector must connect to GPIO pins.

- Connect GPIO to LOS pin:

  If CPU detect the LOS is low, it will execute 10G SerDes rx calibration to optimize 10G SerDes performance.

- Connect GPIO to SDA/SCL pins:

  It provides CPU to judge the fiber transceiver which plug-in is 1G or 10G mode since the SerDes parameters for these two transceivers is different.

- Connect GPIO to MOD_ABS pin:

  It provides the signal of fiber module present for CPU.

2.7. PWRMON Electrical Specification

RTL9301 support OAM dying gasp function, and it monitor the voltage level of PWRMON pin to check if it meet OAM dying gasp conditions.

The electrical specification for PWRMON pins is shown below:

- Trigger condition: voltage is under 1.2V~ 1.3V
- Normal state: voltage must be above 1.55V, and in the range of 1.55V~3.3V

3. Serdes Layout Guidelines

As the SFI+/XSGMII/QSGMII transmits over 10.3125Gbps/10.3125Gbps/5Gbps differential signal pairs, the PCB layout needs some attention in order to meet layout guidelines. The following lists some important guidelines for layout of the SFI+/XSGMII/QSGMII.

3.1. General Guidelines

- All SFI+/ XSGMII/QSGMII must be laid on the top side of a 4-layer PCB, and cannot pass through a via
- Recommend ground shielding for Serdes TX & RX differential pairs
- As possible to space to all other signals be at least 30-mil in order to avoid harmful coupling issues in a 4-layer PCB (see Figure 2)

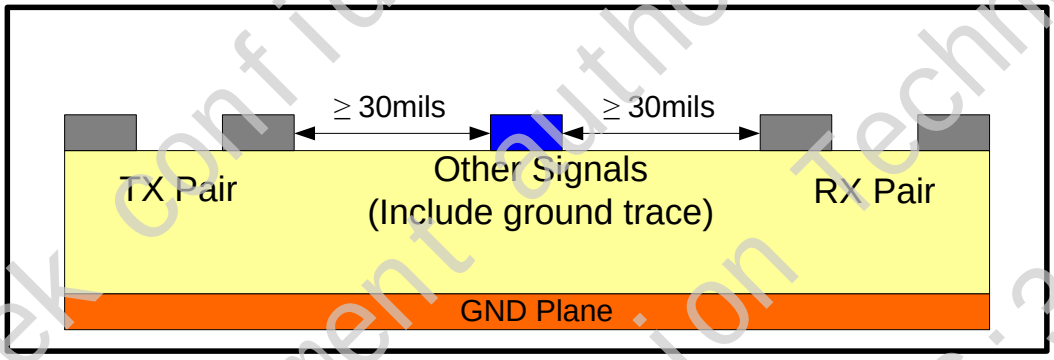

Figure 2. Trace Spacing Recommendation for a 4-Layer PCB

- Differential pairs should maintain symmetry between the two signals of a differential pair whenever possible.

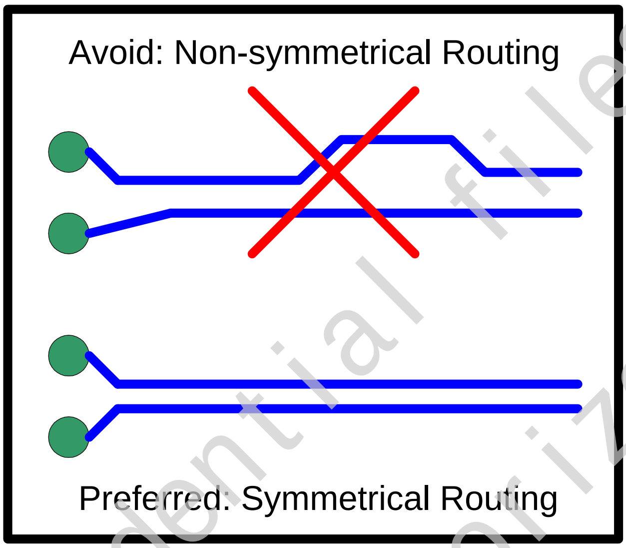

Figure 3. Symmetrical Routing

- Trace routes over long distances should be routed at an off-angle to the X-Y axis of a PCB layer to distribute the effects of fiber glass bundle weaves and resin-rich areas of the dielectric

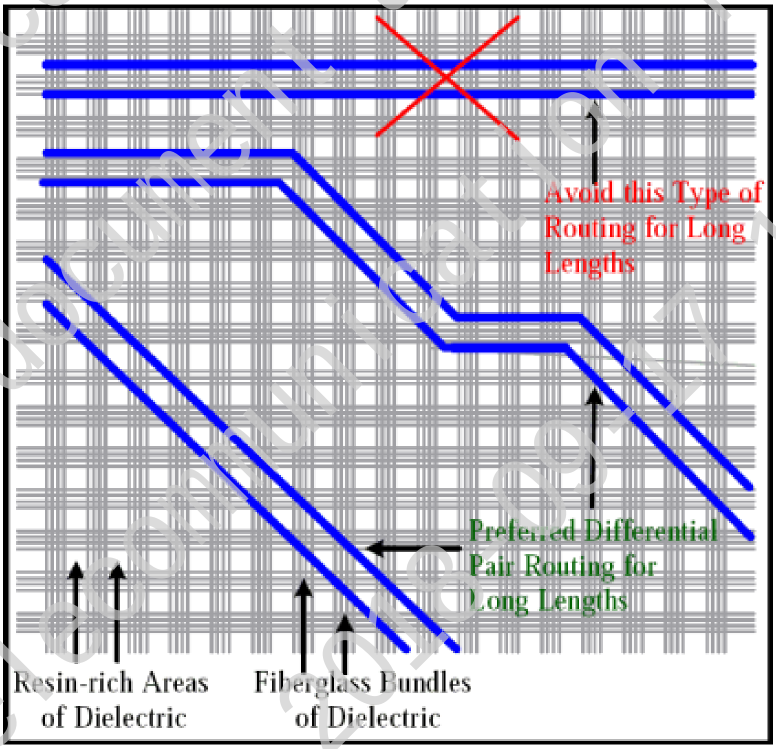

Figure 4. Long Trace Layout for Serdes

- Differential pairs should have a continuous reference plane, and avoid via
- Size 0402 AC coupling capacitors are strongly encouraged as the smaller the package size, the less ESL
- Place AC coupling capacitors near output pins of differential pairs
- Locate capacitors for coupled traces at the same location along the differential traces

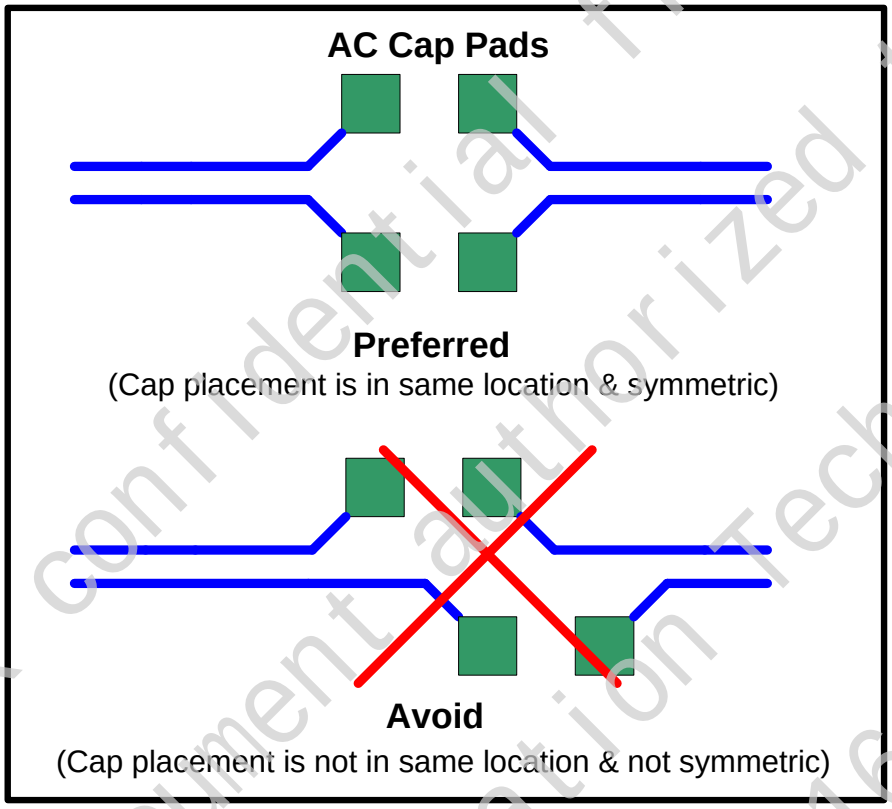

Figure 5. Symmetrical Routing Into AC Capacitors

3.2. QSGMII Layout Guidelines

- Differential pair impedance for QSGMII is 100Ω ± 10%
- QSGMII trace length is required to follow the bellow rule:
  - Trace length not over 15-inch in a 4-layer of normal FR4 PCB
- QSGMII differential pairs P and N trace in PCB total mismatch cannot over 60 mils. If total length matched within 60 mils, avoid serpentine routing.

3.3. SFI/XSGMII Layout Guidelines

- Differential pair impedance for SFI/XSGMII is 100Ω ± 10%
- SFI trace length is required to follow one of the bellow rules:
  - Trace length must be between 2 inches and 5 inches in a 4-layer of normal FR4 PCB
  - PCB trace insertion loss not over -5dB @5.15625GHz
- XSGMII trace length is required to follow the bellow rule:
  - Trace length not over 10-inch in a 4-layer of normal FR4 PCB
- Differential pairs P and N trace in substrate and PCB total mismatch cannot over 10mils for SFI interface (Connected to Fiber Module/DAC) or 20mils for XSGMII interface (Connected to other chip directly). If total length matched within 10 mils or 20mils, avoid serpentine routing. If total length matched over 10 mils or 20mils, serpentine routing is acceptable. The length matching compensation should be made as close as possible to the point where the length variation occurs, for example, near chip pins. Minimize the length of the serpentined sections as much as possible. SFI/XSGMII trace length in substrate:

Table 1 SFI/XSGMII trace length in substrate

Ball No.	Pin Name	Substrate Total Trace Skew Pos vs Neg (mil)
AG23	HSOP_S2	-5
AF23	HSON_S2	
AG25	HSIP_S2	-6
AF25	HSIN_S2	
AD26	HSOP_S3	2
AD27	HSON_S3	
AB26	HSIP_S3	1
AB27	HSIN_S3	
V27	HSOP_S4	1
V26	HSON_S4	
T27	HSIP_S4	1
T26	HSIN_S4	
P26	HSOP_S5	1
P27	HSON_S5	
M26	HSIP_S5	0
M27	HSIN_S5	

Ball No.	Pin Name	Substrate Total Trace Skew Pos vs Neg (mil)
K27	HSOP_S6	1
K26	HSON_S6	
H27	HSIP_S6	0
H26	HSIN_S6	
F26	HSOP_S7	0
F27	HSON_S7	
D26	HSIP_S7	0
D27	HSIN_S7	
A25	HSOP_S8	6.6
B25	HSON_S8	
A23	HSIP_S8	6
B23	HSIN_S8	
B21	HSOP_S9	6
A21	HSON_S9	
B19	HSIP_S9	6
A19	HSIN_S9	

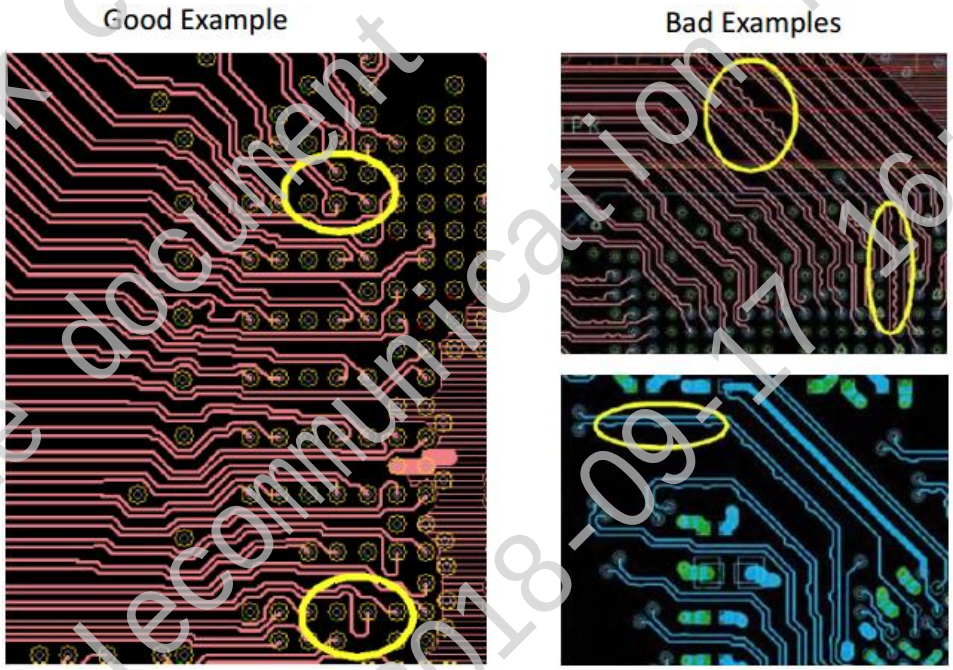

Figure 6. Length Matching and Compensation Example

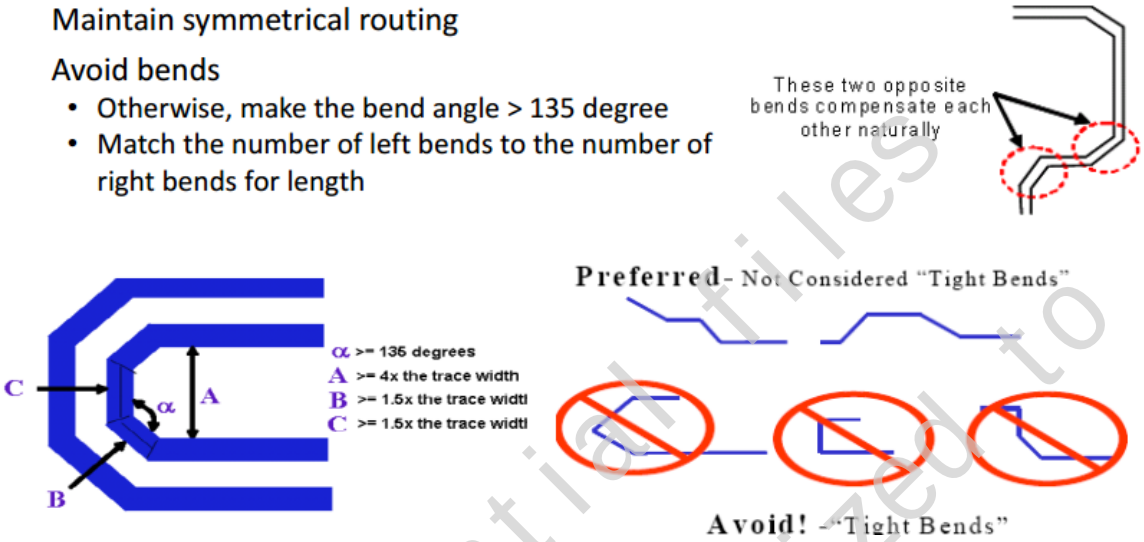

Figure 7. Bend Rule Example

- Recommend arc turn and oblique line for SFI/XSGMII trace
- Minimize impedance mismatch between transmission lines & mounting pads for SFI+/XSGMII PCB layout:

  1. Use smallest mounting pad size if possible.
  2. Partially void the reference layer (~60%) to reduce the capacitance. (see Figure 8)

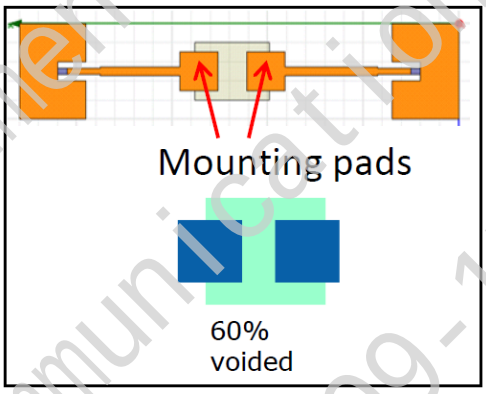

Figure 8. SFI+ Layout Rules for AC Coupling Capacitors

- The biggest discontinuity of impedance occurs at the connector; use ground voiding under the connector footprint to mitigate the effect. The void for tx & rx differential pair pins of SFP+ connector is shown in Figure 9

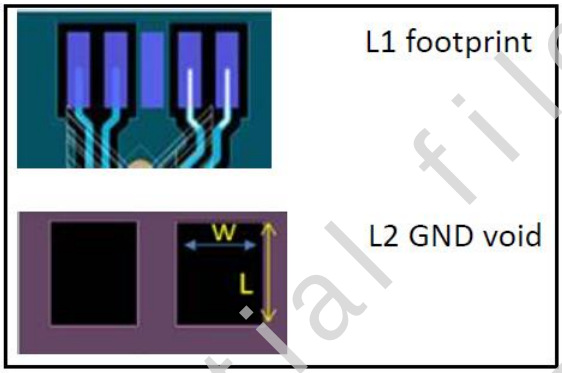

Figure 9. SFP+ Connector Footprint Voiding

4. USB Guidelines

- Differential pair impedance for USB is 90Ω ± 10%

5. DDR3 PCB Layout Guidelines

- DDR3 will run up to 600Mbps. The following PCB layout guidelines should be followed
- DDR3 signal traces should be kept as short as possible
- The suggested longest trace length for MD0-MD15 / MLDM / MHDM / MLDQS_P/N / MHQDS_P/N is not over 1.6-inch
- The suggested longest trace length for MA0-MA15 / BA0-BA2 / MRAS# / MCAS# / MWE# / MCS# / MCKE / MCK_P/N / MRST# / MODT is not over 2.5-inch
- Match the length of both sets of the differential pairs (MCK_P/N / MLDQS_P/N / MHQDS_P/N), allowing no more than a 100-mil delta between the lengths of the two signals
- MA0-MA15 / BA0-BA2 / MRAS# / MCAS# / MWE# / MCS# / MCKE / MCK_P/N / MRST# / MODT should use a source termination resistor
- Termination resistors must be as close to the driver side as possible
- Recommend differential-pair impedance is 100Ω±10%, single-ended impedance is 55Ω±10% in 4-layer PCB
- A 240 ohm+/-1% resistor must be connected between the MZQ pin and ground
- Use the TOP side of the PCB for DDR3 signal traces, and do not use vias

- DDR3 layout reference for a 4-layer PCB:

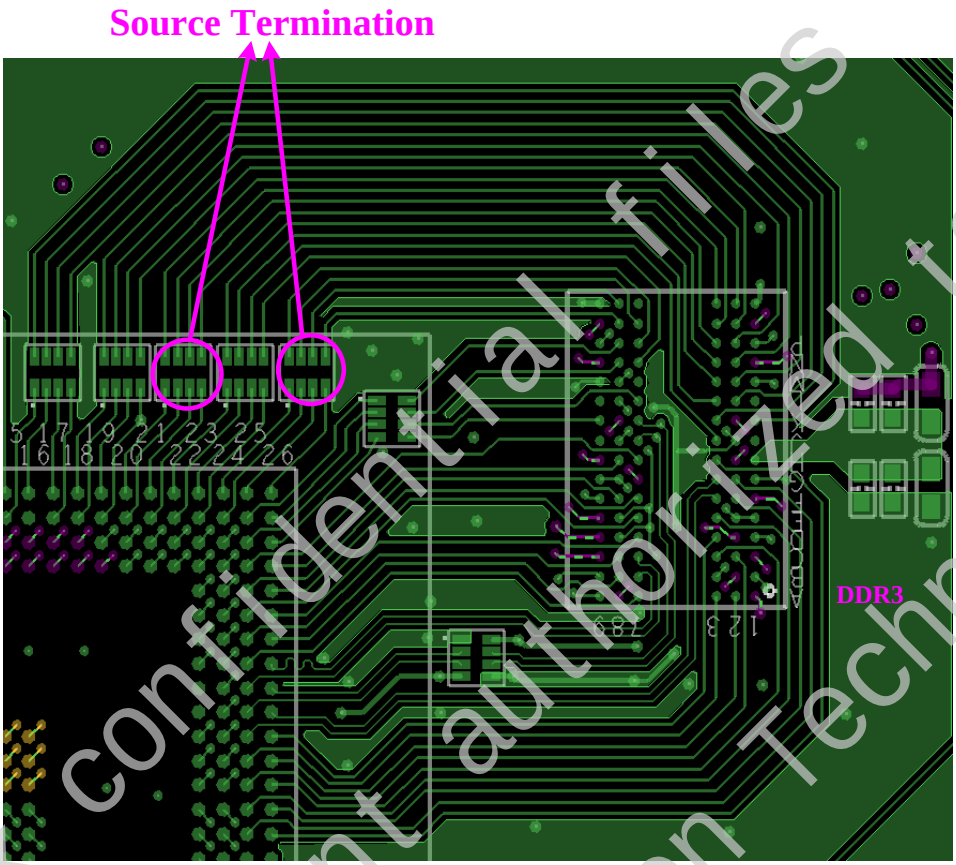

Figure 10. DDR3 Layout Reference for 4-Layer PCB

- The MVREF pin must be dealt as following figure to reduce the ripple of voltage

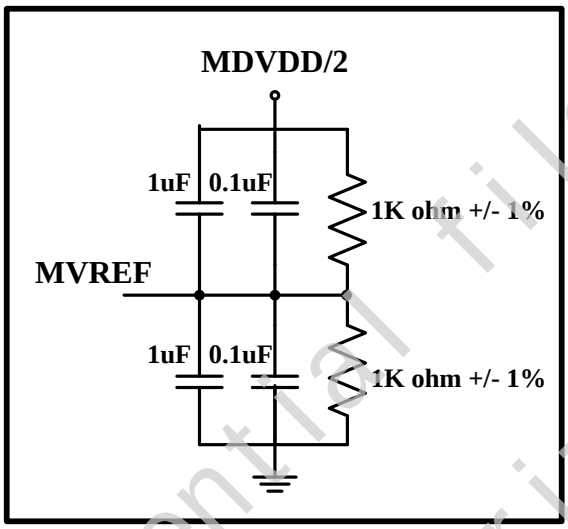

Figure 11. The Scheme for MVREF Pin

- The MCK_P/N pins must be dealt as following figure to adjust the amplitude of MCK_P/N and filter noise.

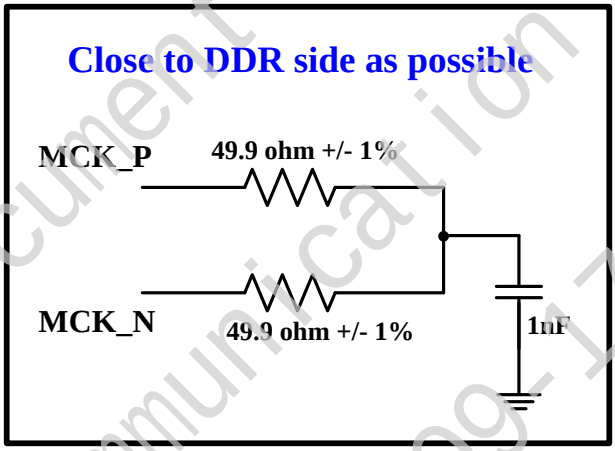

Figure 12. The Scheme for MCK_P/N Pins

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