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RTL8411

PCI EXPRESS 10/100/1000M ETHERNET CONTROLLER WITH INTEGRATED 1-LUN CARD READER CONTROLLER

EEPROM-LESS APPLICATION NOTES

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2011/08/09	First release.
1.1	2011/09/01	Revised section 3 LAN MAC Address Programming, page 1.
1.2	2011/10/04	Revised section 4 SID/SVID Programming (If Necessary), page 2. Revised section 7 Serial Number, page 6.
1.3	2011/11/02	Added section 4 SID/SVID Programming (If Necessary), page 2. Added section 5 SDIO Enabling/Disabling, page 2.

Table of Contents

List of Tables

1. Introduction

This application note helps board designers to implement an EEPROM-less Realtek PCI-E RTL8411 10/100/1000M Ethernet board design. The interaction between the BIOS and driver are highlighted and discussed.

2. Design Considerations

Several major points must be considered when designing an EEPROM-less feature for Realtek's single chip PCI-E RTL8411 10/100/1000M Ethernet controller. Those points are listed below and are detailed in the following sections.

- LAN MAC Address Programming
- SID/SVID Programming (If Necessary)
- LED Mode Configuration
- Serial Number
- PXE Driver

3. LAN MAC Address Programming

Due to the EEPROM-less design goal, the LAN MAC address cannot be loaded from EEPROM and stored in the RTL8411. The BIOS must provide the MAC address to the RTL8411 each boot time. The RTL8411 will hold the MAC address until AC power is off (pulling the PCI reset low will not release the MAC address)

If the MAC address is 001122334455h:

Step1: Write C0h to I/O register offset 0x50 by byte access to disable 'register protection'

Step2: Write 33221100h to I/O register offset 0x00 via double word access

Step3: Write 00005544h to I/O register offset 0x04 via double word access

Step4: Write 33221100h to I/O register offset 0x70 via double word access

Step5: Write 8000F0E0h to I/O register offset 0x74 via double word access

Step6: Write 00005544h to I/O register offset 0x70 via double word access

Step7: Write 800030E4h to I/O register offset 0x74 via double word access

Step8: Write 00h to I/O register offset 0x50 via byte access to enable 'register protection'

Note: When the RTL8411 resumes from S3, S4, or S5, the BIOS must complete the steps given above.

4. SID/SVID Programming (If Necessary)

4.1. Ethernet Controller

The default SID/SVID value of the RTL8411 Ethernet Controller is 8168/10EC. To change the value, follow the steps below.

If SID=8168h, SVID=10ECh:

Step1: Write 816810ECh to I/O register offset 0x64 via double word access

Step2: Write 8002F02Ch to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

Note: When the RTL8411 resumes from S3, S4, or S5, the BIOS must complete the steps given above.

4.2. Card Reader

The default SID/SVID value of the RTL8411 Card Reader is 5289/10EC. To change the value, follow the steps below.

If SID=5289h, SVID=10ECh:

Step1: Write 528910ECh to I/O register offset 0x64 via double word access

Step2: Write 8000F02Ch to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

Note: When the RTL8411 resumes from S3, S4, or S5, the BIOS must complete the steps given above.

5. SDIO Enabling/Disabling

Due to the EEPROM-less design goal, the Secure Digital IO (SDIO) cannot be enabled/disabled from EEPROM and stored in the RTL8411. The SDIO default setting is disabled.

To enable SDIO, follow the steps below.

Step1: Write 000000FFh to I/O register offset 0x64 via double word access

Step2: Write 80001724h to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

To disable SDIO, follow the steps below.

Step1: Write 000000FBh to I/O register offset 0x64 via double word access

Step2: Write 80001724h to I/O register offset 0x68 via double word access

Step3: Wait for 1ms

Note: When the RTL8411 resumes from S3, S4, or S5, the BIOS must complete the steps given above.

6. Customizable LED Configuration

The RTL8411 supports customizable LED operation modes via IO register offset 18h~19h. Table 1 describes the different LED actions.

Table 1. LED Select (IO Register Offset 18h~19h)

Bit	Symbol	RW	Description
15:12	LEDCntl	RW	LED Feature Control
11:8	LEDSEL3	RW	LED Select for PINLED3
7:4	LEDSEL1	RW	LED Select for PINLED1
3:0	LEDSEL0	RW	LED Select for PINLED0

When implementing customized LEDs:

Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x0CA9h (0000110010101001b), the LED actions are:

- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 3: On only in 1000M mode, with blinking during TX/RX

Table 2. Customized LEDs

Speed	LINK			ACT/Full
	Link 10M	Link 100M	Link 1000M	
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 3	Bit 8	Bit 9	Bit 10	Bit 11
Feature Control	Bit 12	Bit 13	Bit 14	Bit 15

Note: There are two special modes:
LED OFF Mode: Set all bits to 0. All LED pin output become floating (power saving).
Fixed LED Mode: Set Option 1 LED table Mode: LED0=LED1=LED2=1 or 2 (see Table 3).

Table 3. Fixed LED Mode

Bit31~Bit0 Value	LED0	LED1	LED2
1XXX 0001 0001 0001	ACT	LINK	Full Duplex + Collision
1XXX 0010 0010 0010	Transmit	LINK	Receive

Note: 'X' indicates 'irrelevant'.

Table 4. LED Feature Control-1

Feature Control	Bit12	Bit13	Bit14	Bit15
0	LED0 Low Active	LED1 Low Active	LED2 Low Active	Indicates Option 1 of Table 6 is selected
1	LED0 High Active	LED1 High Active	LED2 High Active	Indicates Option 2 of Table 6 is selected

Table 5. LED Feature Control-2

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Option 1 (see Table 6): Selected Speed LINK+ Selected Speed ACT Option 2 (see Table 6): Selected Speed LINK+ All Speed ACT

Table 6. LED Option 1 & Option 2 Settings

Link Bit			Active Bit	Description		
10	100	1000		Link	Option 1 LED Activity	Option 2 LED Activity
0	0	0	0	LED Off		
0	0	0	1	-	Act^{10}+Act^{100}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
0	0	1	0	$Link^{1000}$	-	-
0	0	1	1	$Link^{1000}$	Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
0	1	0	0	$Link^{100}$	-	-
0	1	0	1	$Link^{100}$	Act^{100}	Act^{10}+Act^{100}+Act^{1000}
0	1	1	0	$Link^{100}$+$Link^{1000}$	-	-
0	1	1	1	$Link^{100}$+$Link^{1000}$	Act^{100}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
1	0	0	0	$Link^{10}$	-	-
1	0	0	1	$Link^{10}$	Act^{10}	Act^{10}+Act^{100}+Act^{1000}
1	0	1	0	$Link^{10}$+$Link^{1000}$	-	-
1	0	1	1	$Link^{10}$+$Link^{1000}$	Act^{10}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}
1	1	0	0	$Link^{10}$+$Link^{100}$	-	-
1	1	0	1	$Link^{10}$+$Link^{100}$	Act^{10}+Act^{100}	Act^{10}+Act^{100}+Act^{1000}
1	1	1	0	$Link^{10}$+$Link^{100}$+$Link^{1000}$	-	-
1	1	1	1	$Link^{10}$+$Link^{100}$+$Link^{1000}$	Act^{10}+Act^{100}+Act^{1000}	Act^{10}+Act^{100}+Act^{1000}

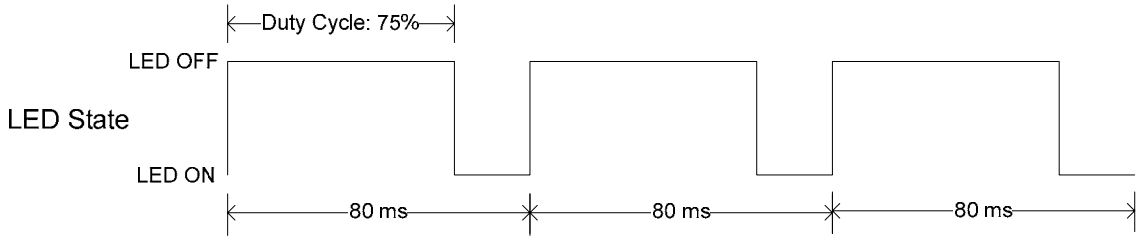
Note:
Act^{10} = LED blinking when Ethernet packets transmitted/received at 10Mbps.
Act^{100} = LED blinking when Ethernet packets transmitted/received at 100Mbps.
Act^{1000} = LED blinking when Ethernet packets transmitted/received at 1000Mbps.
$Link^{10}$ = LED lit when Ethernet connection established at 10Mbps.
$Link^{100}$ = LED lit when Ethernet connection established at 100Mbps.
$Link^{1000}$ = LED lit when Ethernet connection established at 1000Mbps.

6.1. LED Blinking Frequency and Duty Cycle Control

The RTL8411 supports LED blinking frequency control via IO register offset 1Ah to control user's LED blinking frequency and duty cycle (see Table 7). If the IO offset 0x1A is 0x0B (00001011b), the LED blinking frequency is 80ms and the duty cycle is 75%. The LED State is shown in Figure 1.

Table 7. LED Blinking Frequency Control (IO Offset 1Ah)

Bit	RW	Description
3:2	RW	LED Blinking Frequency 0: 240ms 1: 160ms (Default) 2: 80ms 3: Link Speed Dependent
1:0	RW	LED Blinking Duty Cycle 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%



Note: Assume the LED is in low active.

Figure 1. LED Blinking Frequency Example

7. Serial Number

Due to the EEPROM-less design goal, the serial number cannot be loaded from EEPROM and stored in the RTL8411. The BIOS must provide the serial number to the RTL8411 each boot time.

If the serial number is 00E04C6812345678h:

Step1: Write 684CE000h to I/O register offset 0x64 via double word access.

Step2: Write 8002F164h to I/O register offset 0x68 via double word access.

Step3: Wait for 1ms.

Step4: Write 78563412h to I/O register offset 0x64 via double word access.

Step5: Write 8002F168h to I/O register offset 0x68 via double word access.

Step6: Wait for 1ms.

Note: When the RTL8411 resumes from S3, S4, or S5, the BIOS must complete the steps given above.

8. PXE Driver

If the board layer designer wants to enable a Preboot Execution Environment (PXE) driver, the BIOS needs to write one byte of the PXE parameters in the I/O register 0xF0 to allow the ROM code to run properly. The default value of the PXE parameter is 00h (disable PXE). PXE parameter details are listed below.

Note: When the RTL8411 resumes from S3, S4, or S5, the BIOS must complete the steps given above.

Table 8. PXE Parameters

Bit	Symbol	RW	Description
7:6	Boot Protocol	RW	00: PXE protocol 01: RPL protocol
5:4	Boot order	RW	00: ROM disable 01: Int 18h 10: Int 19h 11: PnP/BEV (BBS)
3:0	-	-	Reserved

Note: When the EEPROM-less feature is implemented, the RTL8411 cannot WOL from '1st AC power-on'.

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