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RTL838x

MULTI-LAYER MANAGED 10/26/28*10/100/1000M-PORT SWITCH CONTROLLERS

Design&Layout guide

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211 Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL838x chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2012-8-24	First Release
1.1	2013-2-5	1. Change the DDR2/3 maximum operating rate from 393MHZ to 300MHZ. 2.Add a new item for DDR2/3 " Len CMD/ADDR/CTL Group >= Len CK_P/N >= Len DATA Group(DQS_P/N, DM, DQ) is recommended.
1.2	2013-3-18	1. Add the note: "In order to meet the DDR12 and DDR3 trace, the order of their pins and pin name are not the same, so please during the particles you used to select the correct net name."
1.3	2013-5-29	1. Delete the "single-ended impedance is 60Ω±6%" of the Serdes impedance rule; 2. Modify the function of RTL8380M to 10-port 10/100/1000 switch controller.
1.4	2013-11-28	1. Change the tolerance of between Serdes difference pair length to 50mil.
1.5	2016-10-28	1.Add some solutions to improve the ability of ESD/EMI.

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1. General Description

The RTL8380x are new generation Gigabit switches supporting Energy Efficient Ethernet (EEE). The RTL8380M is a 10-port 10/100/1000M switch controller, and the RTL8382M/RTL8382L is 28-port 10/100/1000 switch controllers. All of them have an 8-port 10/100/1000M Ethernet PHY embedded. The RTL838x is provided via a 55nm CMOS process in an LQFP-216 E-PAD package. The Memory interface of the RTL8380M/RTL8382M support DDR1/DDR2/DDR3 and SPI Flash. The RTL8382L supports only SPI Flash.

The RTL8380M supports two interfaces of SGMII or 1000Base-X.

The RTL8382M/RTL8382L support four pairs of serially connected QSGMII interface ports to connect to two Octal Gigabit PHYS (RTL8218B). The RTL8382M/RTL8382L also supports one serially connected QSGMII interface port to connect to 1 Quad Gigabit PHY (RTL8214FC).

The RTL838x have an embedded 500MHz MIPS-4KEc CPU that supports a 32MByte (max.) SPI flash (Only the RTL8380M/RTL8382M support DDR1/DDR2/DDR3). Two 16C550 compatible UARTS are integrated for low speed serial data, and one E-JTAG is supported for on-chip debugging.

There are 8K entries in the 4-way hash L2 table for MAC address learning and searching. The RTL838x supports two hash algorithms. An independent 512-entry Multicast table supports Layer 2 and IP multicast functions.

The RTL838x adopts advanced technologies such as Realtek Cable Test (RTCT), Automatic loop detection and prevention (RLPP/RLDP), Attack Prevention, and MAC Address Learning Constraints.

Notice: Please contact Realtek FAE or Agent FAE before you design the RTL838x.We will help you to review your schematic and layout in sure minimum hardware revision number.

2. General Design and Layout

In order to achieve maximum performance with the RTL838x good design attention is required throughout the design and layout process. The following recommendations will help implement a high performance system.

2.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits. The following criteria are recommended; power noise of DVDDH/SVDDH/AVDDH should be under 100mV and power noise of DVDDL/SVDDL/AVDDL /MVDDH should be under 50mV.
- Verify the critical components, such as clock source and transformer, to meet the application requirements.
- Keep ground noise levels below 50mV.
- Use bulk capacitors between each power and ground plane.
- Use decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep decoupling capacitors as close as possible to the RTL838x.
- Put the bypass capacitors of RTL838x/RTL8218B VDDL/AVDDL/SVDDL power pins on the top layer, and keep the distance between the capacitors and the power pins as short as possible.
- Fill in unused areas of top side and bottom side with solid copper and attach them with via to the ground plane.
- The transformer should be placed as close as possible to the RTL838x.
- The RJ-45 phone jack should be placed as close as possible to the transformer.
- Avoid right angles on all traces.
- Keep trace in the top layer and avoid layer change if possible.
- The MDIREF pin 21 of RTL838x must connect to GND via 2.49K±1% Ohm resister. This resister must be put as close as possible to RTL838x.
- The MDIREF pin of the RTL8218B must connect to GND via a 2.49K±1%Ohm resister. This resister must be put as close as possible to RTL8218B.

3. Clock Circuit

- Keep the trace between the crystal PIN and RTL838x clock PIN(pin 105,106) less than 800mil,and the spacing of XI and XO greater than 8mil (see figure 1).
- Surround the clock with ground trace to minimize high-frequency emissions if possible.
- Use only one 1.5K pull up external resistance to 3.3V for MDIO.
- Keep the MDC trace away from the other signals, to avoid unnecessary interference.
- Keep clearance area under the crystal or OSC component.
- Ensure clock traces have an unbroken reference ground plane (see Figure 1).
- All clock traces should use a source damping scheme to reduce the signal reflection and EMI radiation.
- Damping resistors must be as close to the driver side (output) as possible.
- Always try routing GND trace adjacent to high speed and sensitive signal(e.g. CKOUT (25M) (see Figure 2)；MDC，MDIO（see Figure3 Figure4）)

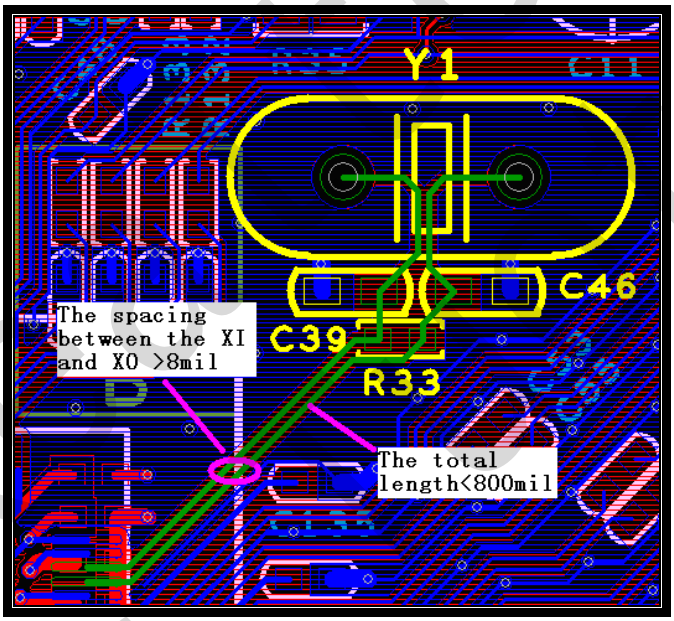

Figure 1 . The clock traces recommended moves

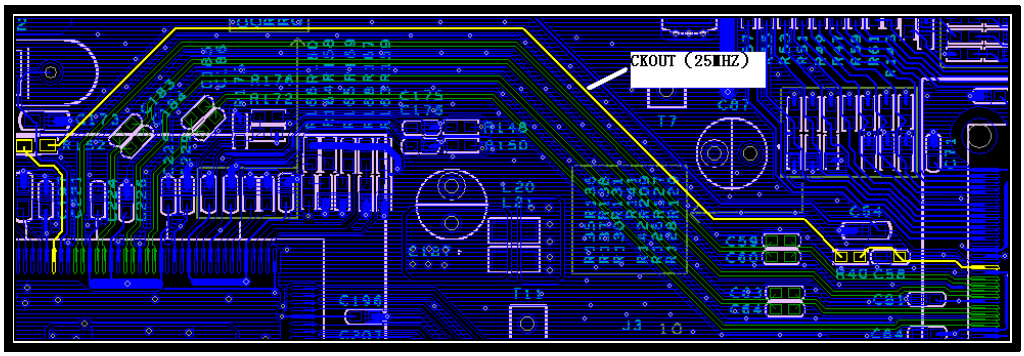

Figure 2. Place GND net adjacent to CKOUT (25M) signal routing trace

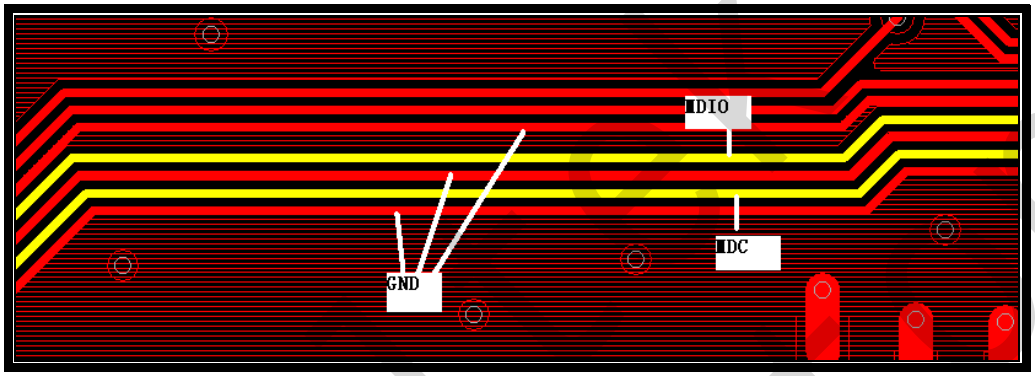

Figure 3. Place GND net adjacent to MDIO /MDC signal routing traces (1)

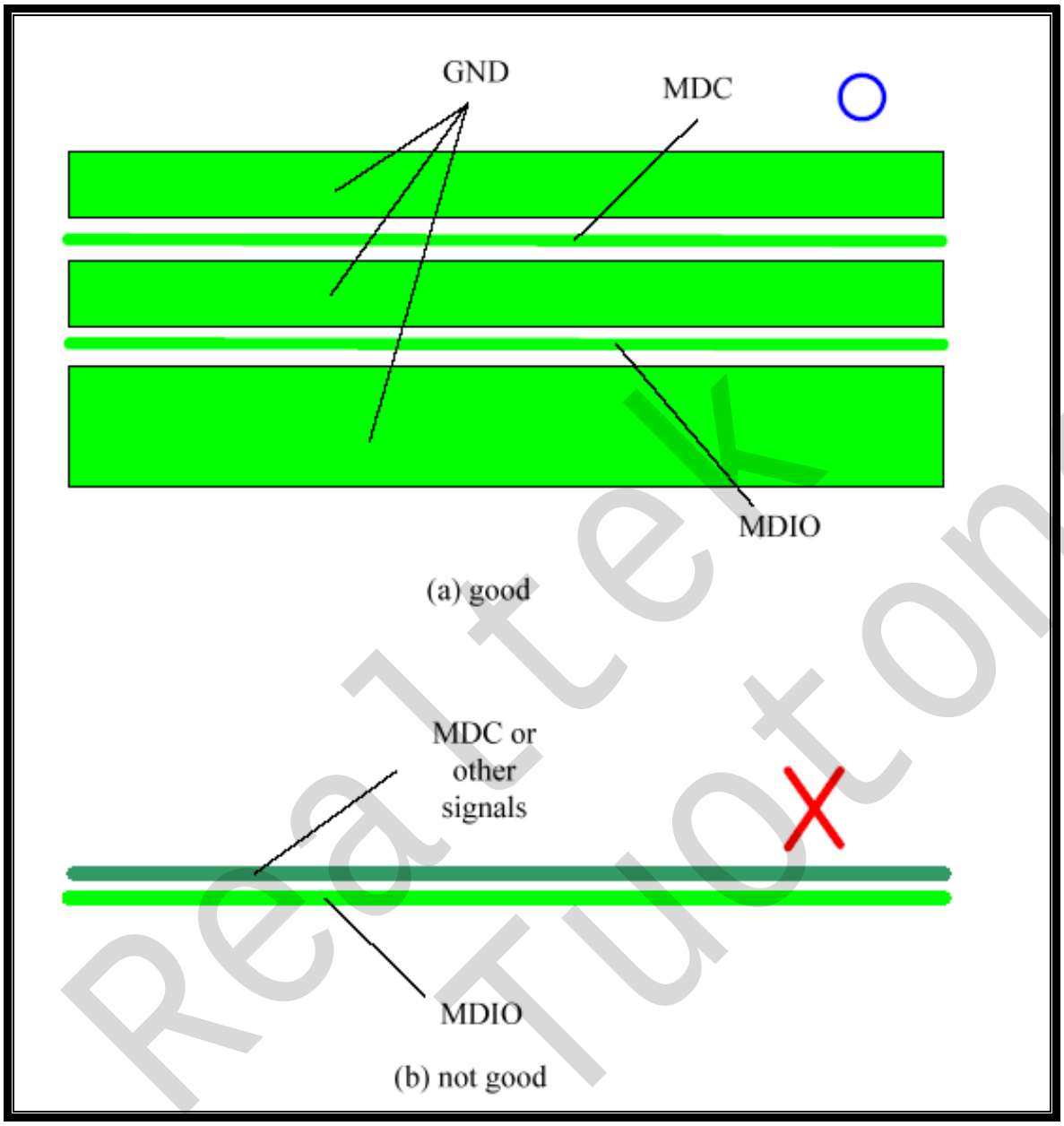

Figure 4. Place GND net adjacent to MDIO signal routing traces (2)

4. Reset Circuit

If reset circuit design used AND-gate logic to implement combinational reset, it needs to take care the C load of AND-gate output if meets the AND-gate datasheet requirement. Normal C load requirement of AND-gate is pF order.

For example, if C load used 0.1uF will cause the AND-gate(74LVC08A) output has glitch signal, and has the risk of system boot-up fail.

5. Reserved GPIO for Combo Port Application

While planning the system design with combo/fiber port, the LOS or MOD-DEF(0) of SFP connector must be connected to the GPIO pins.

- Connect GPIO to LOS pin:

It provides the signal of received optical power is below the worst-case receiver sensitivity for CPU.

- Connect GPIO to MOD-DEF(0) pin:

It provides the signal of fiber module present for CPU.

6. RTL8214FC/18FB for SFP Application

In RTL8214FC and RTL8218FB, there are four dedicated pins FX0_TX_DIS ~ FX3_TX_DIS for SFP to control SFP optical transmitter on and off.

If RTL8382M system design has the fiber ports requirement with RTL8214FC/18FB, the TX_DISABLE pin of SFP must connect to RTL8214FC/18FB. In addition, we recommend the TX_DISABLE pin of SFP pull high to 3.3V with 4.7Kohm to prevent some OE modules that does not built-in the pulled up resistor.

7. Power Planes (Mainly for 2-Layer PCB)

1) Use 0.1μF decoupling capacitors and bulk capacitors between each power and ground.
2) Keep the power trace in the top layer with might and main.(See Figure 5)

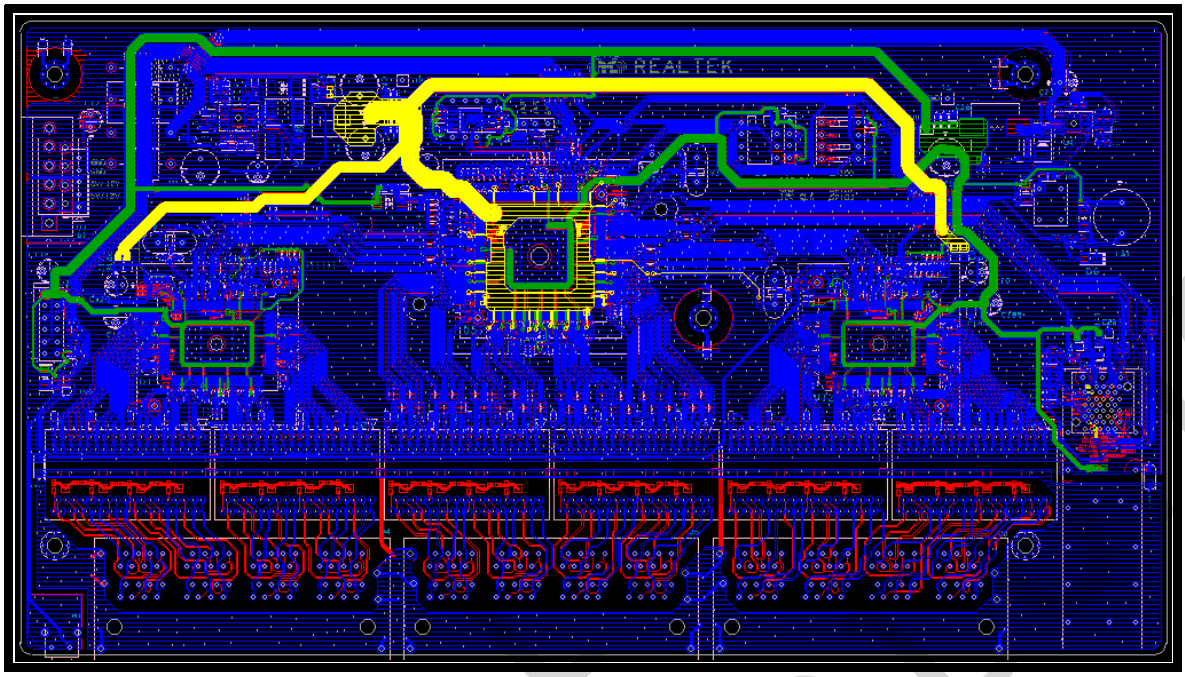

Figure 5. Power Planes

3) For each RTL8218B, add two 100uF/16v bulk capacitors at the VDDL and VDDH power line input point of each RTL8218B.that will help to reduce the VDDL power noise during EEE state on/off.

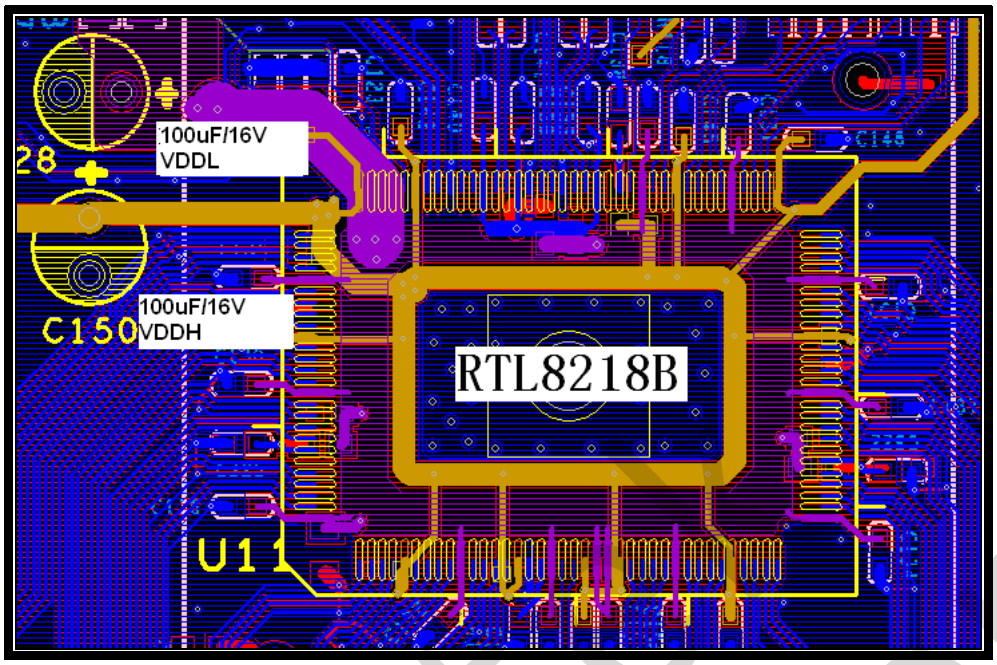

Figure 6. The Left side of RTL8218B

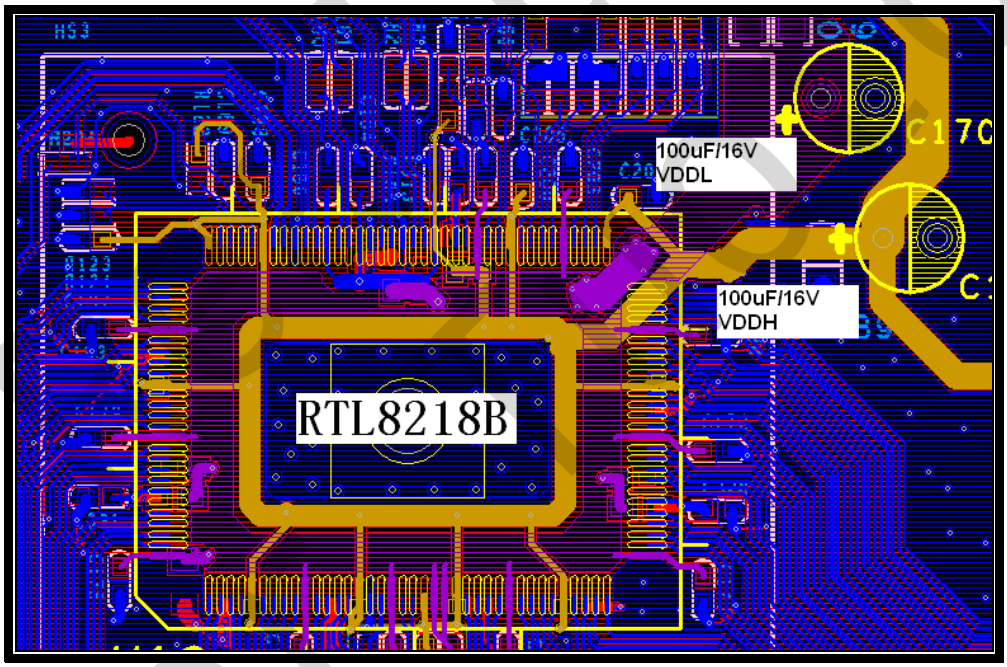

Figure 7. The Right side of RTL8218B

4) When design 2L PCB for 24G Switch system, connects the regulator output source to the VDDL of RTL838x first. Then connects a wide power trace, at least 300mil.that will help to reduce the voltage drop cased to narrow power line resistance.

5) Place at least two 470uF/16V bulk capacitors at the VDDL switching regulator output and 100uF/16V bulk capacitors at the VDDL power input point for each chip, at least one 470uF/16V bulk capacitors at the VDDH switching regulator output and 100uF/16V bulk capacitors at the VDDH power input point of each chips. As shown in figure 8.

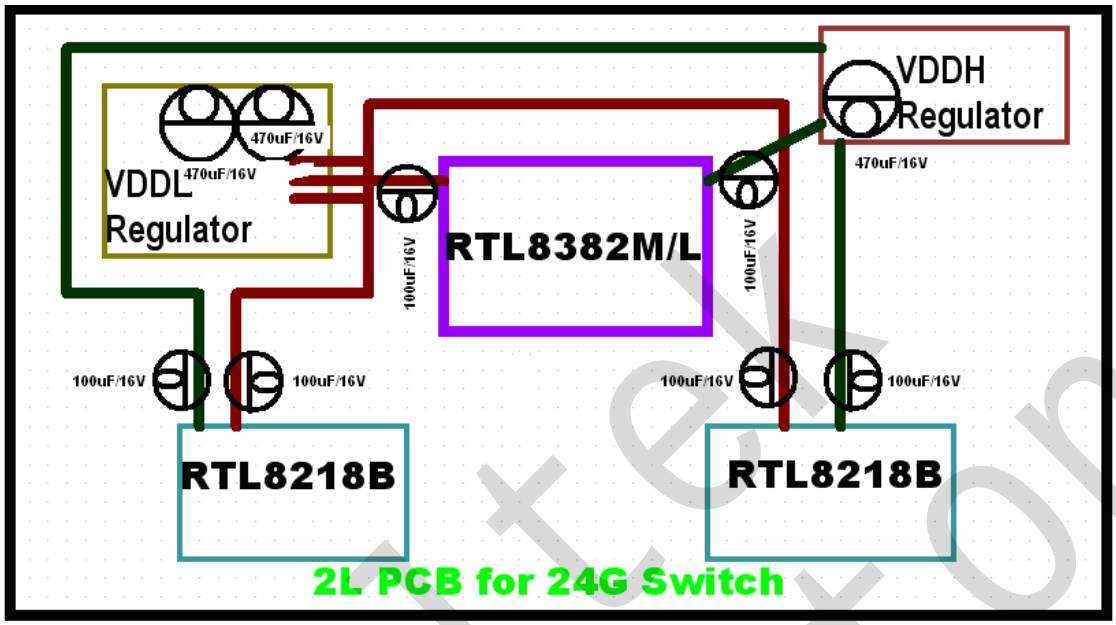

Figure 8. System VDDL/VDDH Trace connect Diagram

8. Ground Planes (Mainly for 2-Layer PCB)

- Keep the ground region under the RTL838x.Avoid too many branches to achieve good heat conductive ability and a good signal return path.
- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board (see Figure 9).
- Place a moat (gap) between the system ground and chassis ground at least 80-mil.

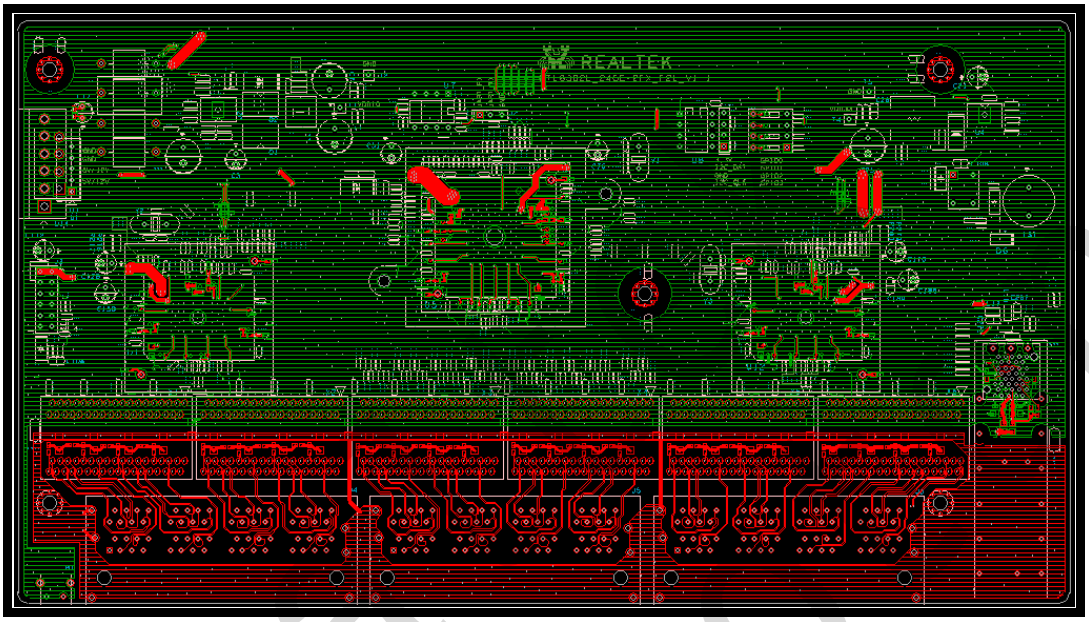

Figure 9. GND Plane on bottom side in 2-layer PCB

9. Serdes PCB Layout Guidelines

As the Serdes transmits over 5 Gbps differential signal, the PCB layout needs some attention in order to meet layout guidelines. The following lists some important guidelines for layout of the Serdes in a 2-layer PCB.

1) Differential impedance is 100Ω±10%.
2) All Serdes signal must be laid on the top side of the 4-layer or 2-layer PCB, and cannot pass through a vias.
3) All micro-strip traces of a differential pair should be 5-mil-wide with 7-mil-wide air-gap spacing between the traces of the pair in a 4-layer PCB.
4) Spacing to all other signals should be at least 30mil in order to avoid harmful coupling issues in a 4-layer PCB.

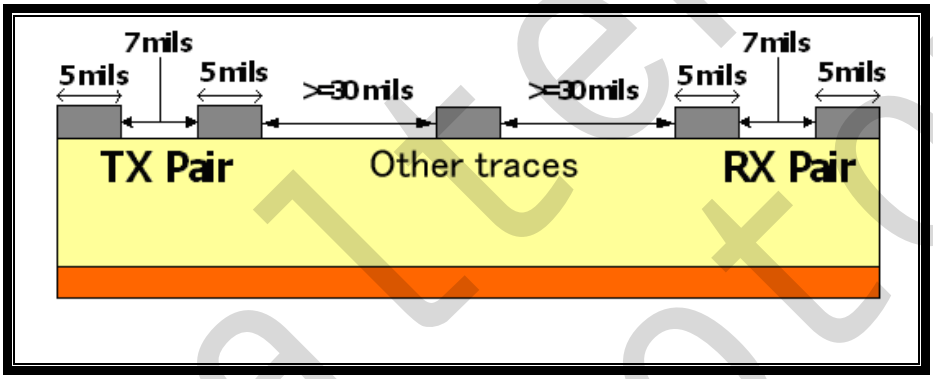

Figure 10. Serdes Trace Width and Spacing Recommendation for a 4-Layer PCB

5) All micro-strip traces of a differential pair should be 7mil/5mil/7mil or 6mil/6mil/6mil (width/spacing/width) between the traces of the pair in a 2-layer PCB. The two moves are both feasible, Can choose in accordance with the recommendations of the PCB factory (see Figure 11/12).

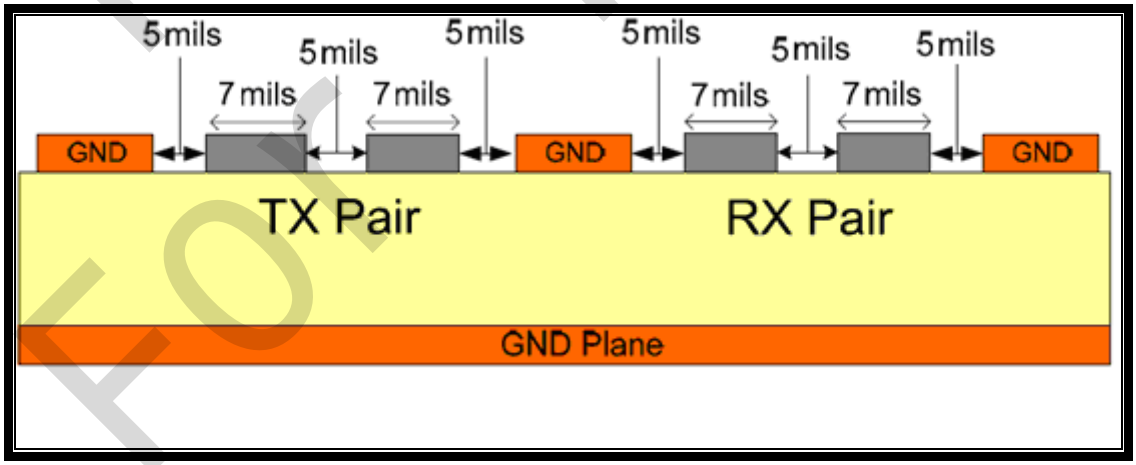

Figure 11. Serdes Trace Width and Spacing Recommendation for a 2-Layer PCB (1)

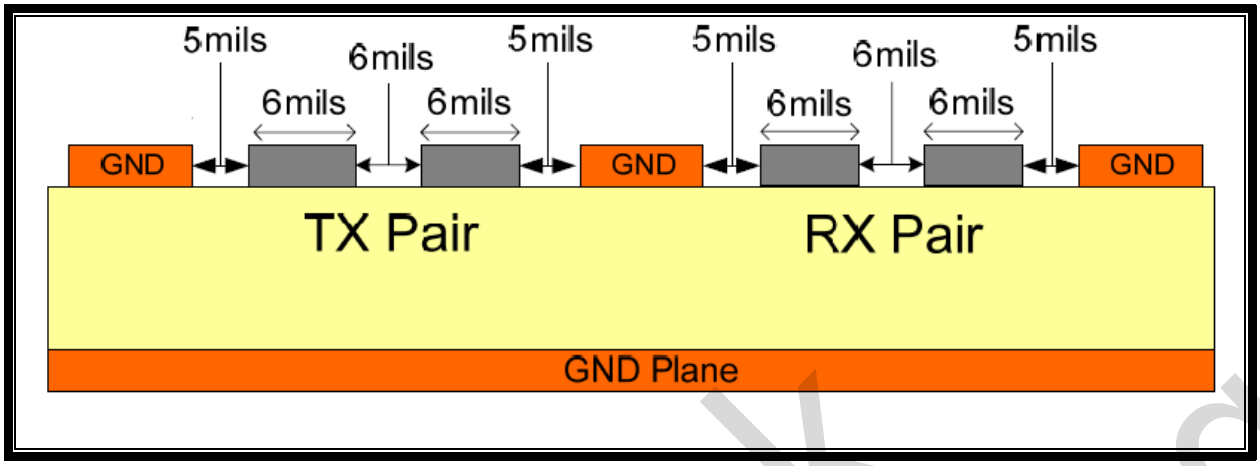

Figure 12. Serdes Trace Width and Spacing Recommendation for a 2-Layer PCB (2)

6) Both sides of the TX pair and RX pair should have a ground trace, and the ground trace should be attached with multiple vias to the ground plane in a 2-layer PCB (see Figure 13).

7) In a 2-layer PCB, the width of ground trace between QSGMII differential pair should be at least 30mils (see Figure 13).

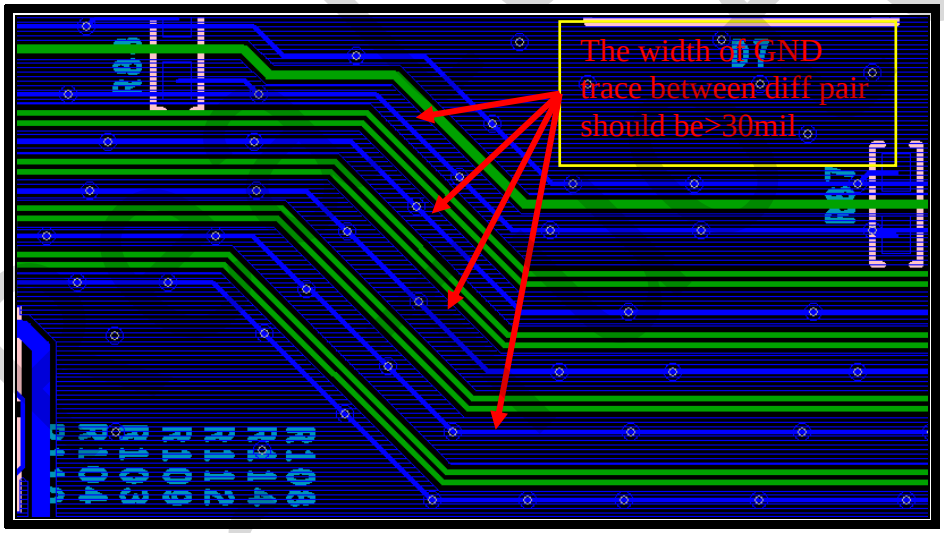

Figure 13. Minimum with GND trace between diff pair in 2L PCB

8) In a 2-layer PCB, to avoid routing QSGMII differential pair(top side) overlapped with other signal(bottom side) (see Figure 14)

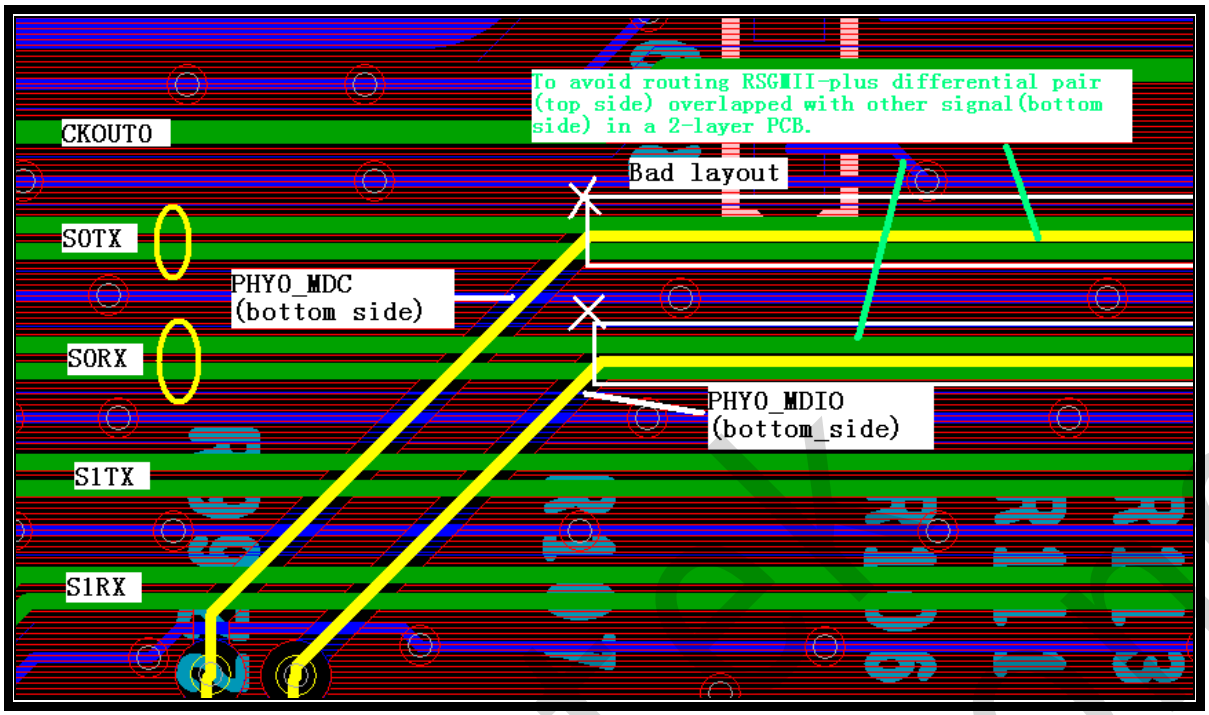

Figure 14. Avoid routing RSGMII-plus I/F overlapped with other signal in 2L PCB

9) The PHY0_MDC,PHY0_MDIO(Near RTL8218B),also suggest avoiding routing overlapped QSGMII differential pair(See Figure 15)

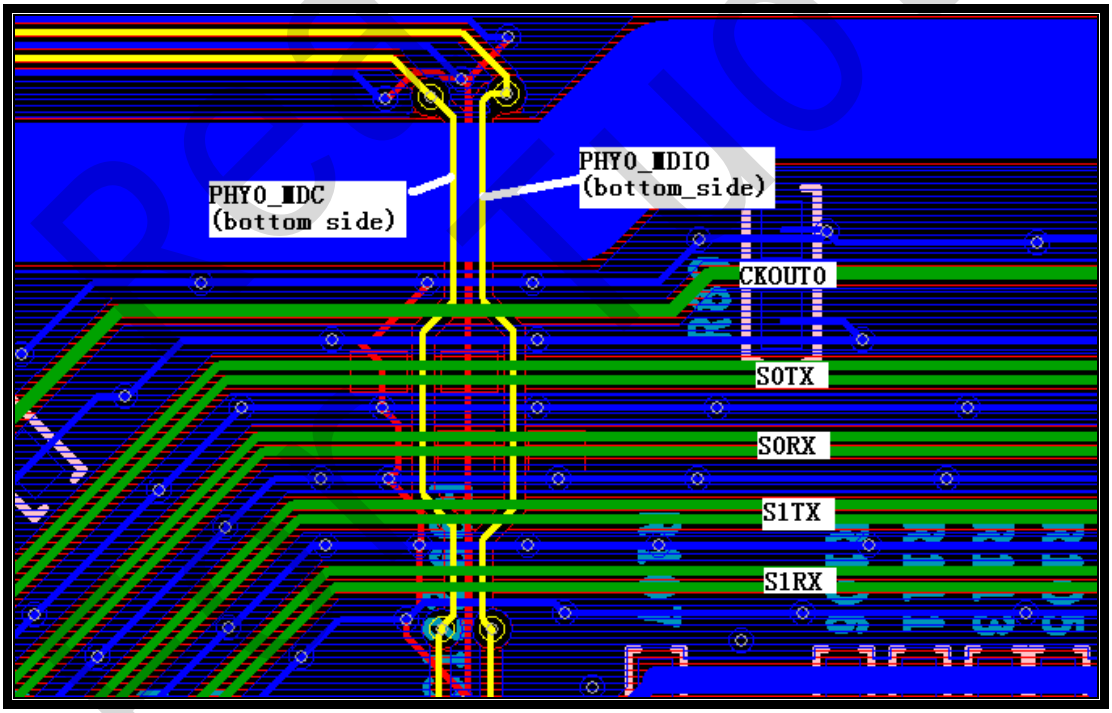

Figure 15. Avoid routing RSGMII-plus I/F overlapped with MDC/MDIO in 2L PCB

10) Trace routes over long distances should be routed at an off-angle to the X-Y axis of a PCB layer to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric (See Figure 16).

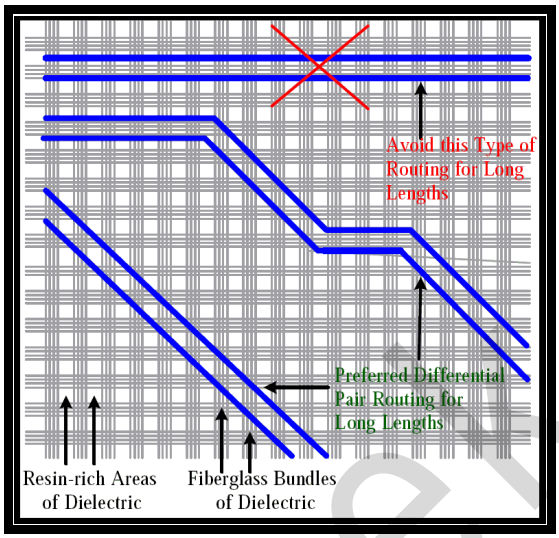

Figure 16. Long Trace Layout for Serdes

11) Differential pairs should maintain symmetry between the two signals of a differential pair whenever possible (refer to Figure 17).

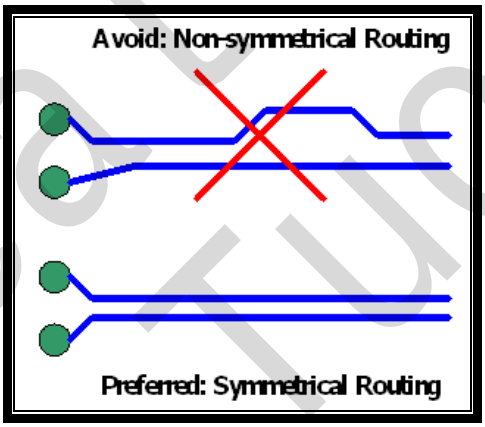

Figure 17. Symmetrical Routing

12) Keep differential pairs routing lengths as short as possible.
13) Match the length of both sets of the differential pairs, allowing no more than a 50-mil delta between the lengths of the two signals.
14) Length matching should occur on a segment-by-segment basis vs. across the total distance of the overall route.
15) Differential pairs should have a continuous reference plane, and avoid vias.
16) Size 0402 AC coupling capacitors are strongly encouraged as the smaller the package size, the less ESL.

17) Locate capacitors for coupled traces at the same location along the differential traces and near output pins of differential pairs (refer to Figure18).

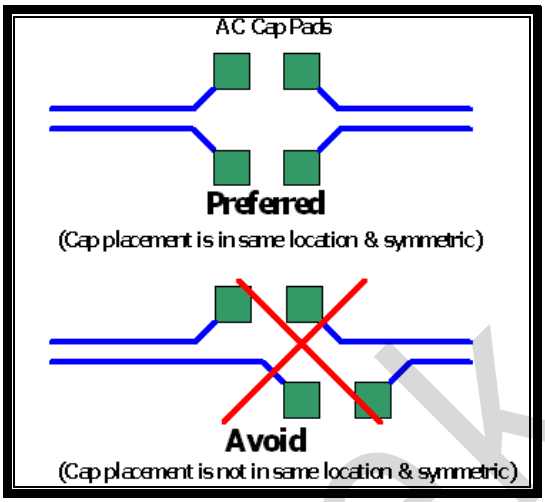

Figure 18. Symmetrical Routing Into AC Caps

18) The 10 inches maximum length of total routing trace of each group 5G Serdes is acceptable only when there is no interference.

10. Memory Interface PCB Layout Guidelines

10.1. DDR1 SDRAM Interface

The DDR1 SDRAM interface will run up to 166MHz. The following PCB layout guidelines should be followed.

1) DDR1 SDRAM clock trace should avoid passing through a vias if possible.
2) DDR1 SDRAM signal traces should be kept as short as possible.
3) Surround the DDR1 SDRAM clock traces with ground trace to minimize high-frequency emissions is possible.
4) Memory interfaces (Data Bus, Address Bus, and Control Signals) should use a source termination scheme to reduce signal reflection and EMI radiation.
5) Termination resistors must be as close to the RTL8380M/RTL8382M side as possible.
6) As much as possible to ensure the complete reference plane.

10.2. DDR2/3 SDRAM Interface

The DDR2 interface will run up to 193MHZ and DDR3 will run up to 300MHZ. The following PCB layout guidelines should be followed.

1) DDR2/3 signal traces should be kept as short as possible.
2) The suggested longest trace length for D0-D7/DM/DQS_P/N is not over 1.6-inch.
3) The suggested longest trace length for A0-A13/BA0-BA2/RAS#/CAS#/WE#/CS#/CKE/CK_P/N/RST#/ODT is not over 2.5-inch.
4) Match the length of both sets of the differential pair(CK_P/N/DQS_P/N),allowing no more than a 100-mil delta between the lengths of the two signals(**RTL8380M/RTL8382M only supported Single-ended Data Strobe Singals Un-use DQS# in DDR2 mode**)
5) A0-A13/BA0-BA2/RAS#/CAS#/WE#/CS#/CKE/CK_P/N/RST#/ODT should use a source termination resistor.
6) Termination resistor must be as close to the driver side as possible.
7) Differential-pair impedance is 100Ω±10%; single-ended impedance is 55Ω±10%.
8) A 240ohm+/-1% resistor must be connected between the ZQ pin and GND.
9) Use the Top side of the PCB for DDR2/3 signal traces, and do not use vias.
10) Surround DDR2/3 differential pair with ground trace and 5-mil space between the GND trace and differential pair in a 2-layer PCB.
11) All micro-strip traces of a DDR2/3 differential pair should be 6-mil-wide with 6-mil-wide air-gap spacing between the traces of the pair in a 2-layer PCB(see Figure 19)
12) Len CMD/ADDR/CTL Group >= Len CK_P/N >= Len DATA Group (DQS_P/N, DM, DQ) is recommended.

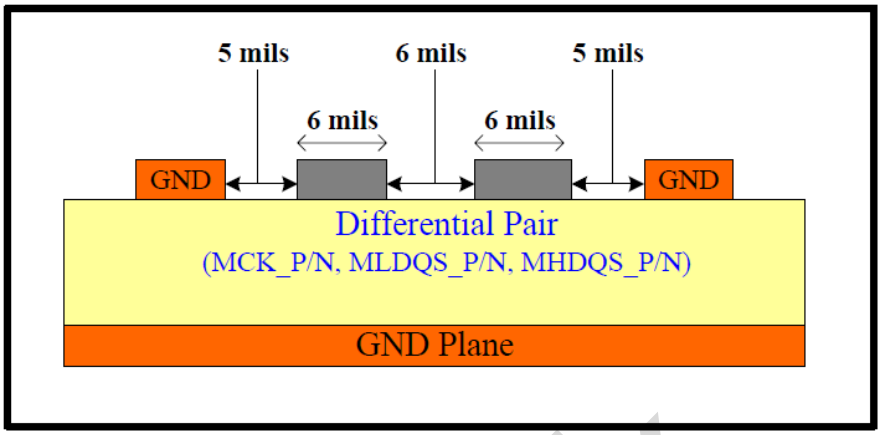

Figure 19. DDR2/3 Differential Pair trace width and spacing Recommendation for 2-Layer PCB

13) All micro-strip traces of a DDR2/3 single-ended signal should be 5-mil-wide with 5-mil-wide air-gap spacing between the traces of the pair in a 2-layer PCB(see Figure 20)

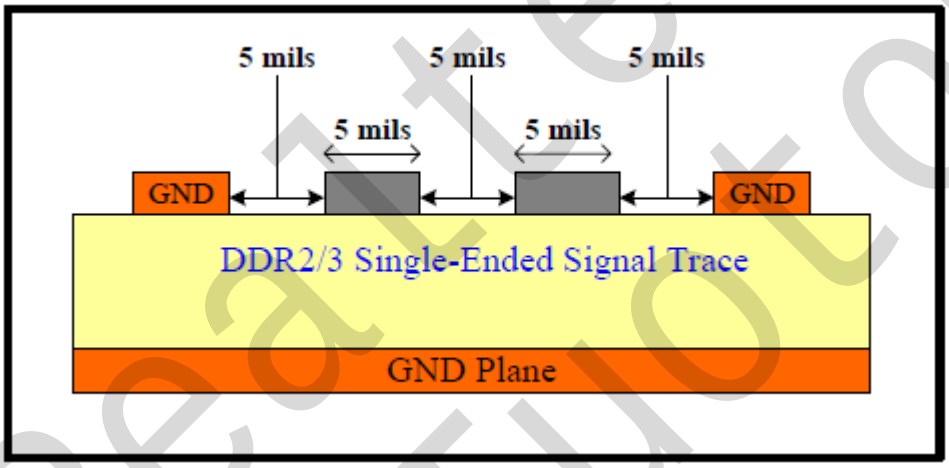

Figure 20. DDR2/3 single-Ended signal trace width and spacing Recommendation for 2-Layer PCB

14) The MVREF pin must be dealt as following figure to reduce the ripple of voltage (see Figure 21).

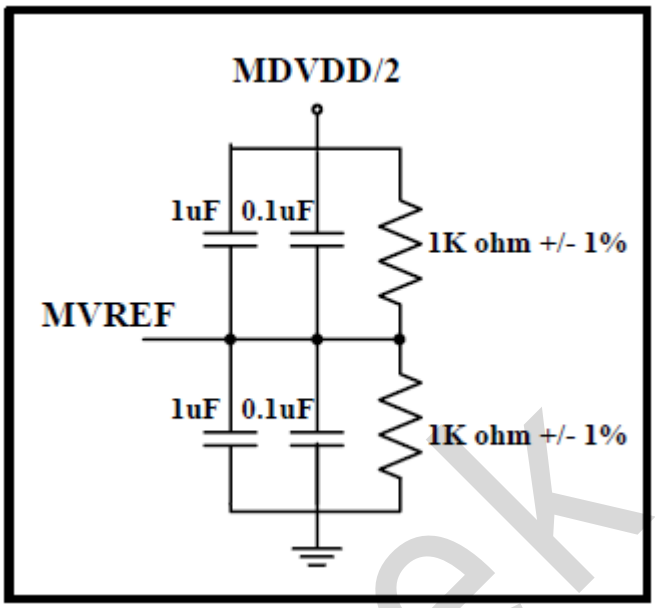

Figure 21. The scheme for MVREF Pin

15) The MCK_P/N pins must be dealt as following figure to adjust the amplitude of MCK_P/N and filter nose (see Figure 22).

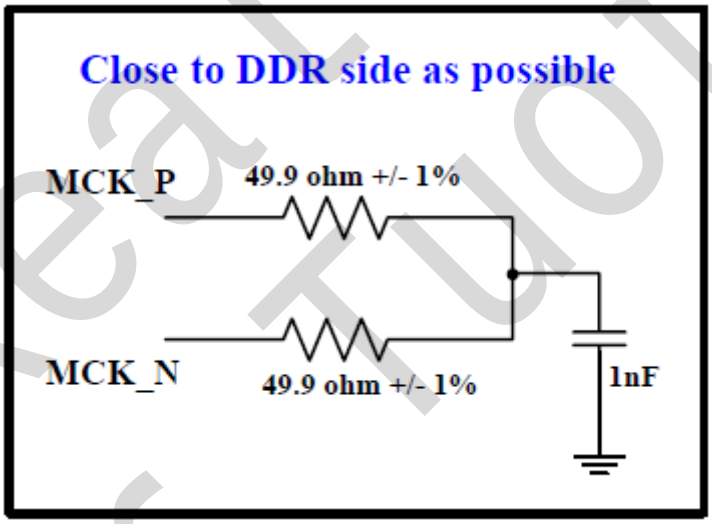

Figure 22. The scheme for MCK_P/N Pins

16) As much as possible to ensure the complete reference plane.
17) If two chip selects both be used, the star topology is suggested

Notice: In order to meet the DDR12 and DDR3 trace, the order of their pins and pin name are not the same, so please during the particles you used to select the correct net name.

10.3. SPI Flash Interface

The SPI Flash interface will run up to 50MHz. The following PCB layout guidelines should be followed.

1) SPI Flash clock trace should avoid passing through a vias if possible.
2) SPI Flash signal trace should be kept as short as possible.
3) Surround the SPI Flash clock traces with ground trace to minimize high-frequency emissions if possible.
4) If the termination resistors be used, the termination resistors must be as close to the driver side as possible.
5) Match each memory interface trace length to within 200mil.

11. Placement for thermal

- In the area under RTL838x, reserve some space for heat dissipation(See Figure 23)

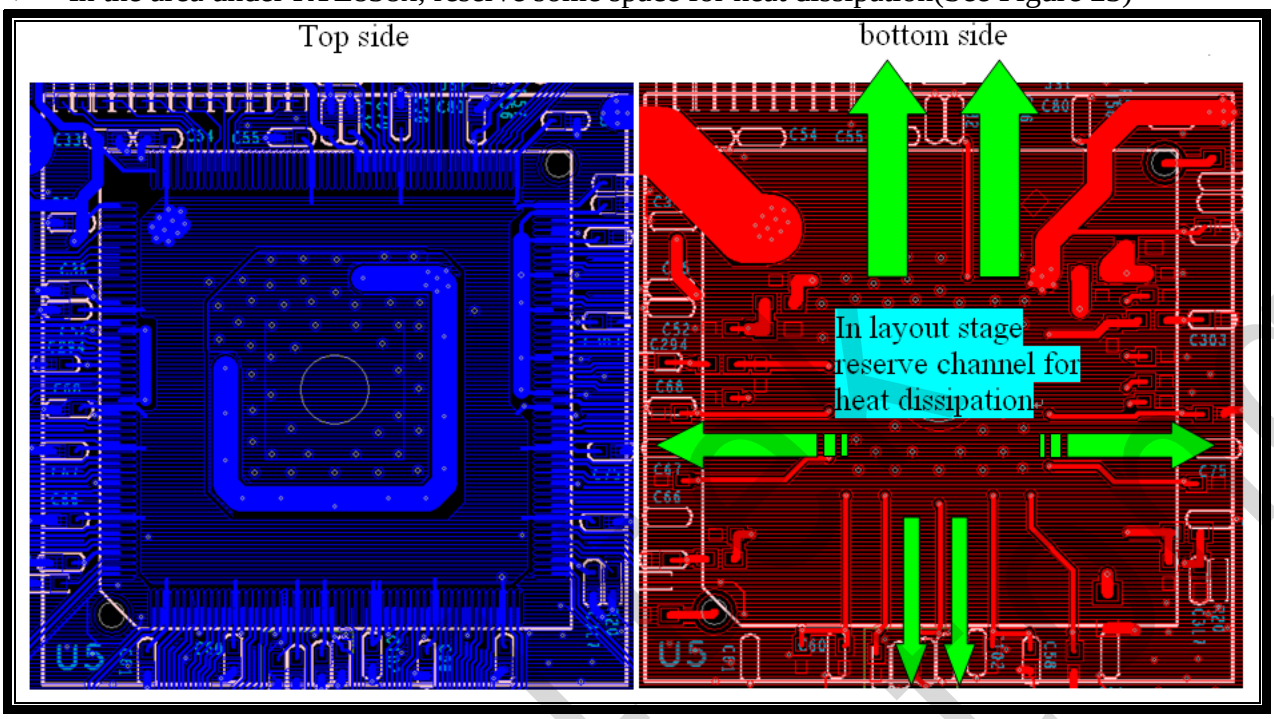

Figure 23. Better way for heat dissipation in RTL8382M/L

- In the area under RTL8218B,reserve some space for heat dissipation(See Figure 24)

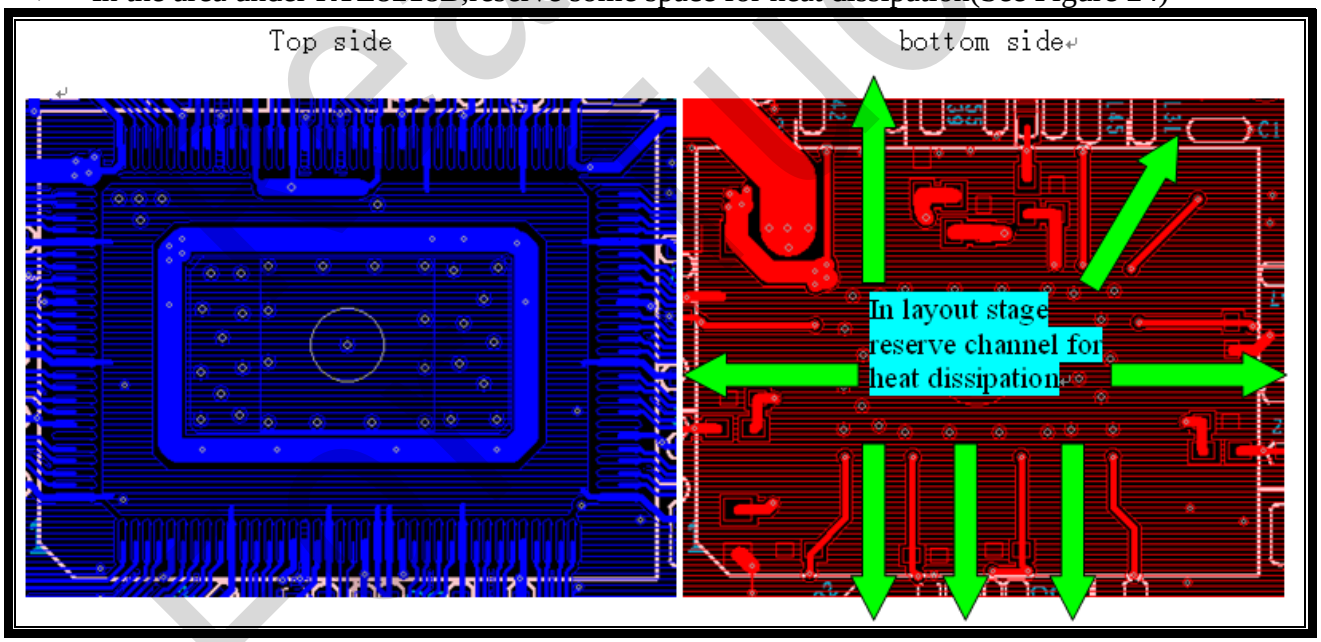

Figure 24. Better way for heat dissipation in RTL8218B

12. ESD/EMI Design Guide

- The System Ground must be away from chassis ground plane at least 80mil(See Figure 25)

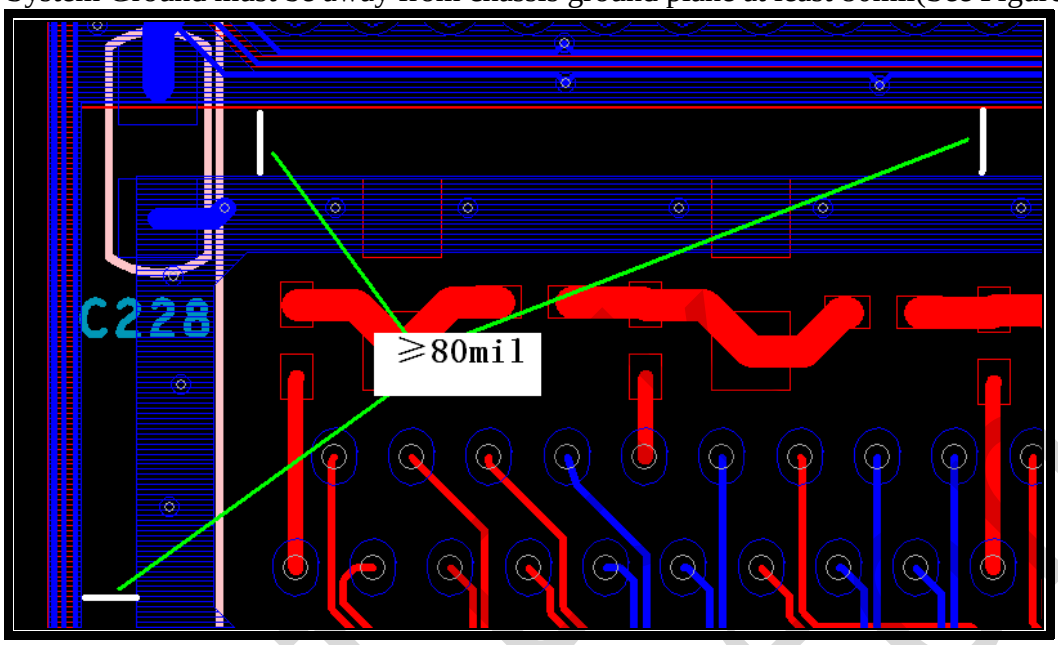

Figure 25. System GND away from chassis GND at least 80mil

- Recommend to Place the 2KV high voltage capacitors that between chassis ground and system ground on both Top and Bottom side.
- The second side of transformer and phone jack should have keep out area. All interconnection between transformer and phone jack must away from chassis ground plane at least 60mils(see Figure 26)

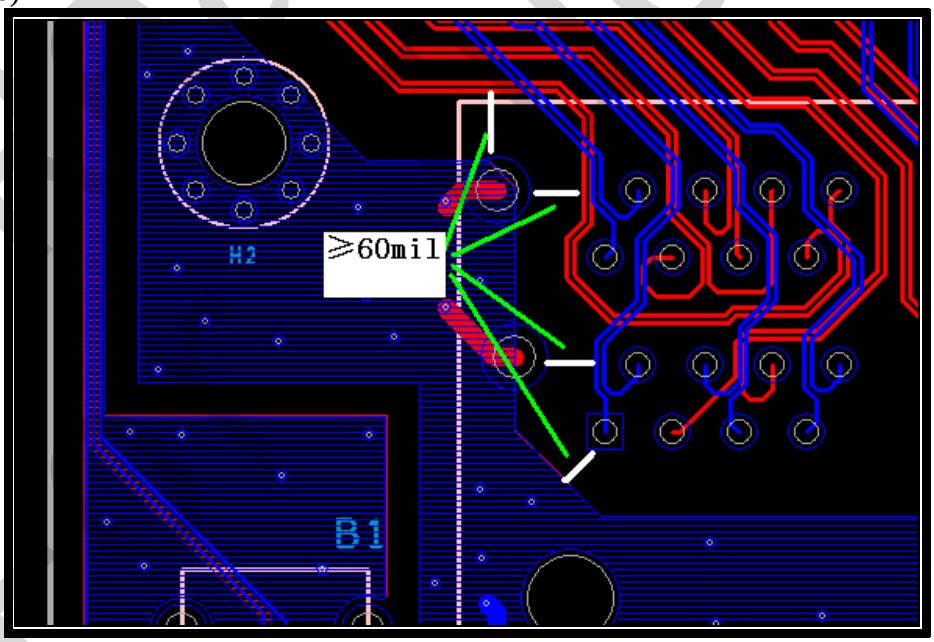

Figure 26. Transformer and Phone Jack Keep-out Area

- Screw holes in the RJ45 region directly connected to the chassis ground (See Figure 27).

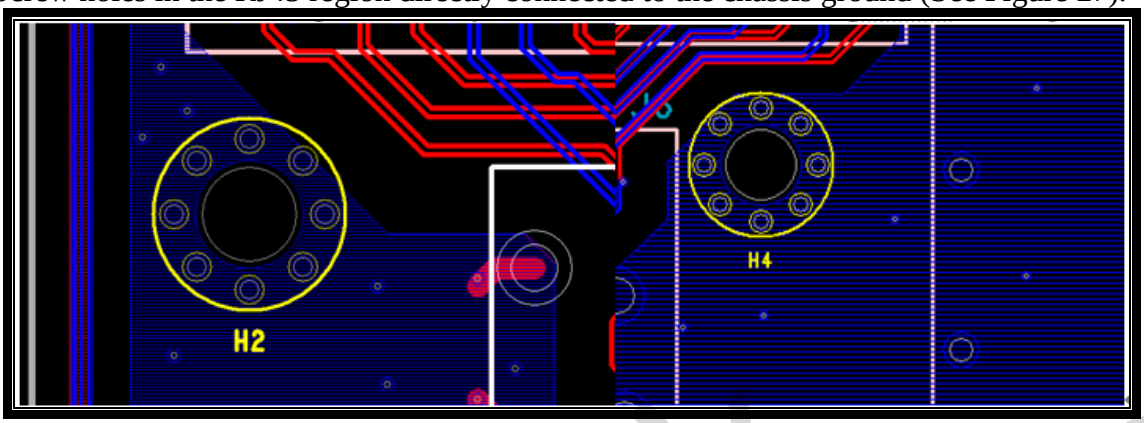

Figure 27. The screw holes in RJ45 region

- The screw holes in system need two 0.1uF capacitance to connect with system GND, and keep to at least 60mil spacing (See Figure 28).

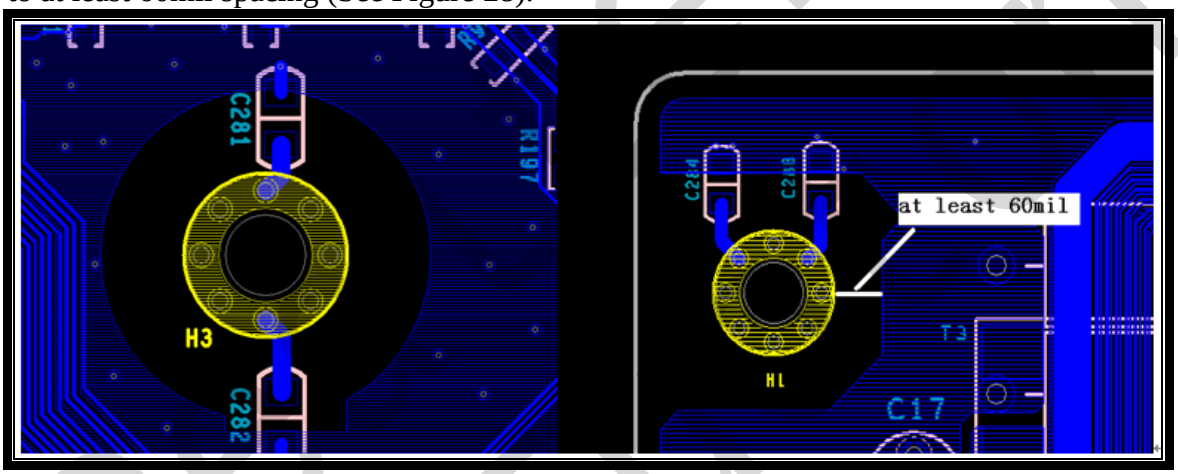

Figure 28. The screw holes in system GND region

- Reserve 2KV capacitor at transformer center tap for ESD solution. Per-port with one 2KV capacitor is better than two ports on 2KV capacitor for ESD test.
- Strongly Recommend to reserve the **15pF** 0402 Capacitances between the MDI signal and GND for improve the ESD ability, and place it near the transformer as soon as possible (See Figure 29).

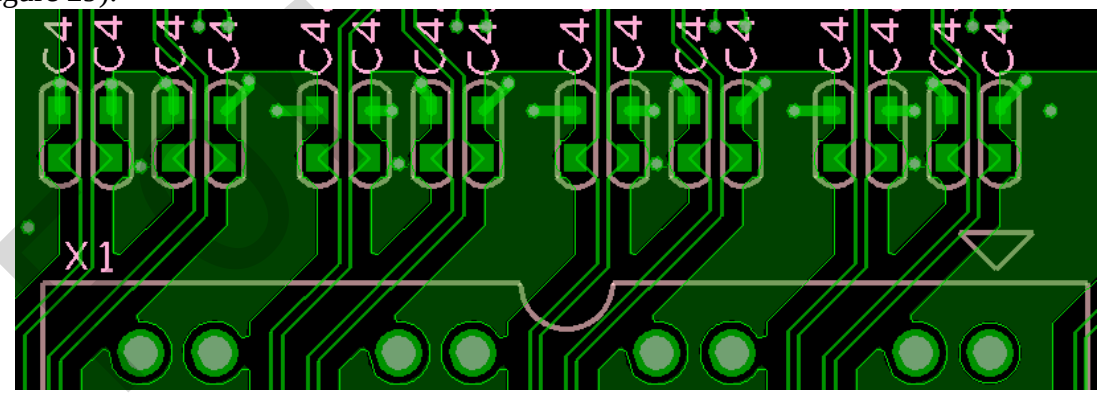

Figure 29. The Capacitance between MDI signal and GND Layout

- Increase the core power plane(1.1V Power) as much as possible
  According to the 4-Layer PCB as an example, Increase the wide of core power plane to about 2 inch Can obviously improve the ESD protection ability.(See Figure 30)

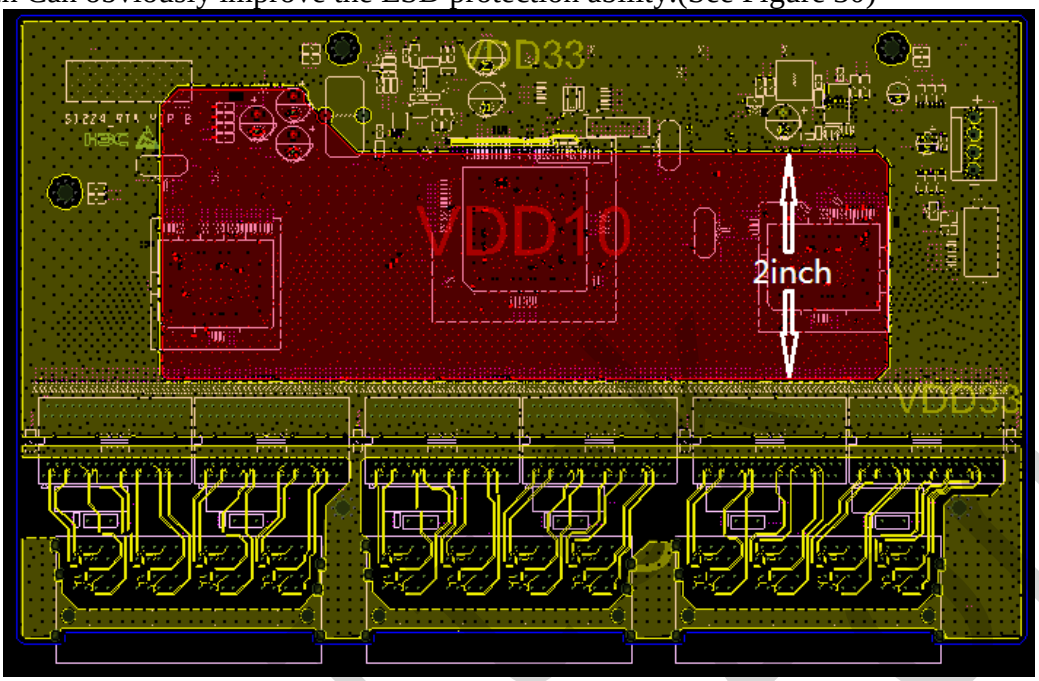

Figure 30. The recommend core power plane

- Recommend using the transformer with common mode chock at IC side for better EMI / ESD performance.(See Figure 31)

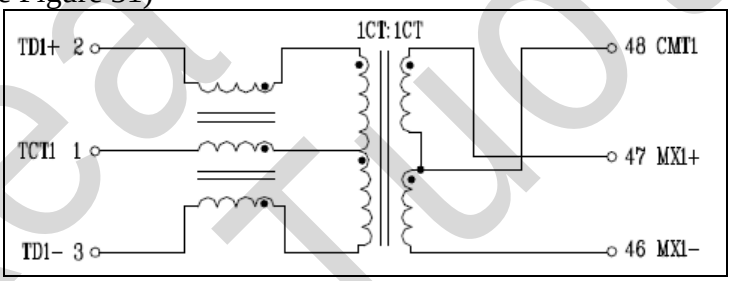

Figure 31. The Transformer with Common Mode chock at IC Side

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com.tw