RTL8305SB Port 4 Application Note

1. General Description

Operation mode of port4: Each port of RTL8305SB has two parts: MAC and PHY. In the UTP and FX mode, Port4 uses both the MAC and internal PHY parts like the other ports. In the other mode, Port4 uses only the MAC part, which provides an external interface to connect to the external MAC or PHY. Two pins are used for those operation mode configurations: P4MODE[1:0].

The fifth port (port 4) supports an external MAC interface which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with an external MAC of a routing engine, PHY of a HomePNA or other physical layer transceiver.

If the MAC part of Port4 connects with an external MAC, such as processor for a router application, it should act as a PHY. This is PHY mode MII or PHY mode SNI. In PHY mode MII or PHY mode SNI, Port4 uses the MAC part only, and provides an external MAC interface to connect MAC of external device. In order to connect both MACs, the MII of the switch MAC should be reversed into PHY mode.

If the MAC part of Port4 connects with an external PHY, such as a PHY for a HomePNA application, Port4 should act as MAC. This is MAC mode MII. In MAC mode MII, Port4 uses its MAC to connect external PHY and ignores the internal PHY part.

External MAC interface: In order to act as PHY. When port4 is in PHY mode, some pins of the external MAC interface should be changed. For example, TXC are input pins for MAC but output pins for PHY. So the pin MTXC/PRXC is input for MAC mode and output for PHY mode. Please refer to below diagram to check the relationship between RTL8305SB and the external device. Hint: Connect input of RTL8305SB to output of external device. RTL8305SB has no RXER, TXER, and CRS pins for MII signaling. Because RTL8305SB does not support pin CRS, it is necessary to connect the MTXEN/PRXDV (output) of PHY mode to both CRS and RXDV (input) of the external device.
Note: In order to differentiate between MAC and PHY mode, the RTL8305SB change the pin name of PHY mode. For example: RTL8305SB=MRXD[0]/PTXD[0], RTL8305S=MRXD[0]/MTXD[0].

Port4 status pins: When P4MODE[1:0]=11, Port4 can be either UTP or MAC mode MII. Port4 will automatically detect the link status of UTP from internal PHY and link status MAC mode MII from both TXC of external PHY and P4LNKSTA#. If both UTP and MII port are linked OK, UTP has higher priority and RTL8305SB will ignore the signal of MII port.

In UTP and FX mode, the internal PHY will provide the port status (Link/Speed/Duplex/Full Flow Control ability) in real time. In order to provide the initial configuration of Port4's PHY (UTP or FX mode), four pins (P4ANEG, P4FULL, P4SPD100, P4EEFC) are used to strap upon reset. **Upon reset:** defined as a short time after at the end of hardware reset. However, three of these pins are also used for Port4's MAC (the other three modes) in real time after reset (P4SPD100 -> P4SPDSTA, P4FULL -> P4DUPSTA, P4ENFC -> P4FLCTRL). **After reset:** defined as the time after upon reset. *Note: These 3 pin are changed as high active in order to provide dual function. For example: RTL8305SB=P4SpdSta/P4Spd100, RTL8305SB=P4SpdSta#.*

In the other three modes, four pins (P4LNKSTA#, P4SPDSTA, P4DUPSTA, P4FLCTRL) are necessary in order to provides the port status to Port4's MAC in real time. That means that the external MAC or PHY should be forced to the same port status as Port4's MAC. In some applications, xDSL or Home Gateway, CPU or xDSL transceivers would poll the PHY status via MDC/MDIO interface. RTL8305SB provides some special information in MII registers for these applications to satisfy the polling procedure of the master chips. PHY 4 register 1.2 reflects the P4LNKSTA# status, and PHY 4 register 0.13 reflects the P4SPDSTA status, and PHY 4 register 0.8 reflects the P4DUPSTA status. Other bits in PHY 4 register 0 and 1 would follow the default value of the chip definition.

Related pins: When port4 is in UTP or FX mode, the LEDs of port4 are used to displays PHY status. When port4 is in other mode, the LEDs of port4 are used to displays MAC status.

Four parallel LEDs corresponding to port 4 can be three-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM as 0. In UTP application, this bit should be 1 to drive LEDs of port 4.

Pin **SEL_MIIMAC#** can be used to indicate MII MAC port active after reset for the sake of UTP/MII auto-detection.

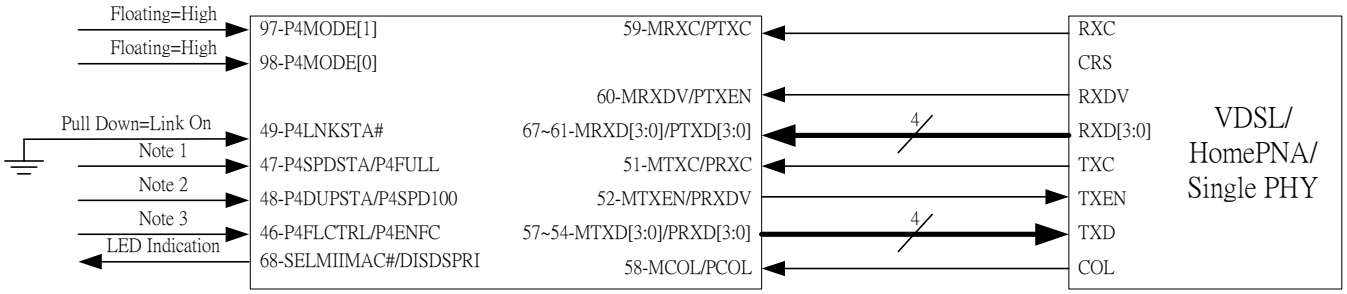
One 25MHz clock output (pin CK25MOUT) can be used as a clock source of the underlying HomePNA/other PHY physical devices. *Note: the output voltage is 2.5V for RTL8305SB but is 3.3V for RTL8305S.*

PHY mode MII/PHY mode SNI: In routing application, RTL8305SB cooperates with a routing engine to communicate with WAN (Wide Area Network) through MII/SNI. In such application, P4LNKSTA# =0 and P4MODE[1] is pulled low upon reset. P4MODE[0] determines whether MII or SNI mode is selected.

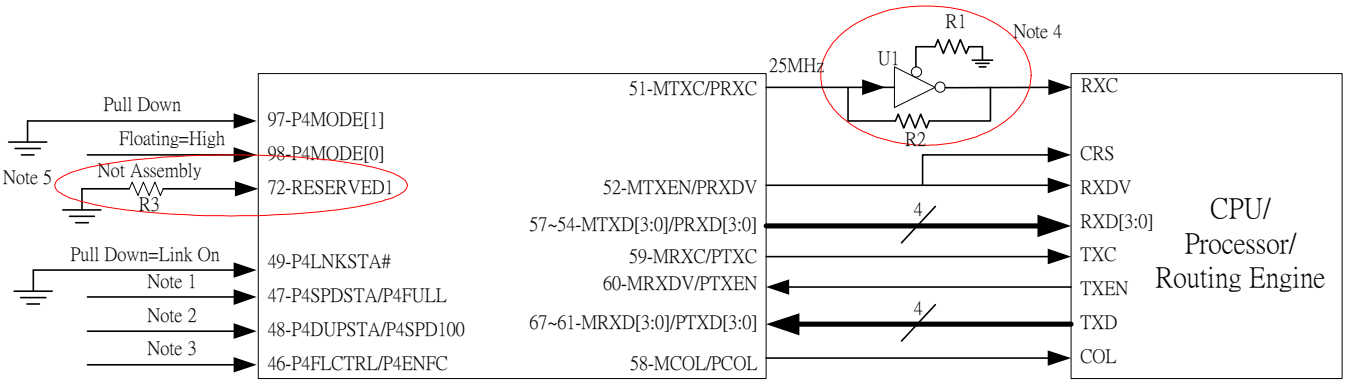
In MII (nibble) mode (P4MODE[0]=1), P4SPDSTA=1 results in MII operating at 100Mbps with MTXC and MRXC runs at 25MHz; however, P4SPDSTA=0 leads to MII operating at 10Mbps with MTXC and MRXC runs at 2.5MHz.

In SNI (serial) mode (P4MODE[0]=0), P4SPDSTA takes no effect and should be pull-down. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. In SNI mode, RTL8305SB does not loopback RXDV signal as response to TXEN and does not support heart-beat function. (asserting COL signal for each complete of TXEN signal).

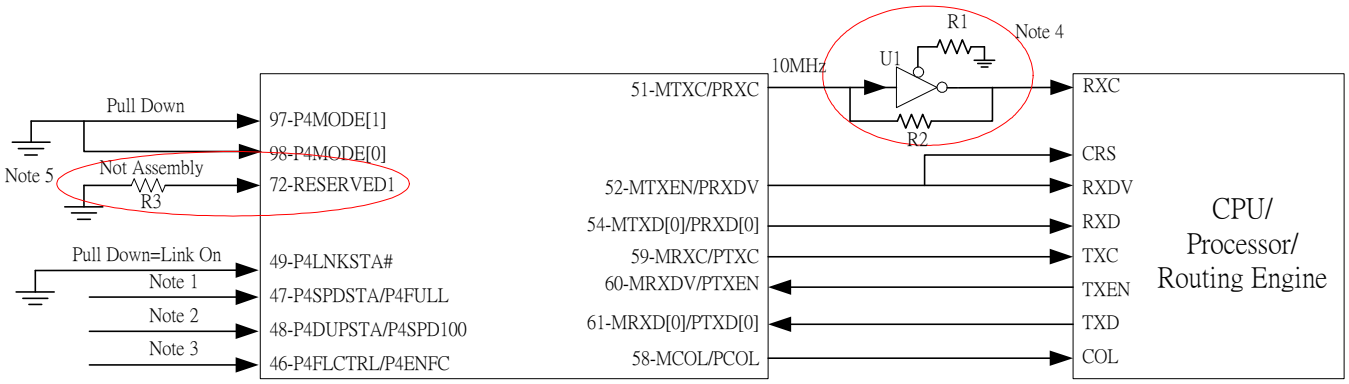
MAC mode MII: In HomePNA or other PHY applications, the RTL8305SB provides the MII interface to the underlying HomePNA or other physical devices so as to communicate with other types of LAN media. In such applications, the P4MODE[1:0] pins are floating upon reset and the RTL8305SB supports the UTP/MII auto-detection function. When both UTP and MII are active (link on), the UTP port has a higher priority over MII port.



MAC mode MII



PHY mode MII



PHY mode SNI

Note 1: Pull high or floating means to set the speed as 100Mbps and pull down means to set the speed as 10Mbps.

Note 2: Pull high or floating means to set as full duplex and pull down means to set as half duplex.

Note 3: Pull high or floating means to enable flow control or backpressure and pull down means to disable flow control or backpressure.

Note 4: R1 is used to enable/disable the single logic gate, R2 is used to bypass the single logic gate, and U1 could be optional selected as 74LVC1G04 or 74LVC1G125 (gate delay within 5 ns) to fine tune the timing of MII interface trace.

Note 5: R3 should not be assembled; it's reserved for future.

2. Pin Description

The following table describes the pin definition of the Port 4 MII interface.

Pin Name	Pin No.	Type	Description
P4MODE[1:0]	97,98	I	**Select Port 4 operating mode:** 11: UTP / MAC mode MII 10: 100Base-FX mode 01: PHY mode MII 00: PHY mode SNI The RTL8305SB has 4 options and the RTL8305S has 3 options. ***These pins have internal 75k ohm pull-high resistors.***
P4LNKSTA#	49	I	**Port4 Link Status for MAC:** This pin determines the link status of the Port4 MAC in real-time. That is link status of real-time for MII MAC/MII PHY/SNI PHY only. This pin is low active. 1: No Link. 0: Link. ***PHY 4, register 1.2 reflects this status in MAC mode MII, and PHY mode MII, and PHY mode SNI.*** ***This pin has internal 75k ohm pull-high resistor.***
P4DUPSTA	48	I	**Port4 MAC Circuit Duplex Status (real time after reset):** Duplex Status for MAC circuit (MAC mode MII/PHY mode MII/PHY mode SNI) in real time after reset. 1: Full duplex. 0: Half duplex. ***PHY 4, register 0.8 reflects this status in MAC mode MII, and PHY mode MII, and PHY mode SNI.***

			This pin has internal 75k ohm pull-high resistor.
P4SPDSTA	47	I	**Port4 MAC Circuit Speed Status (real time after reset):** Speed Status for MAC circuit (MAC mode MII/PHY mode MII/PHY mode SNI) in real time after reset. 1: 100M bps. 0: 10M bps. When P4MODE[1:0]=00 (PHY mode SNI), speed is dedicated to 10MHz clock rate. This pin should be pulled down. ***PHY 4, register 0.13 reflects this status in MAC mode MII, and PHY mode MII, and PHY mode SNI.*** ***This pin has internal 75k ohm pull-high resistor.***
P4FLCTRL	46	I	**Port4 Flow Control (real time after reset):** Flow Control Status for MAC circuit (MAC mode MII/PHY mode MII/PHY mode SNI) in real time after reset. 1=Enable Flow Control ability. 0=Disable Flow Control ability. ***This pin has internal 75k ohm pull-high resistor.***
Port 4 MAC Circuit Interface Pin Definition			
MRXD[3:0]/ PTXD[3:0]	67,66,63,61	I	For MAC mode MII, these pins are MRXD[3:0], MII receive data nibble. For PHY mode MII, these pins are PTXD[3:0], MII transmit data nibble. For PHY mode SNI, PTXD[0] is serial transmit data. And suggest PTXD[3:1] to have 1K ohm external pull-low resisters. ***These pins have no internal pull-high resistors.***
MRXDV/PTXEN	60	I	For MAC mode MII, this pin represents MRXDV, MII receive data valid. For PHY mode MII, this pin represents PTXEN, MII transmit enable. For PHY mode SNI, this pin represents PTXEN, transmit enable. ***This pin has no internal pull-high resistor.***
MRXC/PTXC	59	I/O	For MAC mode MII, it is receive clock, MRXC (acts as input). For PHY mode MII/PHY mode SNI, it is transmit clock, PTXC (acts as output). ***This pin has no internal pull-high resistor.***
MCOL/PCOL	58	I/O	For MAC mode MII, this pin represents MCOL collision (acts as input) For PHY mode MII/PHY mode SNI, this pin represents PCOL collision (acts as output) ***This pin has no internal pull-high resistor.***

MTXD[3]/ PRXD[3]/ P4IRTag[1] MTXD[2]/ PRXD[2]/ P4IRTag[0] MTXD[1]/ PRXD[1]/ LEDMode[1] MTXD[0]/ PRXD[0]/ LEDMode[0]	57 56 55 54	I/O	**Output after reset:** For MAC mode MII (P4Mode[1:0]=11), these pins are MTXD[3:0], **MII transmit data of MAC**. For PHY mode MII (P4Mode[1:0]=01), these pins are PRXD[3:0], **MII receive data of PHY**. For PHY mode SNI (P4Mode[1:0]=00), PRXD[0] is **SNI serial receive data**. ***These pins have internal 75k ohm pull-high resistors.*** *Note: For P4IRTag[1:0] and LEDMode[1:0] please refer to section 5.3 of RTL8305SB-C datasheet.*
MTXEN/PRXDV	52	O	For MAC mode MII, this pin represents MTXEN, MII transmit enable. For PHY mode MII, this pin represents PRXDV, MII received data valid. For PHY mode SNI, this pin represents PRXDV, received data valid. ***These pins have internal 75k ohm pull-high resistors.***
MTXC/PRXC	51	I/O	For MAC mode MII, it is transmit clock, MTXC (acts as input). For PHY mode MII/PHY mode SNI, it is receive clock, PRXC (acts as output). ***These pins have internal 75k ohm pull-high resistors.***

3. MII Register Definition

For port 4 MAC application circuit, PHY 4 MII registers real time represent the port 4 MAC part status (link status, speed, duplex; i.e. Reg1.2, Reg.0.13, Reg.0.8). Other register would follow the default value of the chip definition. The detail definition is shown as the following table.

3.1 Register0: Control Register

Reg.bit	Name	Description	Mode	Default
0.15	Reset	**Reset:** 1: PHY reset. This bit is self-clearing.	RW/SC	**0**
0.14	Loopback (digital loopback)	**Enable Loopback:** This pin enables loopback from the MII TXD to the MII RXD and ignores all the activities on the cable media. 1: Enable loopback 0: Normal operation This function is usable only when this PHY is 10Based-T full duplex or 100Base-T full duplex. The packet is forwarded from other PHY (could be 10Based-T, or 100TX, or 100FX, both full and half duplex) by switch core and will loopback to the switch core. It could be forwarded to the other port or dropped depending on the destination and source MAC address of the packet.	RW	**0**
0.13	Spd_Sel	**Speed Select:** 1: 100Mbps 0: 10Mbps When Nway is enabled, this bit reflects the result of auto-	RW	From pin

		negotiation. (Read only) When Nway is disabled, this bit can be set through SMI. (Read/Write) When 100FX mode is enabled, this bit =1. (Read only) ***For MAC mode MII, PHY mode MII, and PHY mode SNI, it reflects the status of P4SPDSTA.***		
0.12	Auto Negotiation Enable	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI.(Read/Write) When 100FX mode is enabled, this bit =0.(Read only) 100FX should be force mode. In order to avoid errors, the RTL8305SB will ignore the action to this bit when writing Reg0.12 as 1 in 100FX mode.	RW	From pin
0.11	Power Down	1: Power down. All functions will be disabled except SMI function and internal TXC to MAC. 0: Normal operation.	RW	**0**
0.10	Isolate	1: Electrically isolate the PHY from internal MII. The PHY is still able to response to MDC/MDIO. 0: Normal operation	RW	**0**
0.9	Restart Auto Negotiation	1: Restart Auto-Negotiation process. 0: Normal operation.	RW/SC	**0**
0.8	Duplex Mode	Duplex mode: 1: Full duplex operation 0: Half duplex operation When Nway is enabled (Reg0.12=1), this bit reflects the result of auto-negotiation. (Read only) When Nway is disabled (Reg0.12=0, force mode of UTP or 100FX), this bit can be set through SMI*. (Read/Write) 100FX should be force mode. In order to avoid errors, the RTL8305SB will ignore the action to this bit when writing Reg0.12 as 1 in 100FX mode. ***For MAC mode MII, PHY mode MII, and PHY mode SNI, it reflects the status of P4DUPSTA.***	RW	From pin
0.[7:0]	Reserved		RO	**0**

3.2 Register1: Status Register

Reg.bit	Name	Description	Mode	Default
1.15	100Base_T4	0: No 100Base-T4 capability.	RO	**0**
1.14	100Base_TX_FD	1: 100Base-TX full duplex capable. 0: Not 100Base-TX full duplex capable.	RO	**1**
1.13	100Base_TX_HD	1: 100Base-TX half duplex capable. 0: Not 100Base-TX half duplex capable.	RO	**1**
1.12	10Base_T_FD	1: 10Base-TX full duplex capable. 0: Not 10Base-TX full duplex capable.	RO	**1**
1.11	10Base_T_HD	1: 10Base-TX half duplex capable. 0: Not 10Base-TX half duplex capable.	RO	**1**
1.[10:7]	Reserved		RO	**0**
1.6	MF Preamble Suppression	The RTL8305SB will accept management frames with preamble suppressed. The RTL8305SB accepts management frames without preamble. Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is	RO	**1**

		required between any two management transactions as defined in IEEE802.3u specs.		
1.5	Auto-negotiate Complete	1: Auto-negotiation process completed. MII Reg.4,5 are valid if this bit is set. 0: Auto-negotiation process not completed.	RO	**0**
1.4	Remote Fault	1: Remote fault condition detected. 0: No remote fault. When in 100FX mode, this bit means in-band signal Far-End-Fault is detected.	RO/LH	**0**
1.3	Auto-Negotiation Ability	1: Nway auto-negotiation capable. (permanently: 1)	RO	**1**
1.2	Link Status	1: Link is established. If link had ever failed, this bit will be 0 until after reading this bit again. 0: Link is failed. ***For MAC mode MII, PHY mode MII, and PHY mode SNI, it reflects the status of P4LNKSTA#.***	RO/LL	**0**
1.1	Jabber Detect	0: No Jabber detected. Note: this function is not necessary for single chip.	RO	**0**
1.0	Extended Capability	1: Extended register capable. (permanently: 1)	RO	**1**