REALTEK

RTL8211C-GR
RTL8211CL-GR

INTEGRATED 10/100/1000 GIGABIT ETHERNET TRANSCEIVER

LAYOUT GUIDE

(CONFIDENTIAL: Development Partners Only)

Rev. 1.6
06 July 2009
Track ID: JATR-1076-21

REALTEK

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference on the RTL8211C(L) Gigabit Ethernet transceiver.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2007/08/20	First release.
1.1	2008/02/05	Revised section 3.1 RX Clock (RXC), page 5.
1.2	2008/05/26	Revised section 9.1 PCB Layout, page 22. Revised section 9.4 Typical Switching Regulator PCB Layout, page 28. Added section 9.5 Efficiency Measurement, page 29. Revised section 10.5 Power Inductor, page 31.
1.3	2008/09/09	Expanded power, ground, and LED plane layout sections.
1.4	2009/03/17	Revised section 2.1 Placement, page 2. Revised section 3.3 RGMII Signals, page 7. Added section 4 PCB Stack-Up, page 10.
1.5	2009/06/03	Revised matching lengths/pairs spacing of traces in section 3.2, page 6. Added traces distance information in section 3.3, page 7. Revised section 9.1 PCB Layout, page 22. Revised section 10.4 Capacitors, page 31.
1.6	2009/07/06	Corrected minor typing errors.

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1. Introduction

The Realtek RTL8211C(L)-GR is a highly integrated and sophisticated Ethernet transceiver that complies with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable.

The RTL8211C(L)-GR uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, crosstalk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211C(L)-GR to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII) for 1000Base-T, 10Base-T, and 100Base-TX.

2. Design and Layout Guide

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8211C(L)-GR. Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8211C(L)-GR.

(3) Simplify the task of routing signal traces.

In order to achieve maximum performance using the RTL8211C(L)-GR, good design practices are required throughout the process. The following are some recommendations for implementing a high performance system.

2.1. Placement

- The RTL8211C(L)-GR must be placed as close as possible to the MAC (less than 2.5 inches).
- The resistor connected to the RSET pin should be placed close to the RTL8211C(L)-GR (less than 800mils), and as far away as possible from signal traces (e.g., VRRREG, REG_OUT, MDI0+/-, MDI1+/-, etc.) and clock signals (50mils min.).
- For good EMI performance, the PHY device must be placed as close as possible to the MAC (less than 2.5 inches). If the MAC is placed on the top layer, then the PHY should be put on the bottom layer to avoid heat sink coupling.

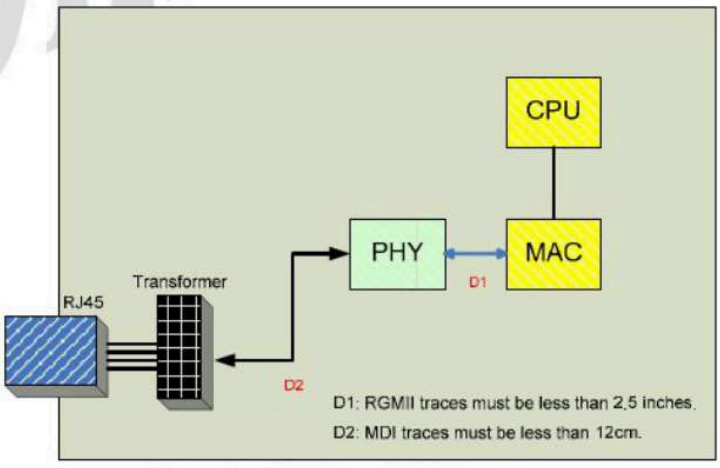


Figure 1. RGMII and MDI Placement

2.2. Magnetics

- The 10/100/1000M magnetics should be placed as close as possible to the RJ-45 connector. The MDI traces must be less than 12cm.
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other.

2.3. Crystal/OSC

- Following the 3W rule, the Crystal should be placed at least three times its own width from I/O ports, important or high frequency signal traces (Tx, Rx, power), and magnetics.
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI. The retaining straps of the OSC, if any, need good grounding as well.

2.4. Termination Resistors and Capacitors

The termination resistors and capacitors are required only for RTL8201N co-layout. Figure 2 shows the layout of the RTL8211C-GR. Refer to the reference schematic, available from Realtek, for details.

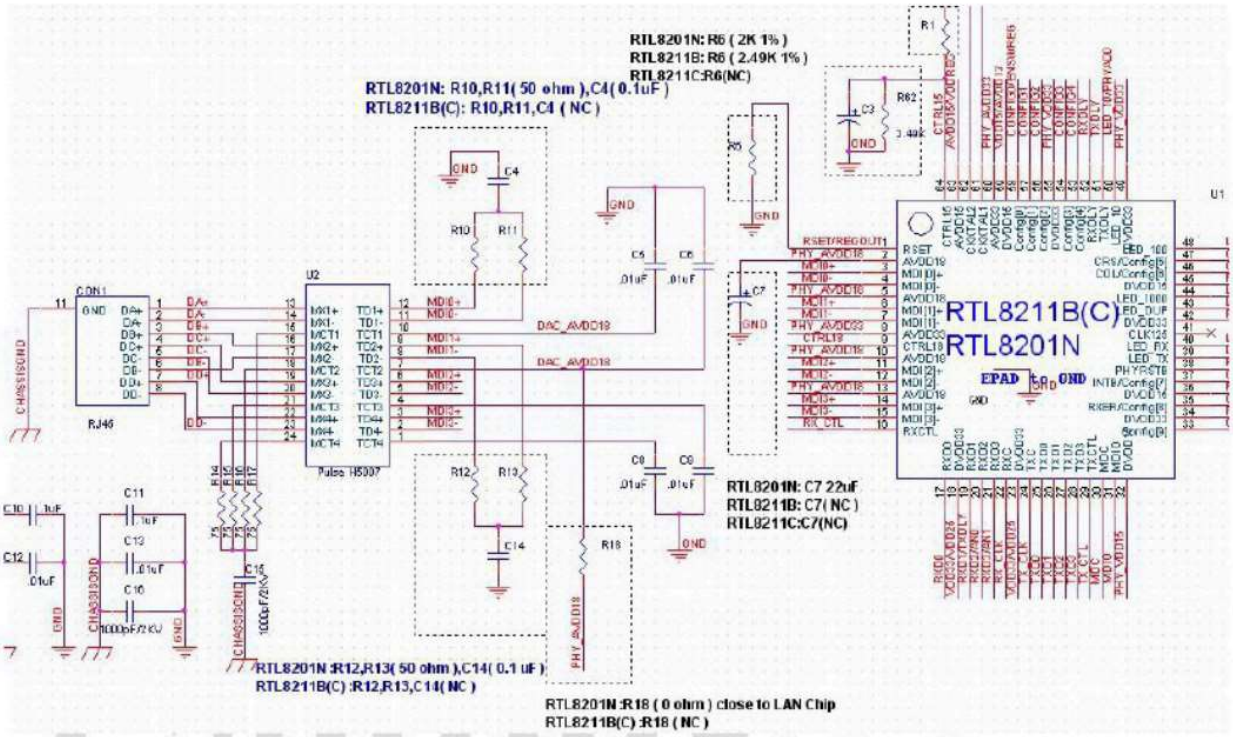


Figure 2. Termination Resistors and Capacitors Placement

2.5. Ferrite Beads and De-Coupling Capacitors

Every PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors must be placed close to the power pins, such that the distance from the IC power pin to the capacitor is less than 200mils.

3. Signal and Trace Routing

Noise, ringing, and data lines must be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

3.1. RX Clock (RXC)

- Clock signal traces should be as short and wide as possible.
- Route the clock traces adjacent to an unbroken ground or power plane. Minimize vias and layer changes.
- Place the filter network (Figure 3) as close to the driving source (RXC pin) as possible. The RXC filter network minimizes EMI effects.

Figure 3 Resistor Value: 22ohm

Figure 3 Capacitor Value: <22pF (Only necessary for countering excessive EMI problems. Default is not connected (NC))

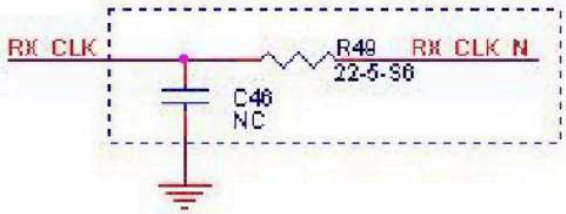


Figure 3. RX Clock

3.2. MDI Signals

- Traces routed from the RTL8211C(L)-GR to the 10/100/1000M magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8211C(L)-GR and magnetics is achievable only when there is no interference.
  It is also very important to keep all four differential pair signal traces (MDI0+/-, MDI1+/-, etc.) at matching lengths (within 800mil). MDI impedance is 50ohm common mode, 100ohm differential mode)
  The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong cancelling effect on noise. D1 can be the width of each of the two differential traces. E.g., if the width of the trace is 8mil, then D1 can be 8mil wide (Figure 4).

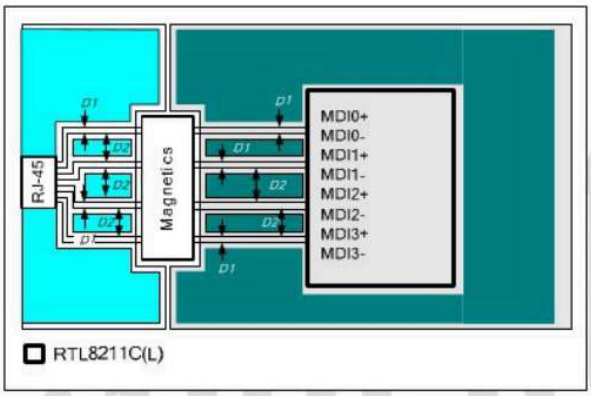


Figure 4. MDI Signals

- We suggest that there should be more than 30mil spacing between different differential pairs to minimize crosstalk coupled from other pairs (D2 in Figure 4). In addition, Ground Plane shielding can be used to separate all four signal pairs. However, a good layout should avoid the following situations:
  --Intersection of any two pairs of signal traces.
  --Intersection of the two signal traces of the same differential pair.
- To minimize impedance mismatch, we recommend not using vias on the four differential pairs.
- Signals crossing a plane split (see Figure 5) may cause unpredictable return path currents and would likely result in signal quality failure, as well as creating EMI problems.

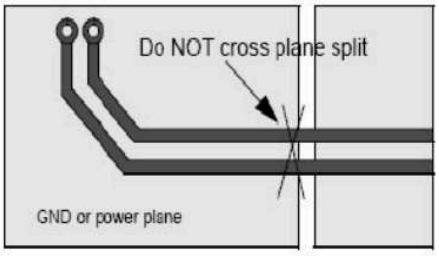


Figure 5. Signal Trace

3.3. RGMII Signals

- Ninety-degree trace turns must be avoided. We recommend that the traces turn at 45° angles as shown in Figure 6. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

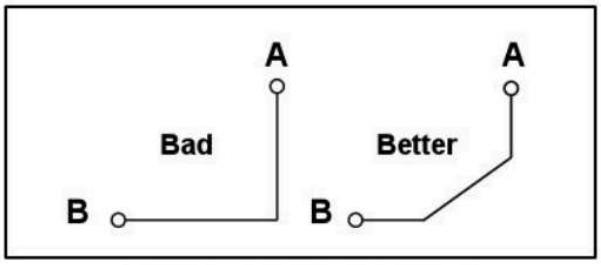


Figure 6. Signal Trace Angles

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. Clock and other high-speed signal traces must be as short as possible (less than 2.5 inches). It is better to have a ground plane under these traces. Using a GND plane to surround them is necessary.
- RXC and TXC are high speed (125MHz) signals; keep a 20mils spacing between clock and data signals.
- Match each RGMII TX and RX (RXC/RXD/RXCTL) group trace length to within 100mils.
- Route the RGMII traces at 50ohm impedance, and route via an inner layer to reduce radiation.
- Keep all RGMII traces as short as possible (less than 2.5 inches).
- All RGMII traces must be referenced to an unbroken ground plane.
- Place R1/C1 close to the RTL8211C(L), and R2/C2 close to the MAC (must be less than 500mils).

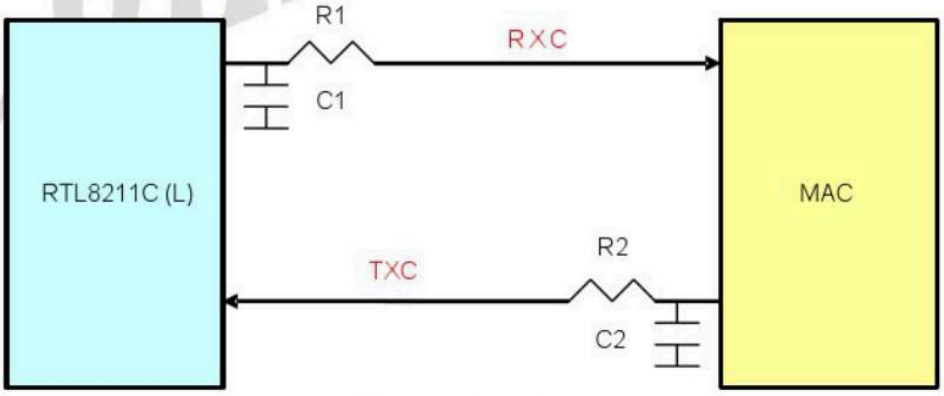


Figure 7. R1C1/R2C2 Placement

- Some return current paths, e.g., clock buffer and clock trace, can couple with the heat sink via parasitic

capacitance, then radiate to air from the heat sink. To avoid this, RGMII traces must be routed away from the heat sink.

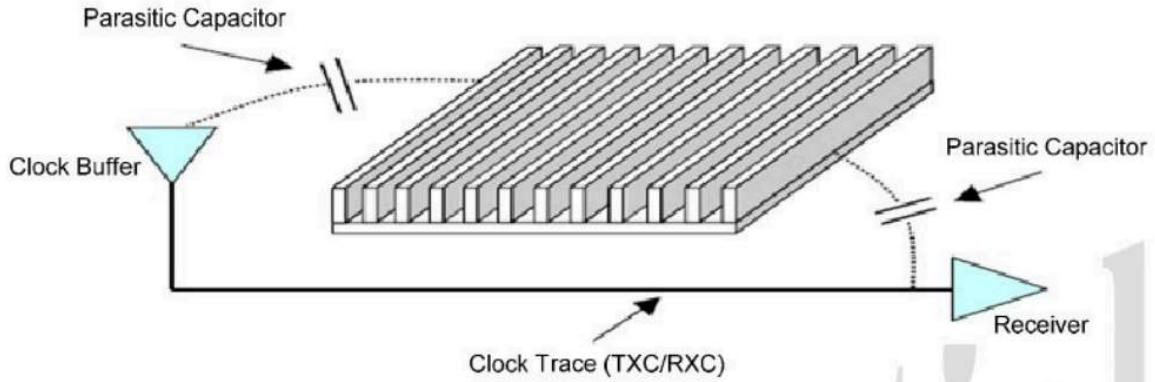


Figure 8. Clock and Heat Sink

- Route the RGMII traces away from I/O traces to avoid crosstalk (>20mils).

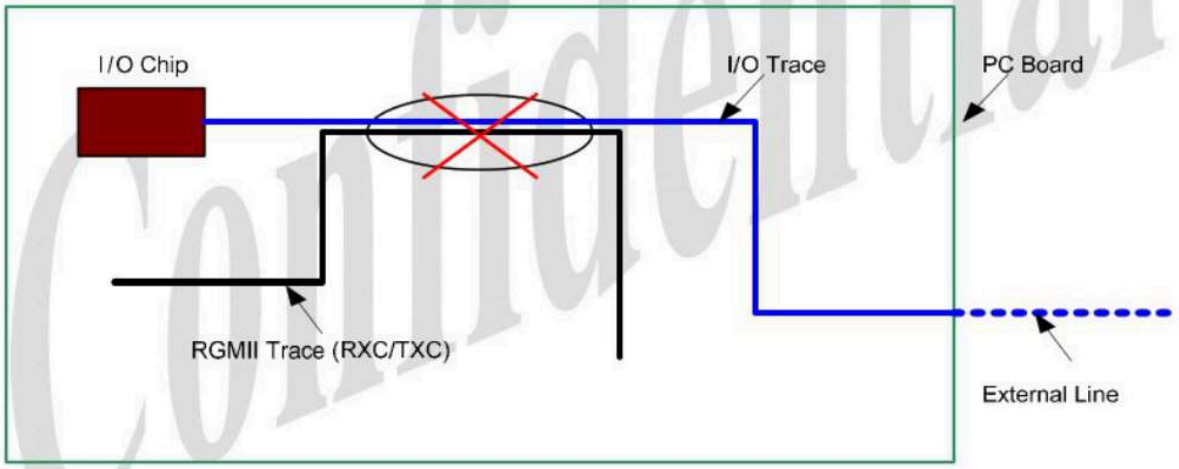


Figure 9. Clock and I/O Trace

- Reserve 2.5V power for RGMII use.

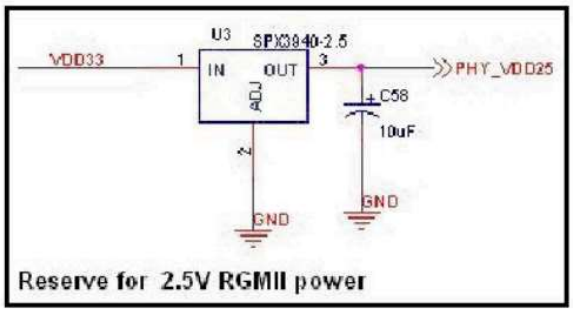


Figure 10. Reserve 2.5V Power for RGMII Use

- The RTL8211C (64-Pin QFN) uses Pin18 and Pin23 for 2.5V RGMII.
- The RTL8211CL (48-Pin LQFP) uses Pin15 and Pin21 for 2.5V RGMII.

3.4. Power Signals

The power supply into the RTL8211C(L) digital power pins can be improved with de-coupling capacitors. The power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the RTL8211C(L) need to be de-coupled with a capacitor. The de-coupling capacitors must be placed close to the RTL8211C(L) (<200 mils), and the traces should be kept short.

4. PCB Stack-Up

4.1. Overview

PCB stack-up is a major factor affecting the EMC performance of a product. A good stack-up can be very effective in reducing radiation from the loops on the PCB (differential-mode emission), as well as the cables attached to the board (common-mode emission). On the other hand, a poor stack-up can increase the radiation from both of these mechanisms considerably.

When using a multi-layer board, there are four main objectives to achieve:

1. Power and Ground planes should be coupled as closely as possible.

2. A signal layer should always be adjacent to a plane, and should be tightly coupled (close) to the adjacent plane.

3. High-speed signals (RGMII traces) must be routed on buried layers between planes so that the planes can act as shields and contain any radiation from the high-speed traces.

4. Multiple ground planes are very advantageous, since they will lower the ground (reference plane) impedance of the board and reduce the common-mode radiation.

The following are some recommendations to improve EMI performance.

4.2. Four-Layer Stack-Up (Motherboard Application)

- MDI and RGMII signals are routed on layer 4 and reference layer 3 (GND plane)

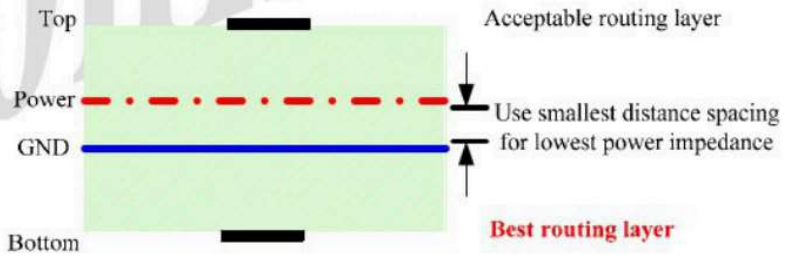


Figure 11. Four-Layer Stack-Up

4.3. Six-Layer Stack-Up (Notebook Application)

- RGMII signals are routed on layer 4 (IN2) and reference layer 5 (GND plane)

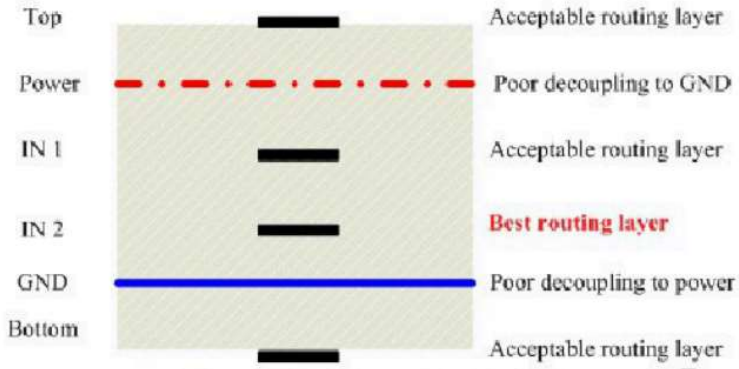


Figure 12. Six-Layer Stack-Up (A)

- RGMII signals are routed on layer 4 (IN1) and reference layer 3 (GND plane)

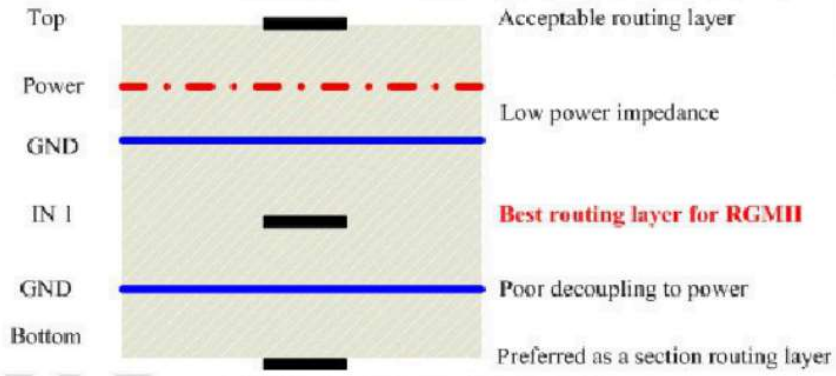


Figure 13. Six-Layer Stack-Up (B)

- RGMII signals are routed on layer 3 (IN1) and reference layer 2 (GND plane)

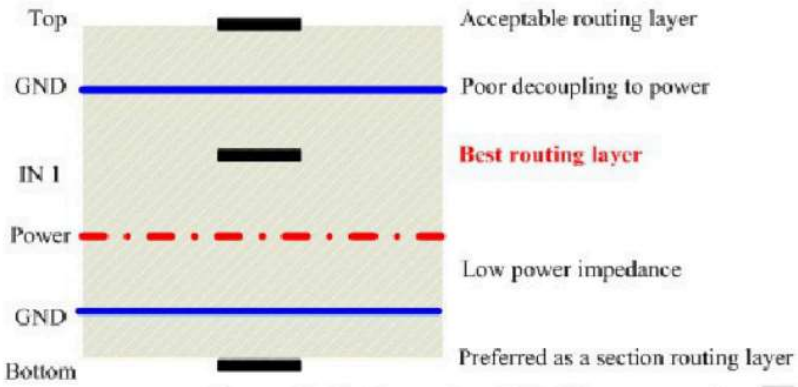


Figure 14. Six-Layer Stack-Up (C)

4.4. *Eight-Layer Stack-Up (Notebook Application)*

- RGMII signals are routed on layer 3 (IN1) or layer 6 (IN3), and reference layer 2 (GND plane) or layer 7 (GND plane)

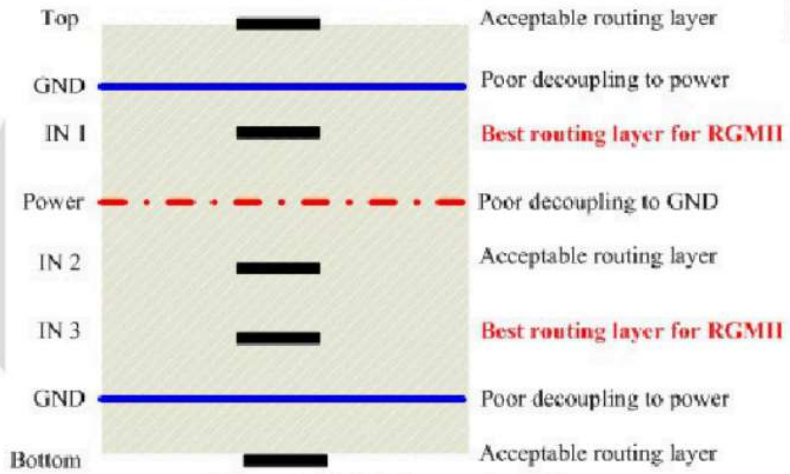


Figure 15. Eight-Layer Stack-Up

5. Ground Plane Layout

Isolated separation between Analog and Digital Ground domains is not recommended, as bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

The RTL8211C(L) has only a single ground plane for analog power (AVDD33 and AVDD12) and digital power (DVDD33, DVDD12). In the center of the IC, there is an Exposed Pad (EPAD) ground. The size of the center EPAD ground is 5.6mm x 5.6mm. The PCB layout requires 9 vias to connect the EPAD to the lower layer ground plane (see Figure 16).

Note: E-pad GND is on the RTL8211C only.

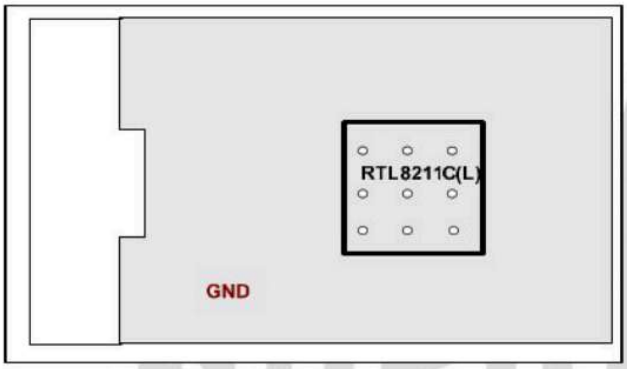


Figure 16. Ground Plane Layout-1

To achieve better ground plane performance, it is recommended to keep the plane as large and uniform as possible. Figure 17 illustrates a not so good (left) and a good ground plane layout (right).

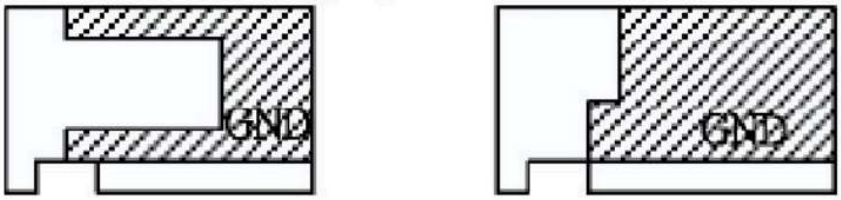


Figure 17. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer-induced noise away from the power and system ground planes (Figure 18).

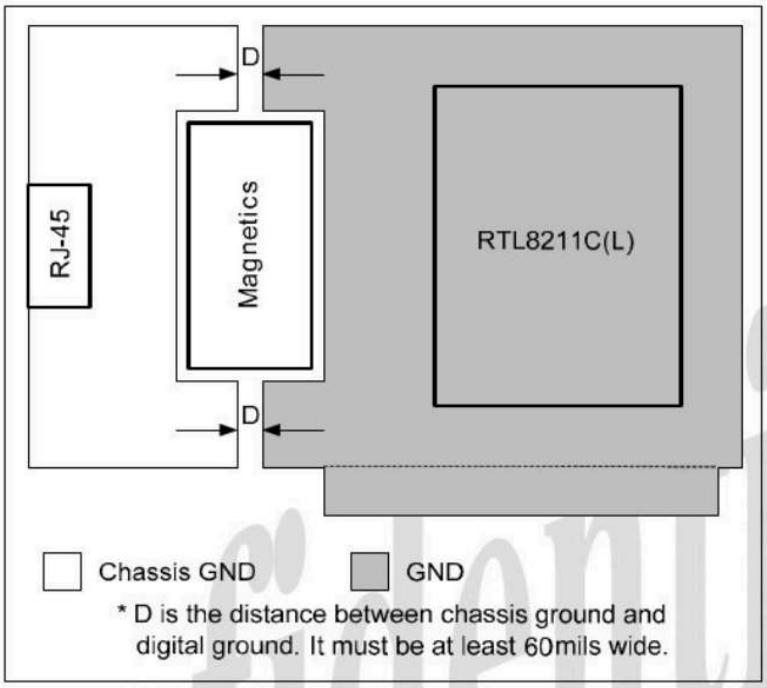


Figure 18. Ground Plane Separation

The Chassis Ground as shown in Figure 18 is known as an 'Isolated Ground'. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, a 2kV (3kV recommended) high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

It is important to keep the gap (D in Figure 18) between Chassis GND and System GND wider than 60mils for better isolation.

5.1. Four-Layer Board Ground Plane Layout (Typical Application)

1. Signal 1 (top layer)

2. Power (Keep GND area for RTL8211C(L))

3. GND

4. Signal 2 (bottom)

5.1.1. Ground Plane Layer 1 Layout

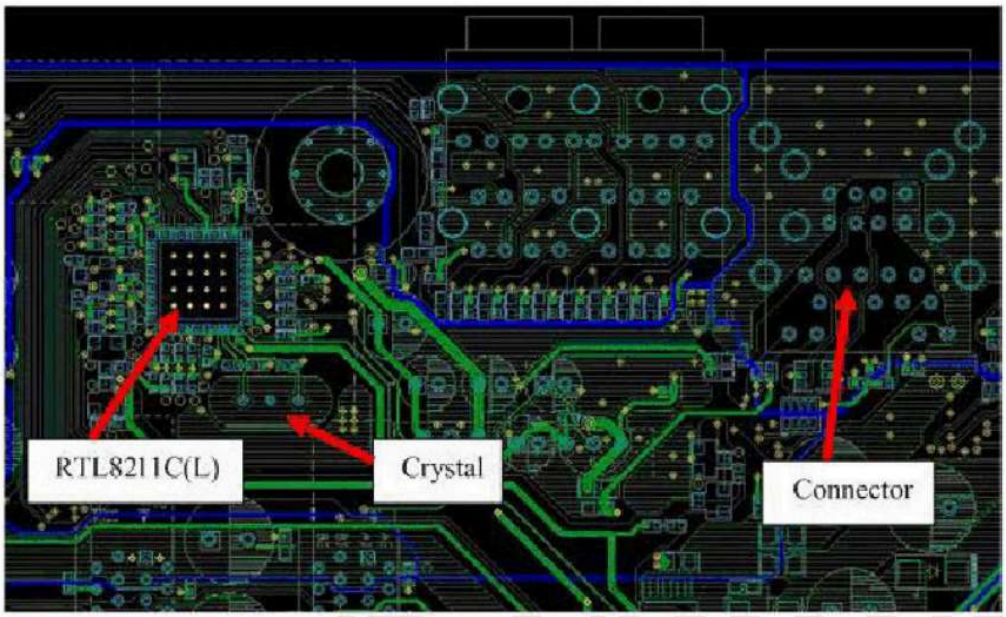


Figure 19. Ground Plane Layer 1 Layout

5.1.2. Ground Plane Layer 2 Layout

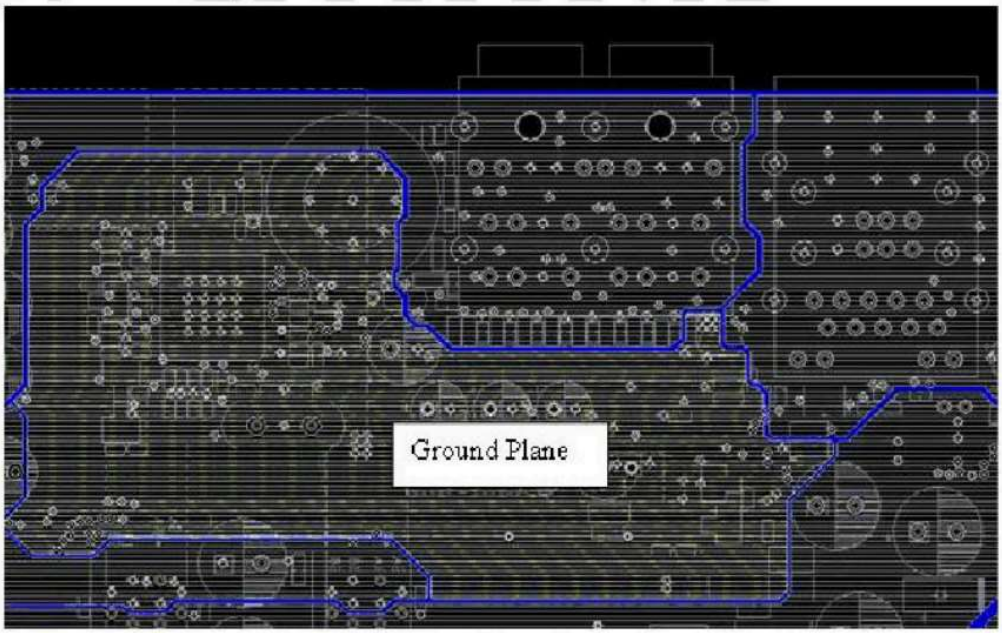


Figure 20. Ground Plane Layer 2 Layout

5.1.3. Ground Plane Layer 3 Layout

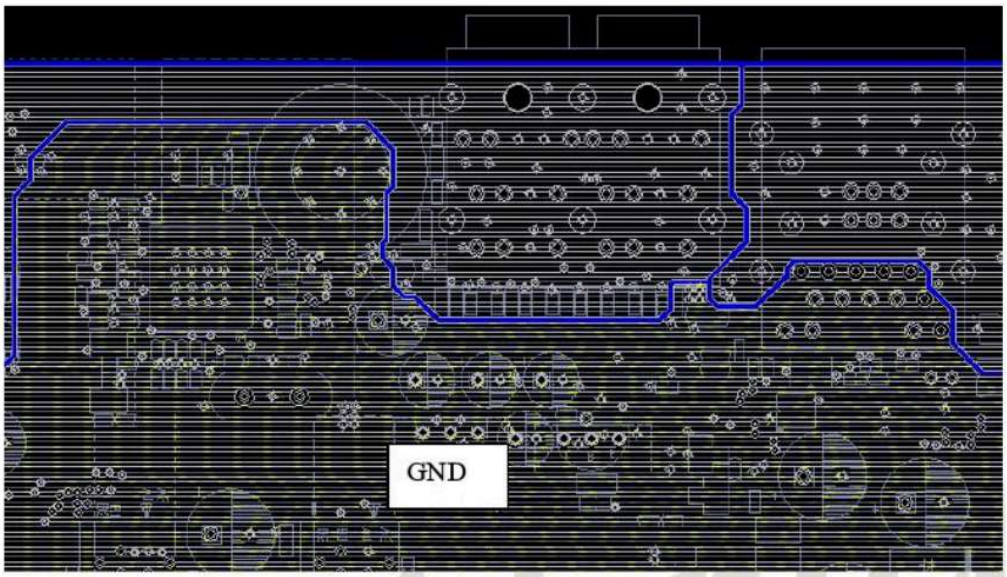


Figure 21. Ground Plane Layer 3 Layout

5.1.4. Ground Plane Layer 4 Layout

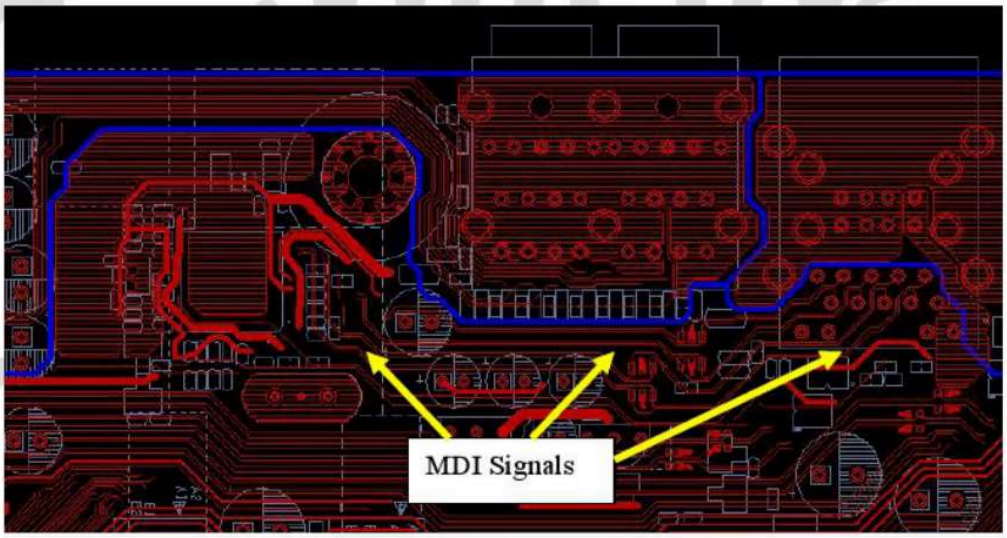


Figure 22. Ground Plane Layer 4 Layout

6. Power Plane Layout

It is recommended to use at least a 4-layer PCB. The digital power plane should be separated from analog areas, which are extremely sensitive to noise.

Any analog circuitry on the same plane as the digital power will experience an energy fluctuation due to the fast switching time of digital components. This could improperly bias transistors, and cause the circuits to malfunction. A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration (Figure 23). Keep power traces to the RTL8211C(L) as short and wide as possible and make good use of vias.

(a) Keep the Digital Power Plane as a whole, and leave some space for the Analog Power Plane

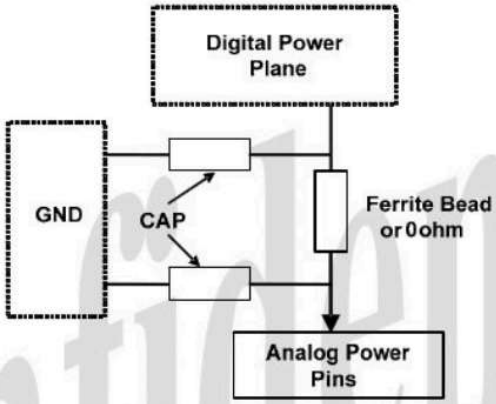


Figure 23. Power Plane

(b) Decoupled Capacitor Example

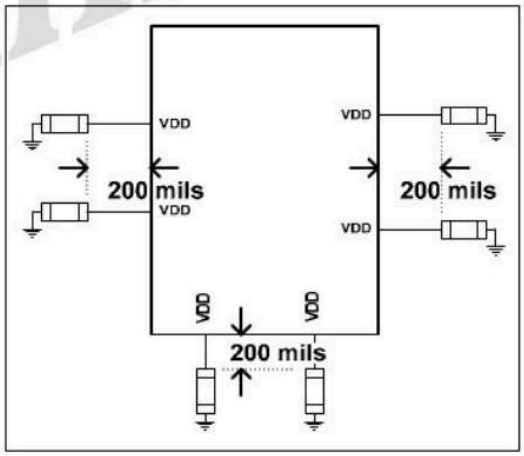


Figure 24. Decoupled Capacitor Example

To improve the performance of the power plane, try to keep the contact area between the RTL8211C(L) VDD pins and power plane as large as possible rather than using small narrow traces (Figure 25).

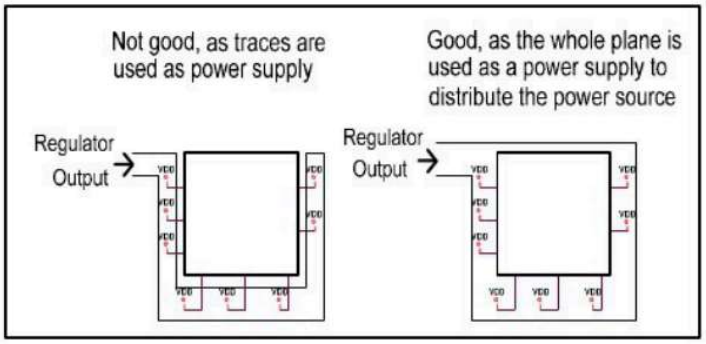


Figure 25. Power Source Distribution

- The power noise levels must be kept below 100mV in gigabit mode.
- All 3.3V/1.2V decoupling capacitors shown in the reference schematic, available from Realtek, should be used in all designs.
- The DVDD33 power (3.3V) plane must be kept as whole and as large as possible.

6.1. Power Plane Layer 1 Layout

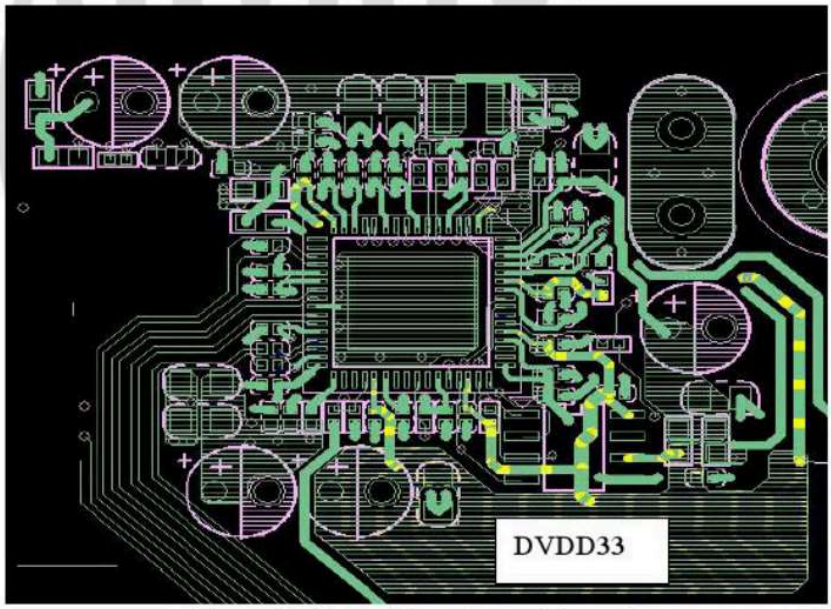


Figure 26. Power Plane Layer 1 Layout

6.2. Power Plane Layer 4 Layout

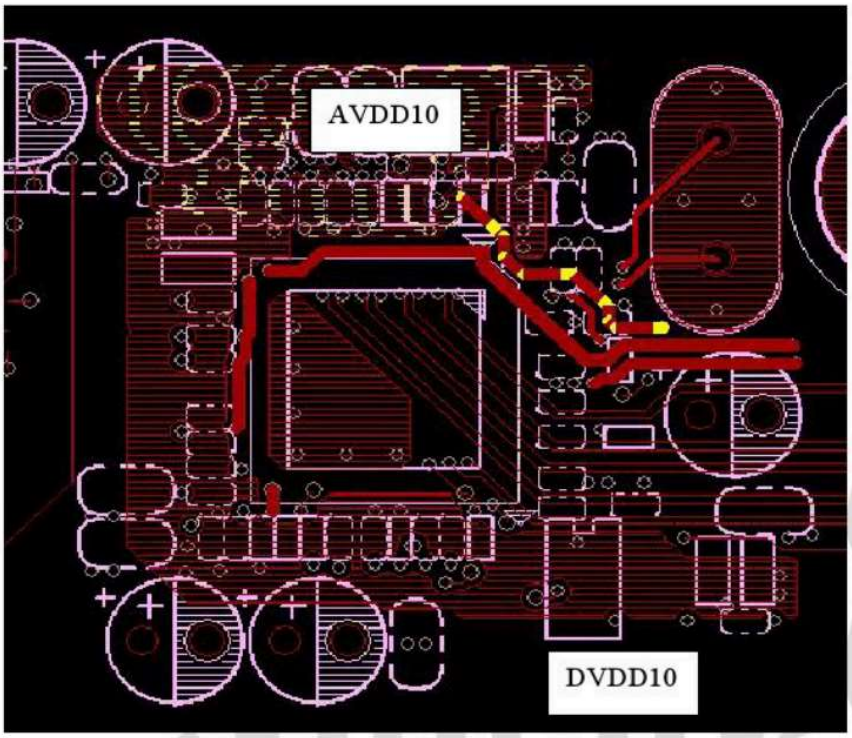


Figure 27. Power Plane Layer 4 Layout

7. Center-Tapping

- A center-tapped fine-tuned capacitor (C1 Value: 0.1μF~10pF) can improve EMI for single tone noise. The capacitor default is NC.
- Changing the R1 resistor to a capacitor (Value: 0.1μF~10pF), and fine-tuning the connection to GND can improve EMI for single tone noise. The resistor default is 0 ohm.

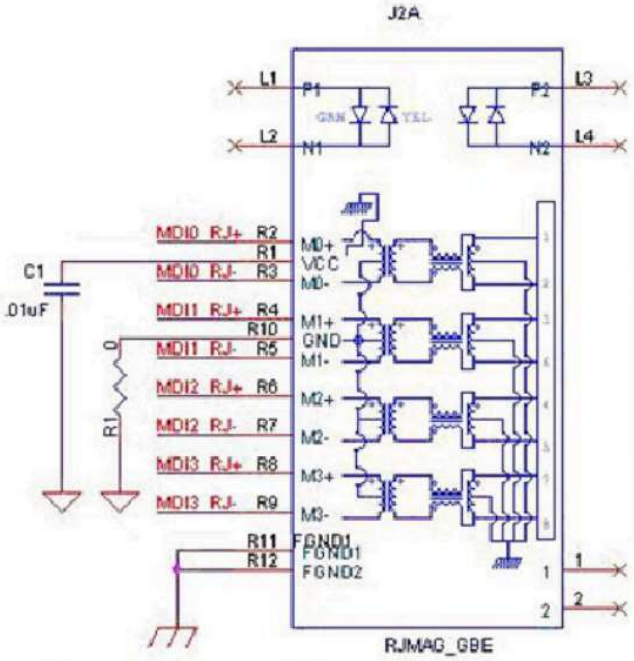
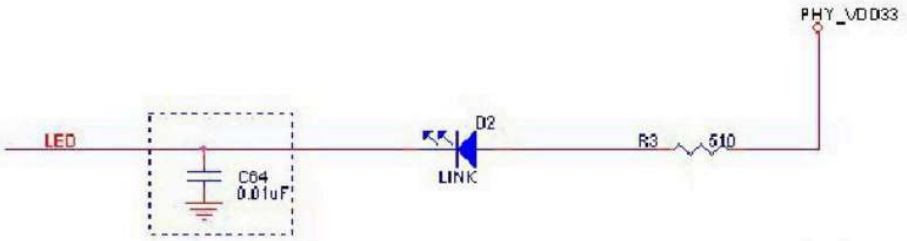


Figure 28. Center-Tapping

8. LED Pins

- Reserve a decoupling capacitor (D-CAP) for LED pins, and place close to the LAN connector (Refer to the reference schematic, available from Realtek).



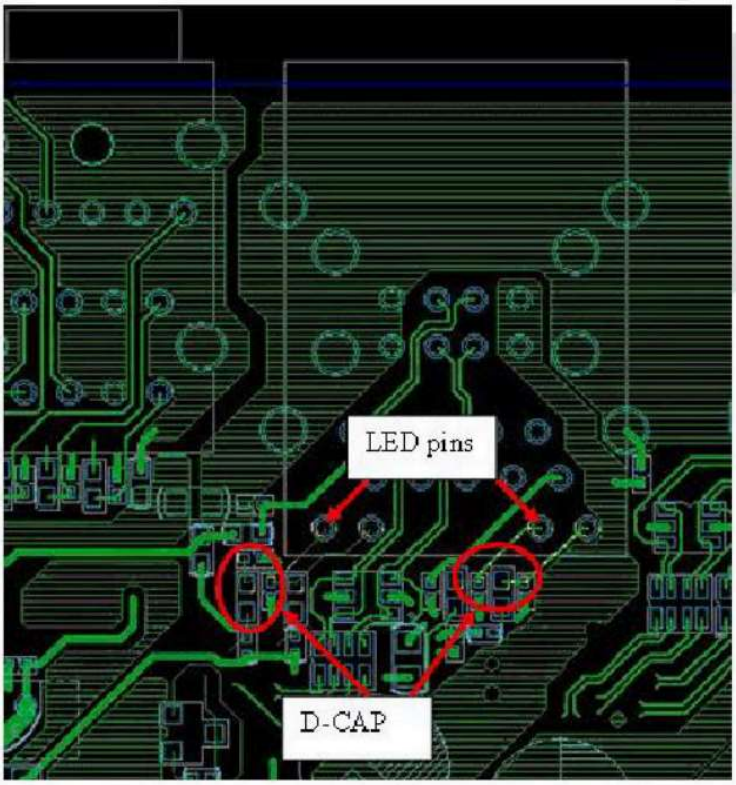


Figure 29. LED Pins

9. Switching Regulator

The RTL8211C(L) incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The 1.05V switching regulator output pin (REG_OUT) should be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

9.1. PCB Layout

- The input 3.3V power trace connected to VDDREG must be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) must be placed within 200mils (0.5cm) of VDDREG to prevent input voltage overshoot and reduce input noise.
- The output power trace out of REG_OUT must be wider than 60mils.
- L1 (4.7µH) must be kept within 200mils (0.5cm) of REG_OUT.
- C18 (X5R) and C19 must be kept within 200mils (0.5cm) of L1 to ensure stable output power and better power efficiency.
- For switching regulator stability, the capacitor C18 and C82 must be a ceramic (X5R) capacitor. C19 and C83 are recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.

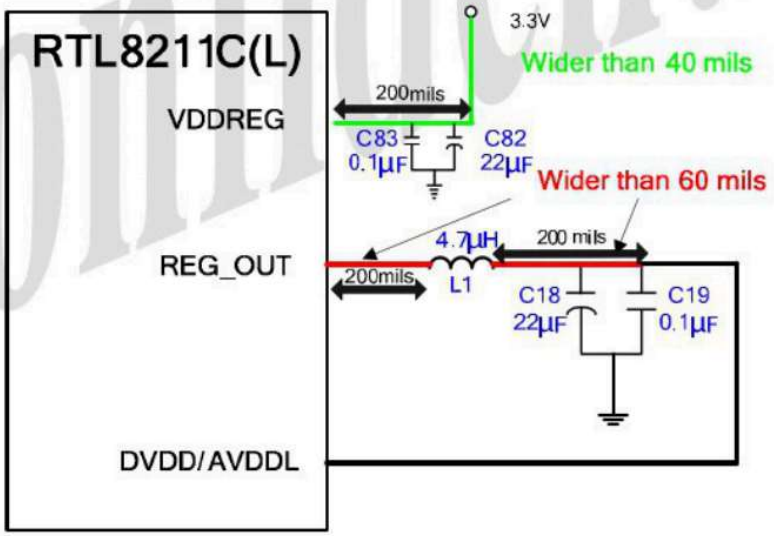


Figure 30. Switching Regulator Illustration

Note: RTL8211C Pin1=REG_OUT. Pin63=VDDREG.
RTL8211CL Pin48=REG_OUT. Pin44 and Pin45=VDDREG (two pins for VDDREG).

9.2. Inductor and Capacitor Parts List

Table 1. Inductor and Capacitor Parts List

Inductor Type	Inductance	Q at 500KHz	ESR at 500KHz (mΩ)	Max I (mA)	Output Ripple (mV)
4R7GTSD32	5.1µH	57.15	281	1100	12.6
6R8GTSD32	6.7µH	67.35	313	900	12
6R8GTSD53	7.1µH	59.7	375	1510	10.4

Note 1: The ESR is equivalent to RDC or DCR. Lower ESR inductor values will promote a higher efficiency switching regulator.

Note 2: The power inductor used by the switching regulator must be capable of handling 600mA of current.

Note 3: Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency must be measured according to the method described in section 9.5 Efficiency Measurement, page 29.

Capacitor Type	Capacitance	ESR at 500KHz (mΩ)	Output Ripple (mV)	Load Transient (mV)
22µF 1210 TDK	21.5µF	24.25	9.6	81.0
22µF 1210 X5R	22.15µF	24.90	10.4	73.0

Note: C18 and C82 must be X5R ceramic. Capacitors C19 and C83 are suggested to be ceramic, as lower ESR values will yield lower output voltage ripple.

9.3. Measurement Criteria

In order for the switching regulator to operate properly, the input and output voltage measurement criteria must be met. From the input side, the voltage overshoot cannot exceed 4V; otherwise the chip may be damaged. Note that the voltage signal must be measured directly at VDDREG, not at the capacitor. In order to reduce the input voltage overshoot, the C82 and C83 must be placed close (<200 mils) to VDDREG. The following figures show what a good input voltage and a bad one look like.

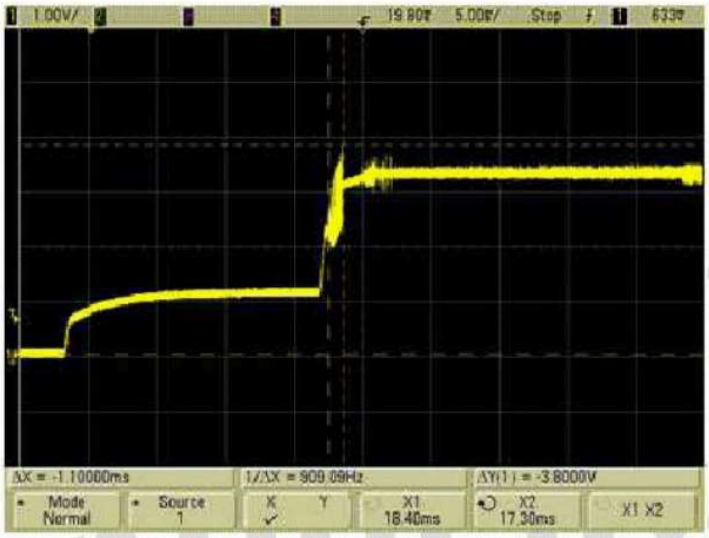


Figure 31. Input Voltage Overshoot <4V (Good)

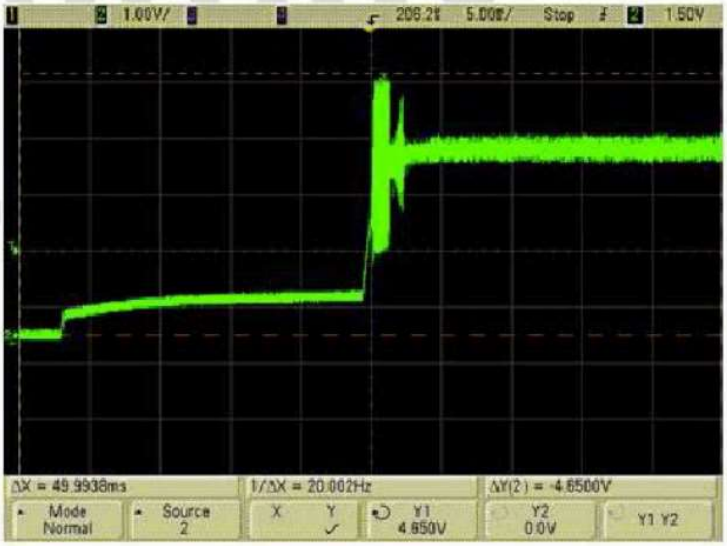


Figure 32. Input Voltage Overshoot >4V (Bad)

From the output side measured at REG_OUT, the voltage ripple must be within 100mV. Choosing different types and values of output capacitor (C18, C19) and power inductor (L1) will seriously affect the efficiency and output voltage ripple of switching regulators. The following figures show the effects of different types of capacitors on the switching regulator's output voltage.

The blue square wave signal (top row) is measured at the output of REG_OUT before the power inductor (L1). The yellow signal (second row) is measured after the power inductor (L1), and shows there is a voltage ripple. The green signal (lower row) is the current. Data in the following figures was measured at gigabit speed.

Figure 33. Ceramic 22μF 1210(X5R) (Good)

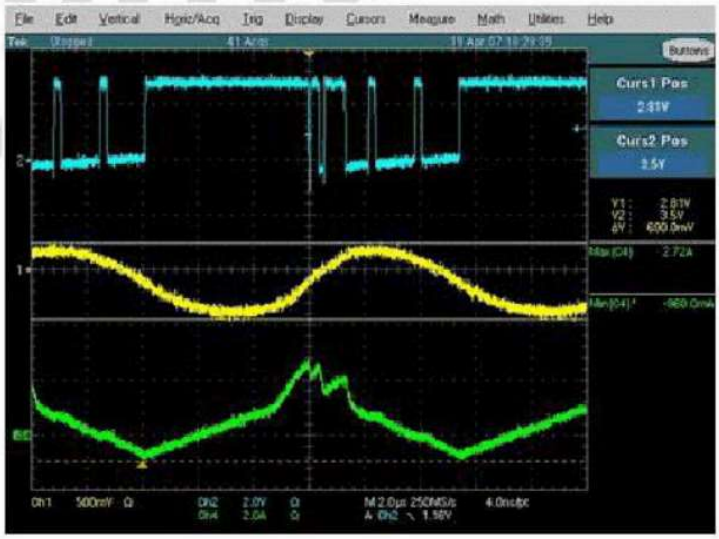


Figure 34. Ceramic 22μF 0805(Y5V) (Bad)

A ceramic 22µF (X5R) will have a lower voltage ripple compared to the electrolytic 100µF. The key to choosing a proper output capacitor is to choose the lowest ESR to reduce the output voltage ripple. Choosing a ceramic 22µF 0805 (Y5V) in this case will cause malfunction of the switching regulator.

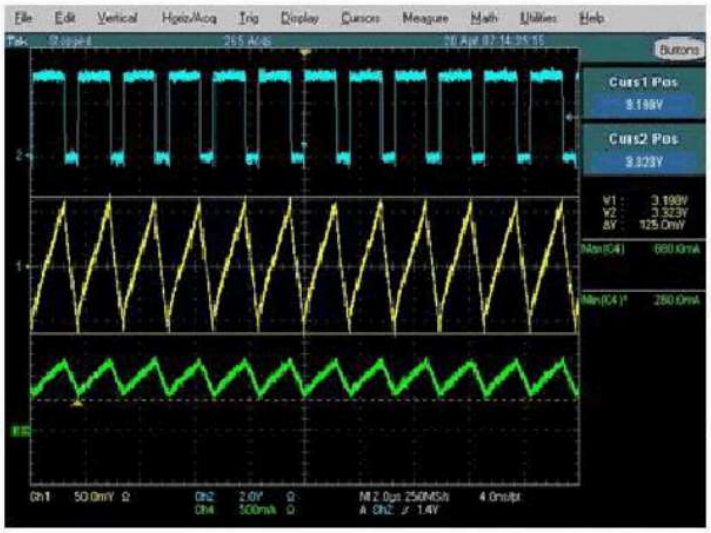


Figure 35. Electrolytic 100µF (Ripple Too High)

The following figures show how different inductors affect the REG_OUT output waveform. The typical waveform should look like Figure 36, which has a square waveform with a dip at the falling edge and the rising edge. If the inductor is not carefully chosen, the waveform may look like Figure 37, where the waveform looks like a distorted square. This will cause insufficient current supply and will undermine the stability of the system at gigabit speed. Data in the following figures was measured at gigabit speed.

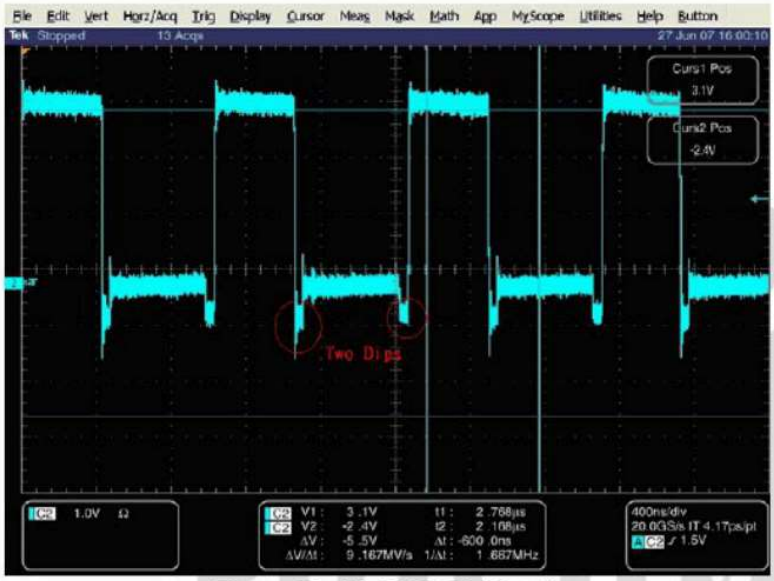


Figure 36. 4R7GTSD32 (Good)

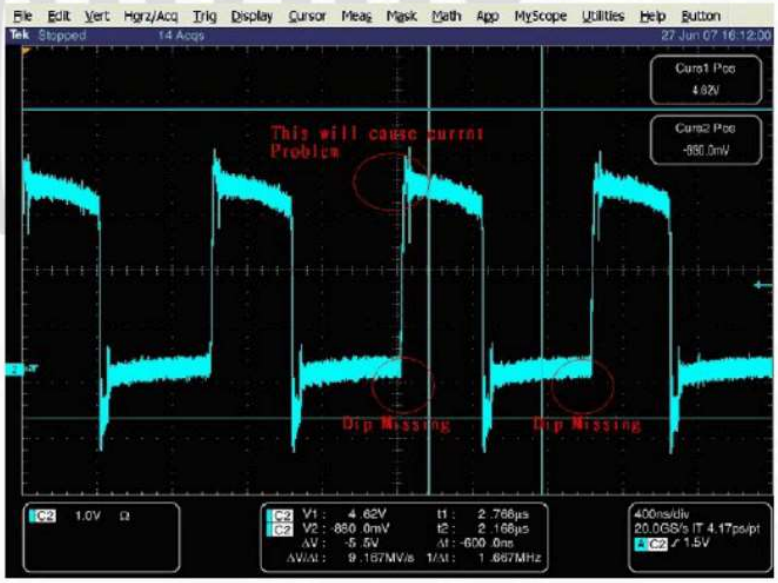


Figure 37. 1μH Bead (Bad)

9.4. Typical Switching Regulator PCB Layout

The typical layout of Figure 38 and Figure 39 are similar. The trace from RSET should pass through a via to the lower layer, and the trace should be protected by a ground trace. The width of the ground trace should be more than 5mils.

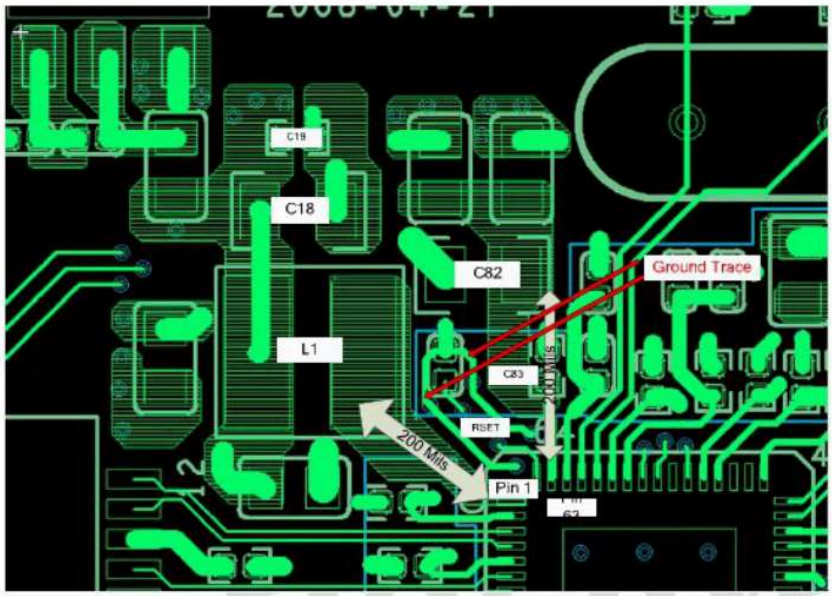


Figure 38. 64-Pin Typical Switching Regulator PCB Layout (Top Layer)

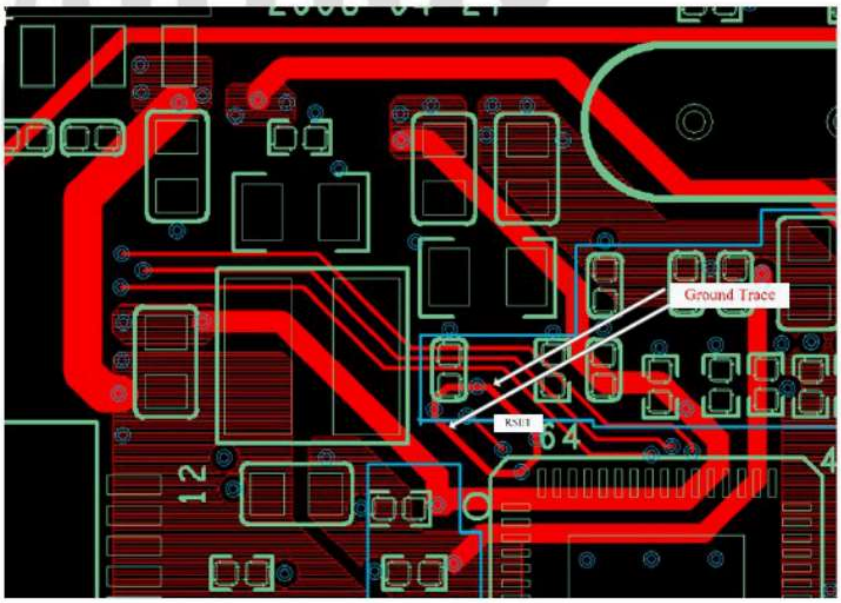


Figure 39. 64-Pin Typical Switching Regulator PCB Layout (Bottom Layer)

9.5. Efficiency Measurement

The efficiency of the switching regulator is designed to be above 75% in gigabit traffic mode. It is very important to choose a suitable inductor before Gerber certification, as the Inductor ESR value will affect the efficiency of the switching regulator. An inductor with a lower ESR value will result in a higher efficiency switching regulator.

The efficiency of the switching regulator is easily measured using the following method.

Figure 40 shows two checkpoints, checkpoint A (CP_A) and checkpoint B (CP_B). The switching regulator input current (Icpa) should be measured at CP_A, and the switching regulator output current (Icpb) should be measured at CP_B.

To determine efficiency, apply the following formula:

Efficiency = Vcpb*Icpb / Vcpa*Icpa

Where Vcpb is 1.05V; Vcpa is 3.3V. The measurements should be performed in gigabit traffic mode.

For example: The inductor used in the evaluation board is a GOTREND GTSD32-4R7M:

- The ESR value @ 1MHz is approximately 0.712ohm
- The measured Icpa is 160mA at CP_A
- The measured Icpb is 400mA at CP_B

These values are measured in gigabit traffic mode, so the efficiency of the GOTREND GTSD32-4R7M can be calculated as follows:

Efficiency = (1.05 V*400mA) / (3.3V*160mA) = 0.80 = 80%.

We strongly recommend that when choosing an inductor for the switching regulator, the efficiency should be measured, and that the inductor should yield an efficiency rating higher than 75%. If the efficiency does not meet this requirement, there may be risk to the switching regulator reliability over the long term.

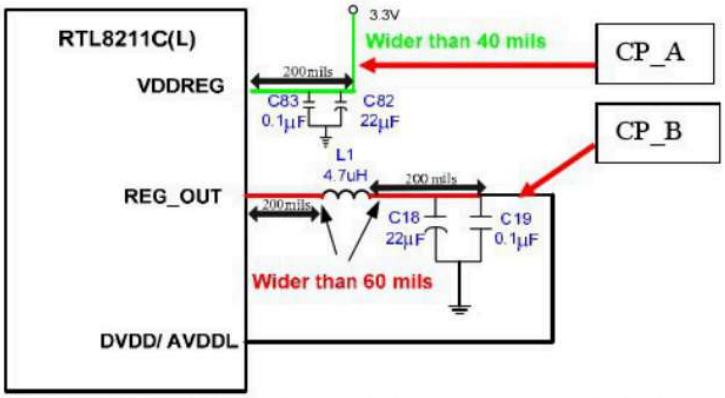


Figure 40. Switching Regulator Efficiency Measurement Checkpoint

10. Parts Recommendations

10.1. 10/100/1000M Magnetic

Turn Ratio Tx/Rx: 1:1

Primary Inductance: 350µH OCL with 8mA bias

Insertion Loss: -1.0 dB Max, 1 ~ 100MHz

Return Loss: -18dB Min @ 100Ω, 1 ~ 30MHz

-14dB Min @ 100Ω, 30 ~ 60MHz

-12dB Min @ 100Ω, 60 ~ 80MHz

Differential to Common Mode Rejection:

-40dB Min @ 1 ~ 60MHz

-30dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature: 0°C to 70°C

Recommended Magnetics: Pulse H5007 or similar

10.2. Reference Clock

A 25MHz (within 50ppm) parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to XTAL1 and XTAL2. Shunt each crystal lead to ground with a 27pF capacitor.

Table 2. Reference Clock

Parameters	Range
Frequency	25MHz
Temperature Stability	±10ppm
Duty Cycle	50% ±10%
Tolerance	±50ppm
ESR	Max 30ohm
Aging	5ppm/year, max.

10.3. Resistors

Resistors that have tolerance requirements within 1% are strongly recommended. Refer to the reference schematic, available from Realtek, for details.

10.4. Capacitors

For switching regulator power filtering, an X5R ceramic capacitor is recommended for the power circuit.

10.5. Power Inductor

The power inductor used by the switching regulator must be capable of handling 600mA of current, and the resistance value should be as small as possible to achieve the expected switching regulator efficiency which must be higher than 75%.

Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency must be measured according to the method described in section 9.5 Efficiency Measurement, page 29.

10.6. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

11. Special Notes

- Keep a void area of at least 100mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions.
- The RGMII traces are high-speed signal traces. For the best performance, be sure to follow all RGMII-specific layout guidelines.

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