RTL8150L
RTL8150LM

SINGLE-CHIP USB TO FAST ETHERNET CONTROLLER WITH MII INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.6	2009/04/20	Added confidential marking.

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1. General Description

The Realtek RTL8150L(M) is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides USB to Fast Ethernet capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. To achieve the most efficient power management, the RTL8150L(M) supports power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM). The RTL8150L(M) also supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft wake-up frame).

To connect to a Home PNA 1.0 PHY or HomePNA 2.0 PHY, the 100-pin RTL8150LM provides an MII interface supporting MII transmit clock from 0.1MHz to 25MHz.

For reduced BOM costs the RTL8150L(M) only requires one 25MHz crystal as its internal clock source, and requires no 'glue' logic or external memory.

The RTL8150L(M) keeps network maintenance cost low and eliminates usage barriers. It is the easiest way to connect a PC to the computer network without opening the cover, adding cards, reconfiguring software, or any of the other technicalities.

2. Features

- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
- Supports 10Mbps and 100Mbps N-way Auto-negotiation.
- Single-chip USB to Fast Ethernet controller
  - Compliant to USB interface ver 1.0/1.1.
  - Full-Speed (12Mbps) USB Device
  - Supports all USB standard commands
  - Supports Suspend/Resume detection logic
  - Supports 4 endpoints
    - 1 control endpoint with maximum 8-byte packet
    - 1 bulk IN endpoint with 64 bytes/packet
    - 1 bulk OUT endpoint with 64 bytes/packet
    - 1 interrupt IN endpoint with 8 bytes/packet
- RTL8150LM supports MII interface
- Supports Wake-On-LAN function and remote wakeup (Magic Packet, LinkChg, and Microsoft wake-up frame)
- Built in 18K bytes SRAM (2k bytes for Tx buffer, and 16k bytes for Rx buffer)
- Uses 93C46 to store resource configuration, ID parameter, etc.
- Supports LED pins for various network indications
- Half/Full duplex 10/100Mbps operation.
- Supports Full Duplex Flow Control (IEEE 802.3x)
- Uses 25MHz crystal as the internal clock source
- 5V power supply
- Packages
  - RTL8150L supports 48-pin LQFP
  - RTL8150LM supports 100-pins LQFP

3. Pin Assignments

3.1. Pin Assignments (RTL8150L)

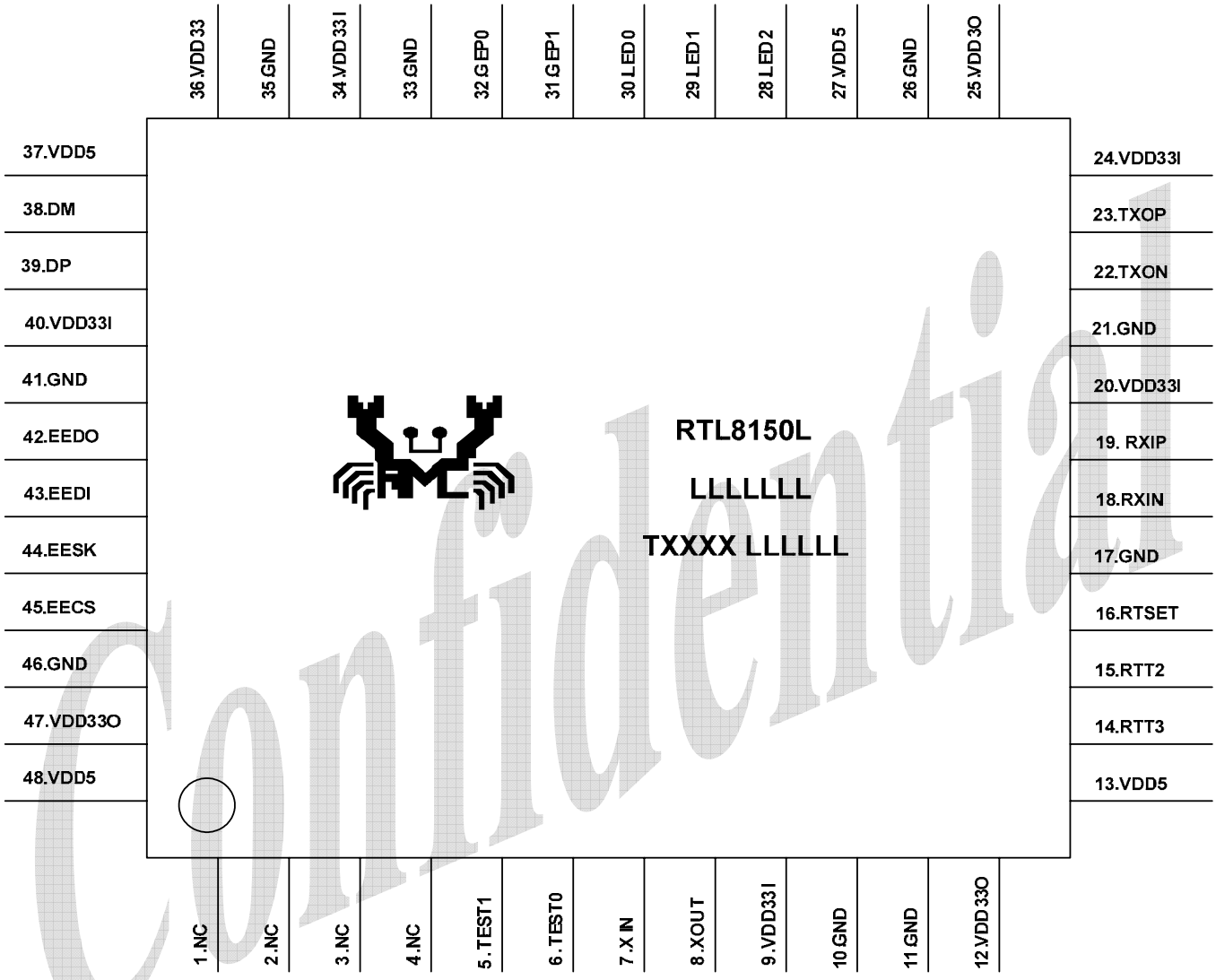


Figure 1. Pin Assignments (RTL8150L)

3.2. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in the illustration above.

3.3. Pin Assignments (RTL8150LM)

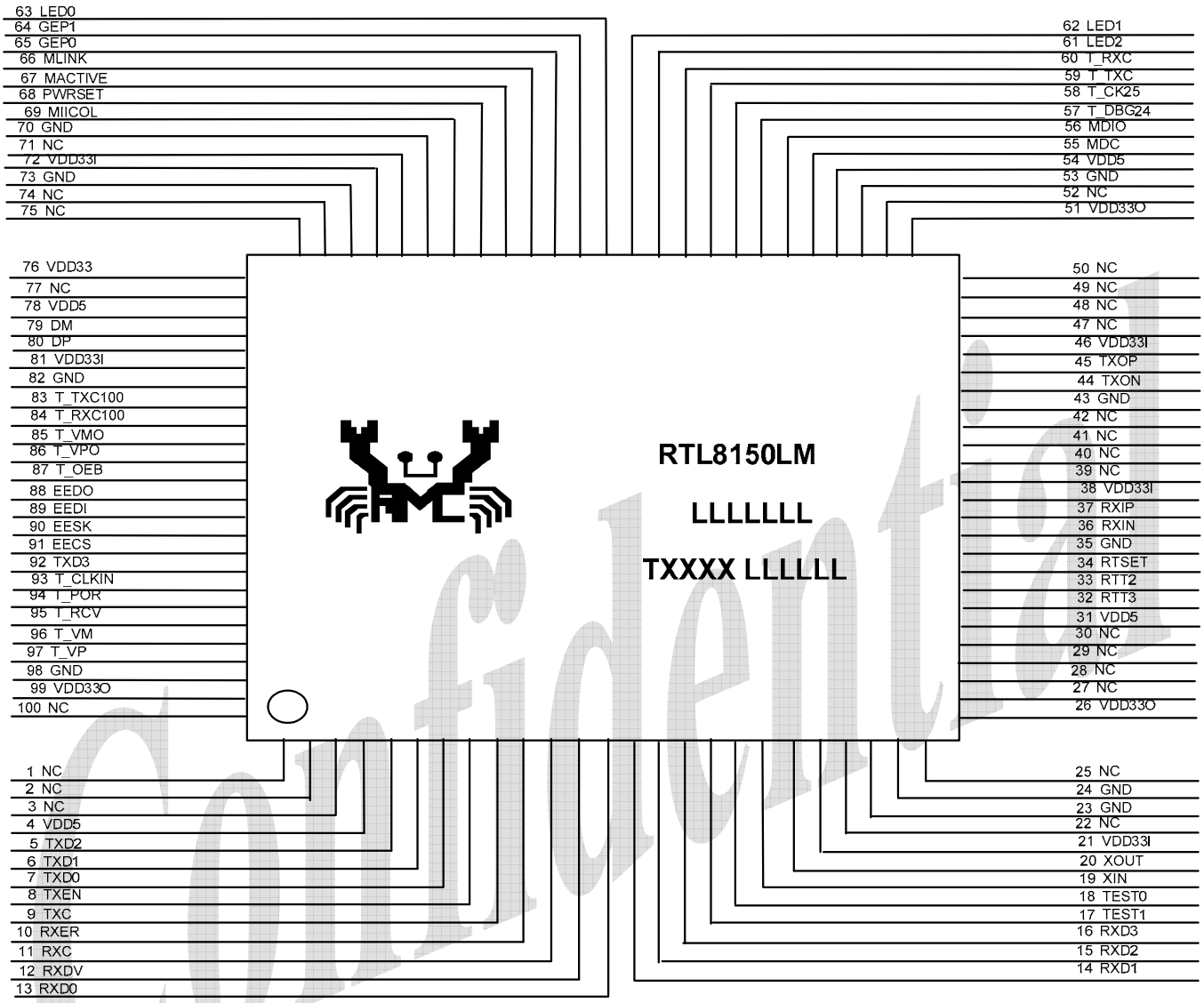


Figure 2. Pin Assignments (RTL8150LM)

3.4. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an ‘L’ in the location marked ‘T’ in the illustration above.

4. Pin Descriptions

4.1. RTL8150L Pin Descriptions

4.1.1. Power Pins

Table 1. Power Pins

Symbol	Type	Pin No	Description
VDD5	P	13, 27, 37, 48	5.0V Power Supply as Internal Regulators Input
VDD33O	P	12, 25, 47	3.3V Power Output from Internal Regulators Pin 47: Digital power
VDD33I	P	9, 20, 24, 34, 40	3.3V Power Pin 40: Digital power
GND	P	10, 11, 17, 21, 26, 33, 35, 41, 46	Ground
VDD33	P	36	3.3V Standby Power

4.1.2. USB Interface

Table 2. USB Interface

Symbol	Type	Pin No	Description
DM	I/O	38	Negative Data Line of USB Differential Data Bus
DP	I/O	39	Positive Data Line of USB Differential Data Bus

4.1.3. 10/100Base-T UTP Interface

Table 3. 10/100Base-T UTP Interface

Symbol	Type	Pin No	Description
TXD+	O	23	10/100Base-T Transmit Data
TXD-	O	22	10/100Base-T Transmit Data
RXIN+	I	19	10/100Base-T Receive Data
RXIN-	I	18	10/100Base-T Receive Data
X1	I	7	25MHz Crystal Input
X2	O	8	25MHz Crystal Output

4.1.4. LED INTERFACE

Table 4. LED INTERFACE

Symbol	Type	Pin No	Description
LED0, 1, 2	O	30, 29, 28	LED Pins (Active Low)

LEDS1-0	00	01	10	11
LED0	TX/RX	TX/RX	TX	TX/RX@ LINK10
LED1	LINK100	LINK10/100	LINK10/100	TX/RX@ LINK100
LED2	LINK10	FULL	RX	FULL

During power down mode, the LED‘s are OFF if SYSLED in configuration register 1 is set.

4.1.5. EEPROM INTERFACE

Table 5. EEPROM INTERFACE

Symbol	Type	Pin No	Description
EECS	O	45	93C46 Chip Select
EESK	O	44	93C46 Clock
EEDI	O	43	93C46 Data Input
EEDO	I	42	93C46 Data Output

4.1.6. Test And Other Pins

Table 6. Test And Other Pins

Symbol	Type	Pin No	Description
RTT2-3	TEST	15, 14	Chip Test Pins
TEST0-1	TEST	6, 5	Chip Test Pins
RTSET	I/O	16	This Pin Must be Pulled Low by a 1.69KΩ Resistor
GEP0-1	I/O	32, 31	General Purpose Pin 0, 1
NC	-	1, 2, 3, 4	Reserved

4.2. RTL8150LM Pin Descriptions

4.2.1. RTL8150LM Power Pins

Table 7. RTL8150LM Power Pins

Symbol	Type	Pin No	Description
VDD5	P	4, 31, 54, 78	5.0V Power Supply as Internal Regulators Input
VDD33O	P	26, 51, 99	3.3V Power Output from Internal Regulators Pin 99: Digital power
VDD33I	P	21, 38, 46, 72, 81	3.3V Power Pin 81: Digital power
GND	P	23, 24, 35, 43, 53, 70, 73, 82, 98	Ground
VDD33	P	76	3.3V Standby Power

4.2.2. RTL8150LM USB INTERFACE

Table 8. RTL8150LM USB INTERFACE

Symbol	Type	Pin No	Description
DM	I/O	79	Negative Data Line of USB Differential Data Bus
DP	I/O	80	Positive Data Line of USB Differential Data Bus

4.2.3. RTL8150LM 10/100Base-T UTP INTERFACE

Table 9. RTL8150LM 10/100Base-T UTP INTERFACE

Symbol	Type	Pin No	Description
TXD+	O	45	10/100Base-T Transmit Data
TXD-	O	44	10/100Base-T Transmit Data
RXIN+	I	37	10/100Base-T Receive Data
RXIN-	I	36	10/100Base-T Receive Data
X1	I	19	25MHz Crystal Input
X2	O	20	25MHz Crystal Output

4.2.4. RTL8150LM MII INTERFACE

Table 10. RTL8150LM MII INTERFACE

Symbol	Type	Pin No	Description
RXD0-3	I	13, 14, 15, 16	MII Receive Data 0-3
TXD0-3	O	7, 6, 5, 92	MII Transmit Data 0-3
TXC	I	9	MII Transmit Clock: 25MHz or 2.5MHz Tx clock supplied by the external PMD device.
MIICOL	I	69	MII Collision Detected: This signal is asserted high synchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
TXEN	O	8	MII Transmit Enable: Indicates the presence of valid nibble data on TXD[3:0].
RXC	I	11	MII Receive Clock: 25MHz or 2.5MHz Rx clock supplied by the external PMD device.
RXDV	I	12	MII Receive Data Valid: Data valid is asserted by an external PHY when receive data is present on the RXD[3:0], and it is de-asserted at the end of the packet. This signal is valid on the rising edge of the RXC.
RXER	I	10	MII Receive Error: This pin is asserted to indicate that invalid symbol has been detected in 100Mbps MII mode. This signal is synchronized to RXC and can be asserted for a minimum of one receive clock.
MDC	O	55	MII Management Data Clock: Synchronous clock for MDIO data transfer.
MDIO	I/O	56	MII Management Data: Bi-directional signal used to transfer management information.
Mlink	I	66	MII Link Status Notification, Indicates to the MAC that External PMD is Link Ok or Not.
Mactiveb	I	67	MII Active Status Notification, when Mactiveb=High, Mlink is Low Active, and Vice Versa.

4.2.5. RTL8150LM LED INTERFACE

Table 11. RTL8150LM LED INTERFACE

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No</th><th>Description</th></tr>
<tr><td rowspan="5">LED0, 1, 2</td><td rowspan="5">O</td><td rowspan="5">63, 62, 61</td><td>LED Pins(Active Low)</td></tr>
<tr><td>
<table>
<tr><th>LEDS1-0</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>TX/RX</td><td>TX/RX</td><td>TX</td><td>TX/RX@ LINK10</td></tr>
<tr><td>LED1</td><td>LINK100</td><td>LINK10/100</td><td>LINK10/100</td><td>TX/RX@ LINK100</td></tr>
<tr><td>LED2</td><td>LINK10</td><td>FULL</td><td>RX</td><td>FULL</td></tr>
</table>
</td></tr>
<tr><td>During power down mode, the LED‘s are OFF if SYSLED in configuration register 0 is set.</td></tr>
</table>

4.2.6. RTL8150LM EEPROM INTERFACE

Table 12. RTL8150LM EEPROM INTERFACE

Symbol	Type	Pin No	Description
EECS	O	91	93C46 Chip Select
EESK	O	90	93C46 Clock
EEDI	O	89	93C46 Data Input
EEDO	I	88	93C46 Data Output

4.2.7. RTL8150LM TEST AND THE OTHER PINS

Table 13. RTL8150LM TEST AND THE OTHER PINS

Symbol	Type	Pin No	Description
RTT2-3	TEST	33, 32	Chip Test Pins
T_***	TEST	17, 18, 57, 58, 59, 60, 83, 84, 85, 86, 87, 93, 94, 95, 96, 97	Chip Test Pins
RTSET	I/O	34	This Pin Must be Pulled Low by a 1.69KΩ Resistor
GEP0-1	I/O	65, 64	General Purpose Pin 0, 1
PWRESETB	O	68	Power-On Reset for External PHY, Active Low
NC	-	1, 2, 3, 22, 25, 27, 28, 29, 30, 39, 40, 41, 42, 47, 48, 49, 50, 52, 71, 74, 75, 77, 100	Reserved

5. SIE–USB Commands

5.1. Vender Memory Read

Table 14. Vender Memory Read

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
C0	05	regoffsetL	regoffsetH	00	00	LengL	LengH

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
reg0	reg1	reg2	reg3	reg4	reg5	reg6	reg7

Note: The total length response of the RTL8150L depends on (LengH, LengL) values.

5.2. Vender Memory Write

Table 15. Vender Memory Write

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
40	05	regoffsetL	regoffsetH	00	00	LenghL	LenghH

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
reg0	reg1	reg2	reg3	reg4	reg5	reg6	reg7

Note: Offset 0x1200 to 0x127f register must write by word mode.

5.3. Set Address

Table 16. Set Address

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
00	05	addrL	addrH	00	00	00	00

Data Transaction: None

5.4. Clear Feature EP0

Table 17. Clear Feature EP0

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
02	01	00	00	00	00	00	00

Data Transaction: None

5.5. Clear Feature EP1

Table 18. Clear Feature EP1

Setup Transaction

BmReq	breq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
02	01	00	00	81	00	00	00

Data Transaction: None

5.6. Clear Feature EP2

Table 19. Clear Feature EP2

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
02	01	00	00	02	00	00	00

Data Transaction: None

5.7. Clear Feature EP3

Table 20. Clear Feature EP3

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
02	01	00	00	83	00	00	00

Data Transaction: None

5.8. Set Feature EP1

Table 21. Set Feature EP1

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
02	03	00	00	81	00	00	00

Data Transaction: None

5.9. Set Feature EP2

Table 22. Set Feature EP2

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
02	03	00	00	02	00	00	00

Data Transaction: None

5.10. Set Feature EP3

Table 23. Set Feature EP3

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
02	03	00	00	00	83	00	00

Data Transaction: None

5.11. Set Interface 0

Table 24. Set Interface 0

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
01	0B	00	00	00	00	00	00

Data Transaction: None

5.12. Set Feature Device

Table 25. Set Feature Device

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
00	03	01	00	00	00	00	00

Data Transaction: None

5.13. Clear Feature Device

Table 26. Clear Feature Device

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
00	01	01	00	00	00	00	00

Data Transaction: None

5.14. Set Config 0

Table 27. Set Config 0

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
00	09	00	00	00	00	00	00

Data Transaction: None

5.15. Set Config 1

Table 28. Set Config 1

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
00	09	01	00	00	00	00	00

Data Transaction: None

5.16. Get Descriptor Device

Table 29. Get Descriptor Device

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
80	06	00	01	00	00	Lengh_L	Lengh_H

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
12	01	10	01	00	00	00	08
DA	0B	50	81	00	01	01	02
03	01	-	-	-	-	-	-

Note: The total length response of the RTL8150L depends on (LengH, LengL) values.

5.17. Get Descriptor Configuration

Table 30. Get Descriptor Configuration

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
80	06	00	02	00	00	Lengh_L	Lengh_H

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
09	02	27	00	01	01	00	A0
50	09	04	00	00	03	FF *	00
FF *	00	07	05	81	02	40	00
00	07	05	02	02	40	00	00
07	05	83	03	08	00	01	-

Note: The total length response of the RTL8150L depends on (LengH, LengL) values.
**The E version is 0xFF, before E version it is 0x00.*

5.18. Get Descriptor String Index 0

Table 31. Get Descriptor String Index 0

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
80	06	00	03	00	00	Lengh_L	Lengh_H

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
04	03	04	09	-	-	-	-

Note: The total length response of the RTL8150L depends on (LengH, LengL) values.

5.19. Get Descriptor String Index 1

Table 32. Get Descriptor String Index 1

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
80	06	01	03	09	04	Lengh_L	Lengh_H

Data Transaction (REALTEK)

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
10	03	52	00	45	00	41	00
4C	00	54	00	45	00	4B	00

Note: The total length response of the RTL8150L depends on (LengH, LengL) values.

5.20. Get Descriptor String Index 2

Table 33. Get Descriptor String Index 2

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
80	06	02	03	09	04	Lengh_L	Lengh_H

Data Transaction (USB 10/100 LAN)

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
1E	03	55	00	53	00	42	00
20	00	31	00	30	00	2F	00
31	00	30	00	30	00	20	00
4C	00	41	00	4E	00	-	-

5.21. Get Descriptor String Index 3

Table 34. Get Descriptor String Index 3

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	WindexH	wLengthL	wLengthH
80	06	03	03	09	04	Lengh_L	Lengh_H

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
0A	03	30	00	30	00	30	00
31	00	-	-	-	-	-	-

Note: The total length response of the RTL8150L depends on (LengH, LengL) values.

5.22. Get Config

Table 35. Get Config

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
80	08	00	00	00	00	01	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
Value	-	-	-	-	-	-	-

5.23. Get Status Device

Table 36. Get Status Device

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
80	00	00	00	00	00	02	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
Value	Value	-	-	-	-	-	-

5.24. Get Status EP0

Table 37. Get Status EP0

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
82	00	00	00	00	00	02	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
Value	Value	-	-	-	-	-	-

5.25. Get Status EP1

Table 38. Get Status EP1

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
82	00	00	00	81	00	02	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
Value	value	-	-	-	-	-	-

5.26. Get Status EP2

Table 39. Get Status EP2

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
82	00	00	00	02	00	02	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
Value	value	-	-	-	-	-	-

5.27. Get Status EP3

Table 40. Get Status EP3

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
82	00	00	00	83	00	02	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
Value	Value	-	-	-	-	-	-

5.28. Get Status Interface 0

Table 41. Get Status Interface 0

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
81	00	00	00	00	00	02	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
Value	value	-	-	-	-	-	-

5.29. Get Interface 0

Table 42. Get Interface 0

Setup Transaction

BmReq	bReq	wValueL	wValueH	wIndexL	wIndexH	wLengthL	wLengthH
81	0A	00	00	00	00	01	00

Data Transaction

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
value	-	-	-	-	-	-	-

6. Memory Allocation

$0000H~$011FH: Reserved
$0120H~$01FFH: RTL8150L(M) REGISTER
$1200H~$127FH: Serial EEPROM(9346)

Table 43. Memory Allocation

Offset	Type	Pin No	Description
0120h-0125h	RW*	IDR0-5	Ethernet Address, Loaded from 93C46
0126h-012Dh	RW	MAR0-7	Multicast Register
012Eh	RW	CR	Command Register
012Fh	RW	TCR	Transmit Configuration Register
0130-0131h	RW	RCR	Receive Configuration Register
0132h	RW	TSR	Transmit Status Register
0133h	RW	RSR	Receive Status Register
0134h	RW	Reserved	Reserved
0135h	RW*	CON0	Configuration Register0
0136h	RW*	CON1	Configuration Register1
0137h	RW	MSR	Medium Status
0138h	RW	PHYADD	MII PHY Address Select
0139-013Ah	RW	PHYDAT	MII PHY Data
013Bh	RW	PHYCNT	MII PHY Control
013Ch	RW	Reserved	Reserved
013Dh	RW*	GPPC	General Purpose Pin Control
013Eh	RW	WAKECNT	Wake Up Event Control
0140h-0141h	RW*	BMCR	Basic Mode Control Register
0142h-0143h	R	BMSR	Basic Mode Status Register
0144h-0145h	RW*	ANAR	Auto-Negotiation Advertisement Register
0146h-0147h	RW	ANLP	Auto-Negotiation Link Partner Ability Register
0148h-0149h	RW	AER	Auto-Negotiation Expansion Register
014Ah-014Bh	RW	NWayT	Nway Test Register
014Ch-014Dh	RW	CSCR	CS Configuration Register
014Eh-014Fh	RW	CRC0	Power Management CRC Register for Wakeup Frame0
0150h-0151h	RW	CRC1	Power Management CRC Register for Wakeup Frame1
0152h-0153h	RW	CRC2	Power Management CRC Register for Wakeup Frame2
0154h-0155h	RW	CRC3	Power Management CRC Register for Wakeup Frame3
0156h-0157h	RW	CRC4	Power Management CRC Register for Wakeup Frame4
0158h-015Fh	RW	BYEMASK0	Power Management Wakeup Frame0 (64bit) Bytemask
0160h-0167h	RW	BYEMASK 1	Power Management Wakeup Frame1 (64bit) Bytemask
0168h-016Fh	RW	BYEMASK 2	Power Management Wakeup Frame2 (64bit) Bytemask
0170h-0177h	RW	BYEMASK 3	Power Management Wakeup Frame3 (64bit) Bytemask
0178h-017Fh	RW	BYEMASK 4	Power Management Wakeup Frame4 (64bit) Bytemask
0180h-0183h	RW	PHY1	PHY Parameter 1
0184h	RW	PHY2	PHY Parameter 2
0186h-0189h	RW	TW1	Twister Parameter 1
018Ah-01ff	-	Reserved	Reserved

**: Denotes auto-loaded from 93C46 during chip initialization.*

7. Register Descriptions

7.1. Command Register (Offset 012Eh, RW)

Table 44. Command Register (Offset 012Eh, RW)

Bit	Symbol	Description	Default/ Attribute
7-6	-	Reserved	-
5	WEPROM	1: EEPROM write enable 0: Disable The EEPROM map from 0x1200 to 127fh. Write 0x1200 equal to program EEPROM offset 0x00. Write to EEPROM must use WORD mode access at a time. The read EEPROM has no limit.	0, RW
4	SOFT_RST	Reset: Setting to 1 forces the RTL8150L(M) to a software reset state that disables the transmitter and receiver, reinitializes the FIFOs, resets the system buffer pointer to the initial value , Rx buffer is empty). The values of IDR0-5 and MAR0-7 will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the RTL8150L(M) when the reset operation is complete.	0, RW
3	RE	Ethernet 10/100M Receive Enable	0, RW
2	TE	Ethernet 10/100M Transmit Enable	0, RW
1	EP3CLREN	1: Enable clearing the performance counter of EP3 after EP3 access 0: Disable	0, RW
0	AUTOLOAD	1: Auto-load the contents of 93c46 into RTL8150L(M)'s registers. This bit is self clearing after load complete.	0, RW

7.2. Transmit Configuration Register (Offset 012Fh, RW)

Table 45. Transmit Configuration Register (Offset 012Fh, RW)

Bit	Symbol	Description	Default/ Attribute
7-6	TXRR1, 0	Tx Retry Count: These 2 bits are used to specify additional transmission retries in multiple of 16(IEEE 802.3 CSMA/CD retry count). If the TXRR is set to 0, the transmitter will re-transmit 16 times before aborting due to excessive collisions. If the TXRR is set to a value greater than 0, the transmitter will re-transmit a number of times equal to the following formula before aborting: Total retries = 16 + (TXRR * 16) The ECOL bit in the TSR register will be set if transmit abort due to excessive collisions.	0, RW
5	Reserved	Reserved	-

Bit	Symbol	Description	Default/ Attribute
4,3	IFG1, 0	InterFrame Gap Time: This field allows the user to adjust the InterFrame Gap Time below the standard: 9.6µs for 10Mbps, 960ns for 100Mbps. The time can be programmed from 9.6µs to .8.4µs (10Mbps) and 960ns to 840ns (100Mbps). The formula for the inter frame gap is: 10Mbps 8.4us + 0.4(IFG(1:0))µs 100Mbps 840ns + 40(IFG(1:0)) ns	0, RW
2, 1	Reserved	Reserved	-
0	NOCRC	1: No CRC appended at the end of a packet 0: CRC appended at the end of a packet	0, RW

7.3. Receive Configuration Register (Offset 0130h-0131h, RW)

Table 46. Receive Configuration Register (Offset 0130h-0131h, RW)

Bit	Symbol	Description	Default/ Attribute
15-8	Reserved	Reserved	-
7	TAIL	0: CRC field forward to HOST 1: Rx Header forward to HOST. The first two bytes of CRC field are replaced by receive header	0, RW
6	AER	1: Accept CRC error packet	0, RW
5	AR	1: Accept RUNT packet (<64 bytes)	0, RW
4	AM	1: Accept all multicast packets enumerated in the driver's multicast address list 0: Disabled	0, RW
3	AB	1: Accept broadcast packets 0: Reject broadcast packets	0, RW
2	AD	1: Packets received containing a destination address that match the MAC address of the networking device are accepted 0: Disabled	0, RW
1	AAM	1: Accept all multicast frames received by the networking device, including the ones enumerated in the device's multicast address list 0: Disable	0, RW
0	AAP	1: Accept all physical frames 0: Disable	0, RW

7.4. Transmit Status Register (Offset 0132h)

Table 47. Transmit Status Register (Offset 0132h)

Bit	Symbol	Description	Default/ Attribute
7-6	Reserved	Reserved	-
5	ECOL	1: Excessive collision indication	R

Bit	Symbol	Description	Default/ Attribute
4	LCOL	1: Late collision indication	R
3	LOSS_CRS	1: Loss of carrier indication	R
2	JBR	1: Jabber time out indication	R
1	TX_BUF_EMPTY	1: Tx buffer empty indication	R
0	TX_BUF_FULL	1: Tx buffer full indication	R

Note: TSR register will be cleared to the default value after read or EP3 access.

7.5. Receive Status Register (Offset 0133h)

Table 48. Receive Status Register (Offset 0133h)

Bit	Symbol	Description	Default/ Attribute
7	WEVENT	Wake Up Event Indication 1: Wakeup event occurs	R
6	RX_BUF_FULL	Rx Buffer Full Indication	R
5	LKCHG	Link Change Indication	R
4	RUNT	Runt Packet Indication 1: The received packet length is smaller than 64 bytes	R
3	LONG	Long Packet Indication 1: The size of the received packet exceeds 4k bytes	R
2	CRC	CRC Error Indication 1: The received packet is checked with CRC error	R
1	FAE	Frame Alignment Error 1: Indicates that a frame alignment error occurred on this received packet	R
0	ROK	Receive OK Indication 1: Indicates that a packet was received without error	R

Note: RSR register will be cleared to the default value after read or EP3 access.

7.6. Configuration Register 0 (Offset 0135h, RW)

Table 49. Configuration Register 0 (Offset 0135h, RW)

Bit	Symbol	Description	Default/ Attribute
7	SUSLED	0: LED pins are driven high to turn off LED during suspend	0, RW
6	PARM_EN	Parameter Enable (These Parameters are Used in 100Mbps Mode) 1: PHY1_PARM, PHY2_PARM, TW_PARM can be modified through access to register 0180H~0189H 0: Disable *Note: Each time 93C46 auto-load process is executed, the PHY1_PARM, PHY2_PARM, TW_PARM will be re-loaded the default value from 93C46.*	0, RW
4-5	Reserved	Reserved	-
3	LDPS	Link Down Power Saving Mode 1: Disable 0: Enable. When the Ethernet cable is disconnected (Link Down), part of the analog circuit will be powered down in order to save power. The part of the analog circuit related to SD signal monitoring and 100M signal receiving are not powered down in case the cable is re-connected and link needs to be re-established again	0, RW
2	MSEL	Medium Select When written: 1: MII mode (disable internal PHY) 0: Auto-detect The UTP mode will be the default. The RTL8150L(M) is switched to MII mode if the internal PHY is not link OK When read: 1: MII mode The MAC MII is connected to the MII interface of the external PHY. 0: UTP mode The MAC MII is connected to the internal PHY.	0, RW
1-0	LEDS1-0	Refer to LED PIN Definition The default value is auto-loaded from 93C46.	0, RW

7.7. Configuration Register 1 (Offset 0136h, RW)

Table 50. Configuration Register 1 (Offset 0136h, RW)

Bit	Symbol	Description	Default/ Attribute
7	Reserved	Reserved	-
6	BWF	Broadcast Wakeup Frame 1: Enable Broadcast Wakeup Frame If set_feature command with Feature Selector =DEVICE_REMOTE_WAKEUP is received from the USB host, and BWF=1, the RTL8150L(M) will signal wakeup to the host when correctly receiving a packet with DID=FF FF FF FF FF FF (Broadcast packet) 0: Disable	0, RW
5	MWF	Multicast Wakeup Frame 1: Enable Multicast Wakeup Frame If set_feature command with Feature Selector =DEVICE_REMOTE_WAKEUP is received from the USB host, and MWF=1, the RTL8150L(M) will signal wakeup to the host when correctly receiving multicast packets (packets that survive the multicast hash) 0: Disable	0, RW
4	UWF	Unicast Wakeup Frame 1: Enable Unicast Wakeup Frame f set_feature command with Feature Selector =DEVICE_REMOTE_WAKEUP is received from the USB host, and UWF=1, the RTL8150L(M) will signal wakeup to the host when correctly receiving a packet with DID=IDR0~5 0: Disable	0, RW
2-3	Reserved	Reserved	-
1	LONGWF1	1: The Bytemask3 and Bytemask4 are cascaded to form a 128-byte long Bytemask for long wakeup frame 1, and long wakeup frame 1 use CRC3 as CRC check. When LONGWF1=1, wakeup frame 3 and wakeup frame 4 are disabled 0: Disable LOGNWF1	0, RW
0	LONGWF0	1: The Bytemask1 and Bytemask2 are cascaded to form a 128 byte long Bytemask for long wakeup frame 0, and long wakeup frame 0 use CRC1 as CRC check. When LONGWF0=1, wakeup frame 1 and wakeup frame 2 are disabled 0: Disable LOGNWF0	0, RW

7.8. Media Status Register (Offset 0137h, RW)

Table 51. Media Status Register (Offset 0137h, RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Default/ Attribute</th></tr>
<tr><td>7</td><td>TXFCE/
LdTXFCE</td><td>Tx Flow Control Enable. The flow control is valid in full-duplex mode only. This register’s default value comes from the 93C46.
<table>
<tr><th>RTL8150L</th><th>Remote</th><th>TXFCE/LdTXFCE</th></tr>
<tr><td>ANE = 1</td><td>NWay FLY mode</td><td>R/O</td></tr>
<tr><td>ANE = 1</td><td>NWay mode only</td><td>RW</td></tr>
<tr><td>ANE = 1</td><td>No NWay</td><td>RW</td></tr>
<tr><td>ANE = 0 &
full-duplex mode</td><td>-</td><td>RW</td></tr>
<tr><td>ANE = 0 &
half-duplex mode</td><td>-</td><td>Invalid</td></tr>
</table>
NWay FLY mode: NWay with flow control capability
NWay mode only: NWay without flow control capability</td><td>RW</td></tr>
<tr><td>6</td><td>RXFCE</td><td>RX Flow Control Enable. Flow control is enabled in full-duplex mode only. The default value comes from the 93C46.</td><td>RW</td></tr>
<tr><td>5</td><td>Reserved</td><td>Reserved</td><td>-</td></tr>
<tr><td>4</td><td>Duplex</td><td>1: Indicates that the current link is full-duplex
0: Indicates that the current link is half-duplex</td><td>R</td></tr>
<tr><td>3</td><td>SPEED_100</td><td>1: Indicates that the current link is in 100Mbps mode
0: Indicates that the current link is in 10Mbps mode</td><td>R</td></tr>
<tr><td>2</td><td>LINK</td><td>Link Status
1: Link OK
0: Link Fail</td><td>R</td></tr>
<tr><td>1</td><td>TXPF</td><td>1: Indicates that the RTL8150L(M) is sending pause packets
0: Indicates that the RTL8150L(M) has sent timer done packets to release the remote station from pause Tx state</td><td>R</td></tr>
<tr><td>0</td><td>RXPF</td><td>1: Indicates that the RTL8150L(M) is in Backoff state because a pause packet from remote station has been receipt
0: Indicates that the RTL8150L(M) is not in pause state</td><td>R</td></tr>
</table>

7.9. MII PHY Address (Offset 0138h, RW)

Table 52. MII PHY Address (Offset 0138h, RW)

Bit	Symbol	Description	Default/ Attribute
7-5	Reserved	Reserved	-
4-0	PHYADD	MII PHY Address Select	RW

7.10. MII PHY DATA (Offset 0139h-013Ah, RW)

Table 53. MII PHY DATA (Offset 0139h-013Ah, RW)

Bit	Symbol	Description	Default/ Attribute
15-0	MIIDAT	Data Read from MII PHY or Data that is to be Written to MII PHY	RW

7.11. MII PHY Access Control (Offset 013Bh, RW)

Table 54. MII PHY Access Control (Offset 013Bh, RW)

Bit	Symbol	Description	Default/ Attribute
7	Reserved	Reserved	-
6	PHYOWN	Own Bit: RTL8150L(M) will initiate a MII management data transaction if this bit is set 1 by software. After transaction, this bit is auto cleared by the RTL8150L.	0, RW
5	RWCR	MII Management Data RW Control 1: Write 0: Read	RW
4-0	PHYOFF	PHY Register Offset	RW

7.12. General Purpose Register (Offset 013Dh, RW)

Table 55. General Purpose Register (Offset 013Dh, RW)

Bit	Symbol	Description/Usage	Default/ Attribute
7-5	GEPREG1~3	Reserved	-
4	GEPREG0	General Purpose Bit 1: Supports external Home PNA PHY	RO
3	GEP1DAT	If GEP1RW is set to 1, the GEP1 pin will reflect the value of GEP1DAT, else GEP1DAT will reflect the value of the GEP1 pin.	RW
2	GEP1RW	General Purpose Pin Control Bit 0: The corresponding GEP1 pin is considered input 1: The corresponding GEP1 pin is considered output	RW
1	GEP0DAT	If GEP0RW is set to 1, the GEP0 pin will reflect the value of GEP0DAT, else GEP0DAT will reflect the value of the GEP0 pin.	RW
0	GEP0RW	General Purpose Pin Control Bit 0: The corresponding GEP0 pin is considered input 1: The corresponding GEP0 pin is considered output	RW

If GEPRW=0=READ only

7.13. Wake Up Event Control (Offset 013E, RW)

Table 56. Wake Up Event Control (Offset 013E, RW)

Bit	Symbol	Description/Usage	Default/ Attribute
7	Reserved	Reserved	-
6	LKWEN	Link Change Wake-Up Enable	0, RW
5	MAGWEN	Magic Packet Wake-Up Enable	0, RW
4	WUF4EN	Wakeup Frame 4 Enable	0, RW
3	WUF3EN	Wakeup Frame 3 Enable	0, RW
2	WUF2EN	Wakeup Frame 2 Enable	0, RW
1	WUF1EN	Wakeup Frame 1 Enable	0, RW
0	WUF0EN	Wakeup Frame 0 Enable	0, RW

Note: The RTL8150L(M) will signal wakeup to the host only when the following two conditions are met:

1. The host has sent a set_feature_device command.

2. One of the wakeup frame functions has been enabled and triggered.

7.14. Basic Mode Control Register (Offset 0140h-0141h, RW)

Table 57. Basic Mode Control Register (Offset 0140h-0141h, RW)

Bit	Name	Description/Usage	Default/ Attribute
15	Reset	This bit, which is self-clearing, will reset the control and status registers of PHY into the default states if it is set 1.	0, RW
14	Reserved	Reserved	-
13	Spd_Set	Speed Select 1: 100Mbps 0: 10Mbps *Note: The initial value of this bit comes from 93C46.*	RW
12	Auto Negotiation Enable (ANE)	This Bit Enables/Disables the NWay Auto-Negotiation Function 1: Enable auto-negotiation. If this bit is set, bit 8 and bit13 will be ignored, and the values of bit8 and bit 13 indicate the result of auto negotiation process 0: Disable auto-negotiation *Note: The initial value of this bit comes from 93C46.*	0, RW
11-10	Reserved	Reserved	-
9	Restart Auto Negotiation	This Bit Allows the NWay Auto-Negotiation Function to be Re-Initiated 1: Re-start auto-negotiation 0: Normal operation.	0, RW
8	Duplex Mode	This Bit Sets the Duplex Mode 1: Full-duplex 0: Normal operation *Note: This bit's initial value comes from the 93C46.*	0, RW
7-0	Reserved	Reserved	-

7.15. Basic Mode Status Register (Offset 0142h-0143h, R)

Table 58. Basic Mode Status Register (Offset 0142h-0143h, R)

Bit	Name	Description/Usage	Default/ Attribute
15	100Base-T4	100Base-T4 Capable 0: Device not able to perform in 100Base-T4 mode	0, RO
14	100Base_TX_FD	100Base-TX Full Duplex Capable 1: Device able to perform 100Base-TX in full duplex mode	1, RO
13	100Base_TX_HD	100Base-TX Half Duplex Capable 1: Device able to perform 100Base-TX in half duplex mode	1, RO
12	10Base_T_FD	10Base-T Full Duplex Capable 1: Device able to perform 10Base-T in full duplex mode	1, RO
11	10_Base_T_HD	10Base-T Half Duplex Capable 1: Device able to perform 10Base-T in half duplex mode	1, RO
10~6	Reserved	Reserved	-
5	Auto Negotiation Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0, RO
4	Remote Fault	1: Remote fault condition detected (clear on read) 0: No remote fault condition detected	0, RO
3	Auto Negotiation ability	1: Device is able to perform Auto-Negotiation 0: Device not able to perform Auto-Negotiation	1, RO
2-1	Reserved	Reserved	
0	Extended Capability	1: Extended register capabilities 0: Basic register set capabilities	1, RO

7.16. Auto-negotiation Advertisement Register (Offset 0144h-0145h, RW)

Table 59. Auto-negotiation Advertisement Register (Offset 0144h-0145h, RW)

Bit	Name	Description/Usage	Default/ Attribute
15	NP	Next Page Capability 0: Advertise that NP capability not supported by local mode 1: Advertise NP exchange capability and desire to transfer next page	0, RO
14	ACK	1: Acknowledge reception of link partner's capability data word	0, RO
13	RF	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	0, RW
12-11	Reserved	Reserved	-
10	PAUSE	1: Advertise flow control supported by local node 0: Advertise flow control not supported by local mode	The default value comes from EEPROM, RO
9	T4	1: Advertise 100Base-T4 supported by local node 0: Advertise 100Base-T4 not supported by local node	0, RO

Bit	Name	Description/Usage	Default/ Attribute
8	TXFD	1: Advertise 100Base-TX full duplex supported by local node 0: Advertise 100Base-TX full duplex not supported by local node	1, RW
7	TX	1: Advertise 100Base-TX supported by local node 0: Advertise 100Base-TX not supported by local node	1, RW
6	10FD	1: Advertise 10Base-T full duplex supported by local node 0: Advertise 10Base-T full duplex not supported by local node	1, RW
5	10	1: Advertise 10Base-T supported by local node 0: Advertise 10Base-T not supported by local node	1, RW
4-0	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD <00001> is specified. No other protocols are supported.	<00001>, RW

7.17. Auto-Negotiation Link Partner Ability Register (Offset 0146h-0147h, R)

Table 60. Auto-Negotiation Link Partner Ability Register (Offset 0146h-0147h, R)

Bit	Name	Description/Usage	Default/ Attribute
15	NP	Next Page Indication 0: Link Partner does not desire Next Page Transfer 1: Link Partner desires Next Page Transfer	0, RO
14	ACK	1: link partner acknowledges reception of the capability data word 0: Not acknowledged The device's Auto-Negotiation state machine will automatically control this bit based on the incoming FLP bursts.	0, RO
13	RF	Remote Fault 1: Remote Fault indicated by Link Partner 0: No Remote Fault indicated by Link Partner	0, RO
12-11	Reserved	Reserved	-
10	Pause	1: Flow control is supported by link partner 0: Flow control is not supported by link partner	0, RO
9	T4	100Base-T4 Support 1: 100Base-T4 is supported by the link partner 0: 100Base-T4 not supported by the link partner	0, RO
8	TXFD	100Base-TX Full Duplex Support 1: 100Base-TX full duplex is supported by the link partner 0: 100Base-TX full duplex not supported by the link partner	0, RO
7	TX	100Base-TX Support 1: 100Base-TX is supported by the link partner 0: 100Base-TX not supported by the link partner	0, RO
6	10FD	10Base-T Full Duplex Support 1: 10Base-T full duplex is supported by the link partner 0: 10Base-T full duplex not supported by the link partner	0, RO

Bit	Name	Description/Usage	Default/ Attribute
5	10	10Base-T Support 1: 10Base-T is supported by the link partner 0: 10Base-T not supported by the link partner	0, RO
4-0	Selector	Protocol Selection Bits Link Partner's binary encoded protocol selector.	0, RO

7.18. Auto-Negotiation Expansion Register (Offset 0148h-0149h, R)

This register contains additional status for NWay auto-negotiation.

Table 61. Auto-Negotiation Expansion Register (Offset 0148h-0149h, R)

Bit	Name	Description/Usage	Default/ Attribute
15-5	Reserved	Reserved. This bit is always set to 0.	-
4	MLF	Status Indicating whether a Multiple Link Fault Has Occurred 1: Fault occurred 0: No fault occurred	0, RO
3	LP_NP_ABLE	Status Indicating whether the Link Partner Supports Next Page Negotiation 1: Supported 0: Not supported	0, RO
2	NP_ABLE	This Bit Indicates whether the Local Node is Able to Send Additional Next Pages	0, RO
1	PAGE_RX	This Bit is Set when a New Link Code Word Page Has Been Received The bit is automatically cleared when the auto-negotiation link partner's ability register (register 146h) is read by management.	0, RO
0	LP_NW_ABLE	1: Link partner supports NWay auto-negotiation	0, RO

7.19. NWay Test Register (Offset 014Ah-014Bh, RW)

Table 62. NWay Test Register (Offset 014Ah-014Bh, RW)

Bit	Name	Description/Usage	Default/ Attribute
15-8	Reserved	Reserved	-
7	NWLPBK	1: Set NWay to loopback mode	0, RW
6-4	Reserved	Reserved	-
3	ENNWLE	1: LED0 Pin indicates link pulse	0, RW
2	FLAGABD	1: Auto-negotiation experienced ability detect state	0, RO
1	FLAGPDF	1: Auto-negotiation experienced parallel detection fault state	0, RO
0	FLAGLSC	1: Auto-negotiation experienced link status check state	0, RO

7.20. CS Configuration Register (Offset 014Ch-014Dh, RW)

Table 63. CS Configuration Register (Offset 014Ch-014Dh, RW)

Bit	Name	Description/Usage	Default/ Attribute
15	Testfun	1: Speeds up internal timer for Auto-Negotiation	0,WO
14-10	Reserved	Reserved	-
9	LD	Active Low TPI Link Disable Signal When low, TPI still transmits link pulses and TPI stays in good link state.	1, RW
8	HEART BEAT	1: Heartbeat Enable 0: Heartbeat Disable Heartbeat function is only valid in 10Mbps mode	1, RW
7	JBEN	1: Enable jabber function 0: Disable jabber function	1, RW
6	F_LINK_100	Force Link-Up in 100Mbps for Diagnostic Purposes 1: Disable 0: Enable	1, RW
5	F_Connect	Force Connection of the Link for Diagnostic Purposes 1: Fore connection 0: Disable	0, RW
4	Reserved	Reserved	-
3	Con_status	This Bit Indicates the Status of the Connection 1: Valid connected link detected 0: Disconnected link detected.	0, RO
2	Con_status_En	Assertion of This Bit Configures LED1 Pin to Indicate Connection Status	0, RW
1	Reserved	Reserved	-
0	PASS_SCR	Bypass Scramble Function	0, RW

8. EEPROM 93C46 Contents

The 93C46 is a 1K-bit EEPROM. Although it is actually addressed by words, we list its contents by bytes below for convenience.

After the valid duration of the RSTB pin or auto-load command in Command Register (offset 012Eh), the RTL8150L(M) performs a series of EEPROM read operation from the 93C46.

Note: We recommend that you have Realtek approval before making changes to the Realtek EEPROM content default settings.

Table 64. EEPROM 93C46 Contents

Bytes	Contents	Description
00h	50h	These 2 Bytes Contain ID Code Words for the RTL8150L(M)
01h	81h	The RTL8150L(M) will load the contents of EEPROM into the corresponding location if the ID word (8150h) is correct.
02h-07h	Ethernet ID	Ethernet ID. After an auto-load command or hardware reset, the RTL8150L(M) loads the Ethernet ID to IDR0-IDR5 of the RTL8150L(M).
08h	CONFIG0	RTL8150L(M) Configuration Register 0, Operational Registers Offset 0135h
09h	MSR/BMCR	Bit7-6 Map to Bit7-6 of the Media Status Register (MSR) Bit5, 4, and 0 map to bit13, 12, and 8 of the Basic Mode Control register (BMCR). Bit2 maps to bit10 of the Auto-negotiation Advertisement Register (ANAR). Bit3 and 1 are reserved. If the network speed is set to Auto-Detect mode (i.e. NWay mode), then Bit2=0 means the local RTL8150L(M) supports flow control (IEEE 802.3x) (in this case, Bit10=1 in Auto-negotiation Advertisement Register (offset 146h-147h), and Bit2=1 means the local RTL8150L(M) does not support flow control (in this case, Bit10=0 in Auto-negotiation Advertisement). This is because there are some NWay switches that, if the link partner supports NWay flow control, will keep sending flow control pause packets for no reason.
0Ah	GEP	General Purpose Pin Control Register (Offset 013Dh)
0Bh	UDP	Reserved. Do not change this field without Realtek approval. USB Device Parameter.
0Ch	ATTR	USB Configuration Characteristics Bit7 is reserved and must be set to one for USB spec. A device configuration that uses power from the bus and a local source reports a non-zero value in MaxPower to indicate the amount of bus power required and sets Bit 6. Bit5 is set one to support remote wakeup. Bit4-0: Reserved and must be reset to zero for USB spec.
0Dh	PHY2_PARM	Reserved. Do not change this field without Realtek approval. PHY Parameter 2 for RTL8150L(M). The Operational register of the RTL8150L(M) is 0184h.
0Eh-11h	PHY1_PARM	Reserved. Do not change this field without Realtek approval. PHY Parameter 1 for RTL8150L(M). The Operational register of the RTL8150L(M) is 0180h-0183h.

Bytes	Contents	Description
12h-15h	TW1_PARM	Reserved. Do not change this field without Realtek approval. Twister Parameter for RTL8150L(M). The Operational registers of the RTL8150L(M) are 0186h-0189h.
16h	MAXPOR	The Maximum USB Power Consumption
17h	INTERVAL	Interval for Polling Endpoint 3 for Data Transfers. Expressed in milliseconds.
18h-19h	LanguageID	The String in a USB Device May Support Multiple Languages A manufacturer can specify the desired language using a sixteen-bit language ID.
1Ah-1Bh	ManufacturerID	The System Manufacturer's ID
1Ch-1Dh	ProductID	The System Manufacturer's Product ID
1Eh-27h	Serial number	The Product's Serial Number
28h-4fh	Manufacturer String	These Bytes Specify a Manufacturer's Information for the USB Standard Request Maximum string length is 40 bytes.
50h-7dh	Product String	These Bytes Specify a Device's Information for the USB Standard Request Maximum string length is 46 bytes.
7eh-7fh	Reserved	Reserved

8.1. Summary of the RTL8150L's Registers in the EEPROM (93C46)

Table 65. Summary of the RTL8150L's Registers in the EEPROM (93C46)

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	ROMID0	R	0	1	0	1	0	0	0	0
01h	ROMID1	R	1	0	0	0	0	0	0	1
02-07h	IDR0-IDR5	RW								
08h	Config0	RW	SUSLED	PARM_EN	-	-	LDPS	MSEL	LEDS1	LEDS0
09h	MSR/BMCR	RW	TXFCE	RXFCE	Spd_set	ANE	-	PAUSE	-	FUDUP
0Ah	GPCP	RW	GEPREG3	GEPREG2	GEPREG1	GEPREG0	GEP1DAT	GEP1RW	GEP0DAT	GEP0RW
0Bh	UDP	RW	8 Bit Read Write							
0Ch	ATTR	RW	1	0	1	0	0	0	0	0
0Dh	PHY2_PARM	RW	8 Bits Read Write							
0E-11h	PHY1_PARM	RW	32 Bits Read Write							
12h-15h	TW1_PARM	RW	32 Bits Read Write							
16h	MAXPOR	RW	8 Bits Read Write							
17h	Interval	RW	0	0	0	0	0	0	0	1
18h-19h	Language ID	RW	16 Bits Read Write							
1Ah-1Bh	Manufacture ID	RW	16 Bits Read Write							
1Ch-1Dh	Product ID	RW	16 Bits Read Write							
1Eh-27h	Serial Number	RW	10 Bytes Read Write							
28h-4fh	Manufacture String	RW	40 Bytes Read Write							
50h-7dh	Product String	RW	46 Bytes Read Write							
7eh-7fh	Reserved	-	Reserved							

9. Functional Description

9.1. System Block Diagram

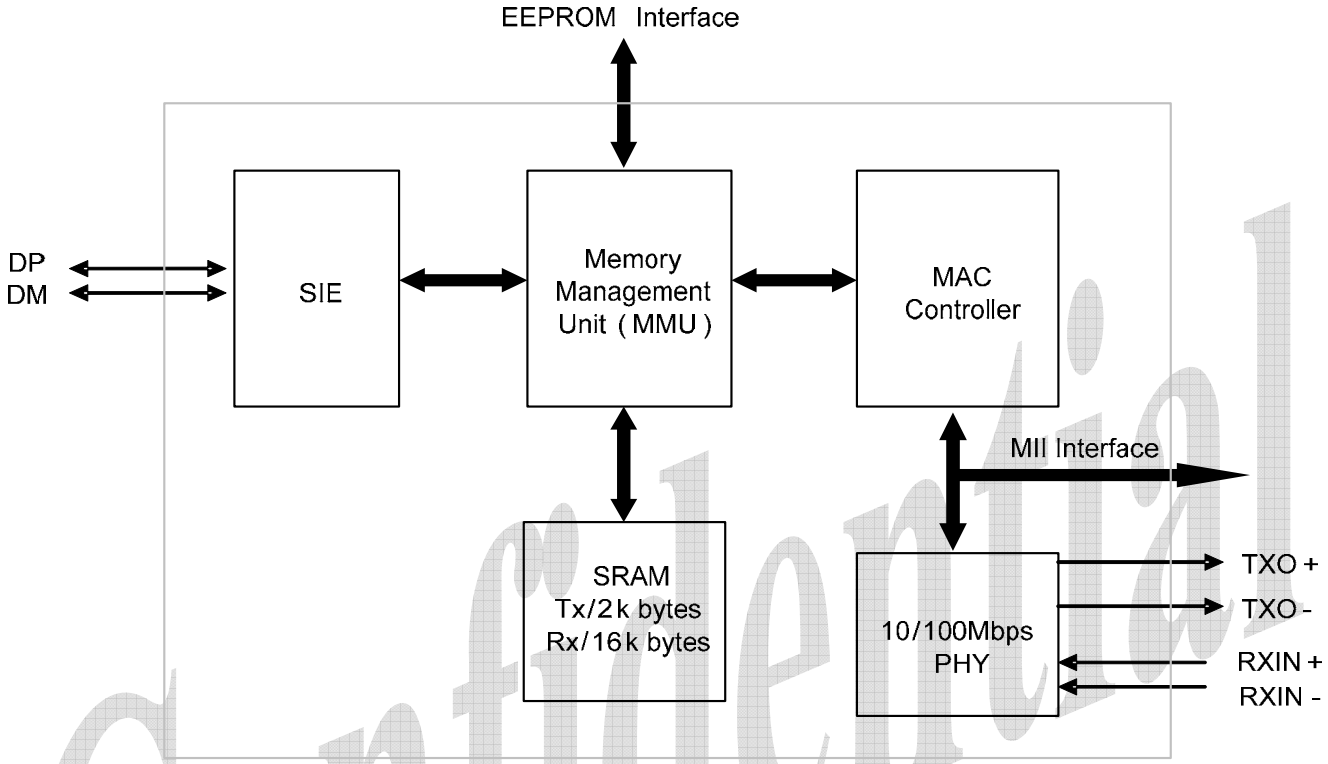


Figure 3. System Block Diagram

9.2. USB Endpoint SIE Function Description

The SIE (Serial Interface Engine) employs a robust hardwired USB protocol implementation so that the entire USB interface operation can be completed without firmware intervention. For all three types of endpoint (bulk in, bulk out, and interrupt), appropriate responses and handshake signals are generated by the SIE. The SIE analog transceiver complies fully with driver and receiver characteristics defined in USB Spec. Rev. 1.1.

9.2.1. Endpoint0

All USB devices support a common access mechanism for accessing information through this control pipe. Associated with the control pipe at endpoint zero is the information required to completely describe the USB device. This pipe also provides the register read and write to the RTL8150L.

9.2.2. Endpoint 1 Bulk IN

The maximum Bulk IN packet size is 64 bytes. Each Ethernet packet is transferred to the Host by this Endpoint. If the Ethernet packet is larger than 64 bytes, the RTL8150L(M) splits the Ethernet packet into multiples of 64 bytes. The Host treats USB packets that are less than 64 bytes or that equal zero as End of Ethernet packets.

9.2.3. Endpoint 2 Bulk OUT

The Host sends the USB packet to Ethernet with a maximum Bulk OUT packet size of 64 bytes. If the Ethernet packet is larger than 64 bytes, the Host will send this Ethernet packet in USB packets with multiples of 64 bytes. A USB packet less than 64 bytes (including zero byte) indicates the end of a Ethernet packet.

The Ethernet packet (containing multiple USB packets) will be queued in TX FIFO and transmitted later when possible. If the Ethernet packet is transmitted to medium without error, the TX FIFO space which was occupied by the transmitted Ethernet packet will be released again. If the 2Kbyte TX FIFO is full, the RTL8150L(M) will respond with a NAK when the host is trying to bulk out more USB packets. It is possible to have multiple Ethernet packets in the TX FIFO simultaneously. If an Ethernet packet is to be transmitted, but experiences collisions more than 16 times (default), this is called a transmit abort and this packet will be skipped for transmission by the RTL8150L(M).

9.2.4. Endpoint 3 Interrupt IN

The Interrupt Endpoint (EP3) can be used to poll the current status of the RTL8150L(M). The 8 bytes of EP3 contain the information listed below. After EP3 access, the information will be cleared and the counter will be reset if EP3CLREN (Reg 012Eh) is set. The NUMTXOK, RXLOST, CRCERR, COLCNT counters will saturate to 255 if the number of up-count events is greater than 255.

The eight bytes of EP3 Interrupt IN contains:

DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7
TSR	RSR	GEP/MSR	WAKSR	NUMTXOK	RXLOST	CRCERR	COLCNT

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	TSR	R	-	-	ECOL	LCOL	LOSS_CRS	JBR	TX_BUF_EMPTY	TX_BUF_FULL
01h	RSR	R	-	RX_BUF_FULL	LKCHG	RUNT	LONG	CRC	FAE	ROK
02h	GEP/MSR	R	GEP1DAT	GEP0DAT	-	Duplex	SPEED_100	LINK	TXPF	RXPF
03h	WAKSR	R	-	PARM_EN	-	-	WAKEUP_EV	LKWAKE_EV	MAGIC_EV	BMU_EV
04	TXOK_CNT	R	8-bit counter that counts valid packets transmitted.							
05h	RXLOST_CNT	R	8-bit counter that counts packets lost due to Rx buffer overflow.							
06h	CRCERR_CNT	R	8-bit counter that counts error packets.							
07h	COL_CNT	R	8-bit counter that counts collisions.							

9.3. Ethernet Function Description

9.3.1. Transmit Operation

The USB host initiates a transmission by transferring multiple USB packets into the Tx buffer. When the MAC receives USB BULK OUT packets from the USB host, the RTL8150L(M) starts Ethernet packet transmission.

9.3.2. Receive Operation

Incoming Ethernet packets are queued in the RTL8150L(M)'s Rx buffer. While the RTL8150L(M) is receiving the Ethernet packets, it also performs address filtering of multicast packets according to its hash algorithms. When the Ethernet packet is correctly received or the amount of data in the Rx buffer reaches the level defined in the Receive Configuration Register (Early receive function is on), the RTL8150L(M) requests the USB SIE to begin transferring the data to the USB Host memory.

Rx header format (ref. Receive Configuration Register, offset 0130h)

Bit 11-0: Rx bytes count

Bit 12: Valid packet (Packet that is RXOK and not accept error)

Bit 13: Runt packet

Bit 14: Physical match packet

Bit 15: Multicast packet

9.4. Collision

If the RTL8150L(M) is not set to full-duplex mode, a collision event occurs when the receive input is not idle while the RTL8150L(M) transmits. If the collision is detected during the preamble transmission, the jam pattern is transmitted after completing the preamble transmission (including the JK symbol pair).

9.5. Flow Control

The RTL8150L(M) supports IEEE802.3X flow control to improve performance in full-duplex mode. It recognizes PAUSE packets sent from remote stations, and also backoff transmissions according to IEEE802.3X (if RXFCE is set), or the RTL8150L(M) sends PAUSE packets to remote station when the local RX FIFO exceeds some threshold if the TXFCE is set.

9.6. Control Frame Transmission

When the free space of RX FIFO is less than 3K bytes. The RTL8150L(M) sends a PAUSE packet with pause_time(=FFFFh) to request the remote station stop transmission for the specified period of time. After the packets in the RX FIFO are consumed and free space in the RX FIFO is greater than 5K bytes, the RTL8150L(M) sends a PAUSE packet with pause_time(=0000h) to request the remote station to restart transmission.

9.7. Control Frame Reception

The RTL8150L(M) backoffs transmission for the specified period of time when it receives a valid PAUSE packet with pause_time(=n). If the PAUSE packet is received while the RTL8150L(M) is transmitting, the RTL8150L(M) will start to backoff after the current transmission completes. The RTL8150L(M) is free to transmit packets again if a valid PAUSE packet with pause_time(=0000h) is received or the backoff timer(=n*512 bit time) elapses.

Note: The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. PAUSE packets). The NWay flow control capability can be disabled (Refer to section 8 EEPROM 93C46 Contents, page 32 for a detailed description).

10. ELECTRICAL CHARACTERISTICS

10.1. Temperature Limit Ratings

Table 66. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C

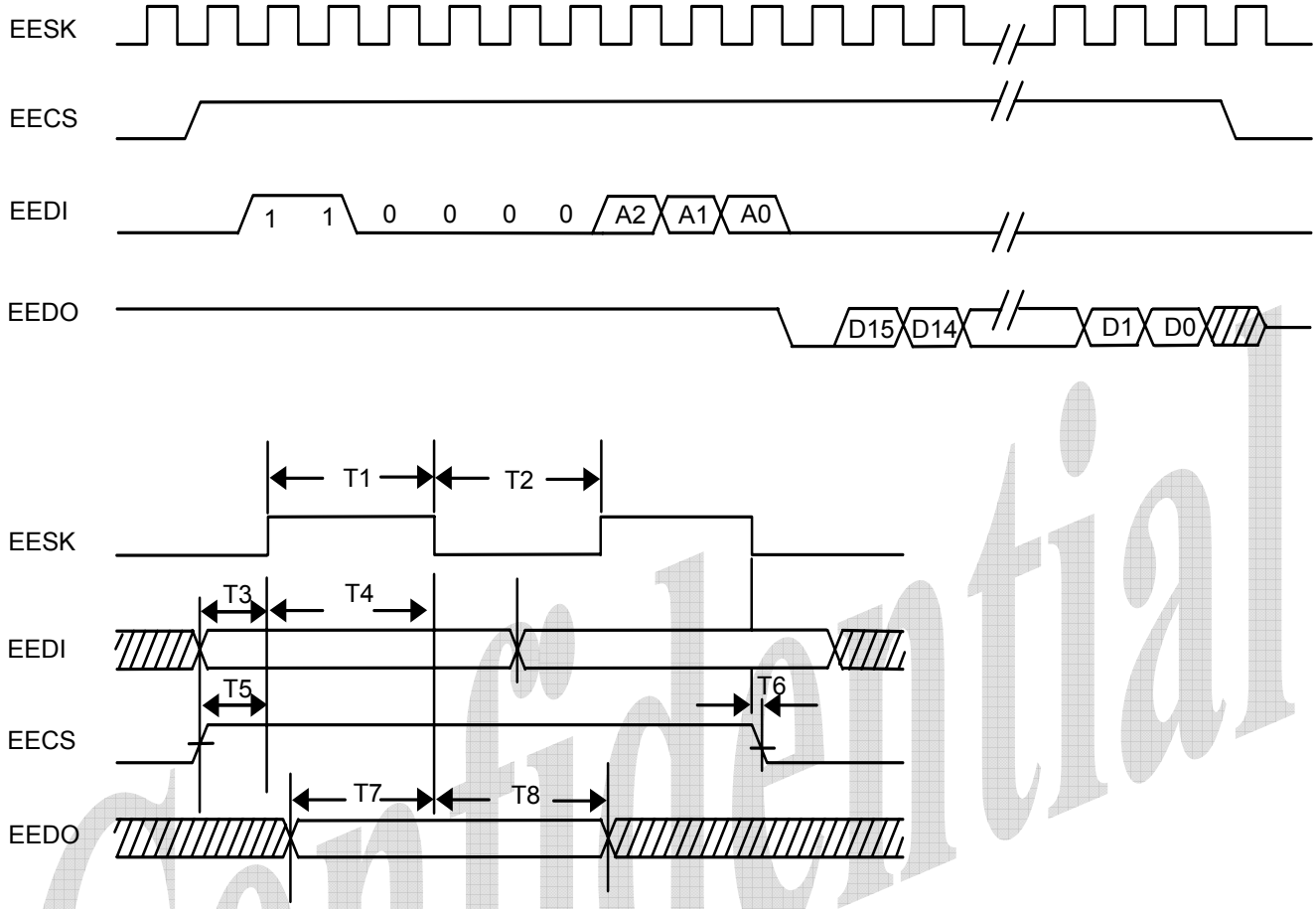
10.2. DC Characteristics

Supply Voltage (Bus Power) Vbus=4.5V min. to 5.5V max. Vcc=3.3V

Table 67. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH}=-2mA	0.9*Vcc	Vcc	V
V_{OL}	Maximum Low Level Output Voltage	I_{OL}=8mA	-	0.1*Vcc	V
V_{IH}	Minimum High Level Input Voltage	-	0.5*Vcc	Vcc+0.5	V
V_{IL}	Maximum Low Level Input Voltage	-	-0.5	0.3*Vcc	V
I_{IN}	Input Current	V_{IN}=V_{CC} or GND	50	50	µA
I_{OZ}	Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND	50	50	µA
I_{CC}	Average Operating Supply Current	I_{OUT}=0mA	-	110	mA

10.3. EEPROM Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EESK High Width	-	3.2	-	µs
T2	EESK Low Width	-	3.2	-	µs
T3	EEDI Setup to EESK Rising Edge	3.0	-	-	µs
T4	EEDI Hold from EESK Rising Edge	3.0	-	-	µs
T5	EECS Goes High to EESK Rising Edge	3.0		-	µs
T6	EECS Goes Low from EESK Falling Edge	-	0	-	ns
T7	EEDO Setup to EESK Falling Edge	20	-	-	ns
T8	EEDO Hold from EESK Falling Edge	10	-	-	ns

10.4. GPIO Interface

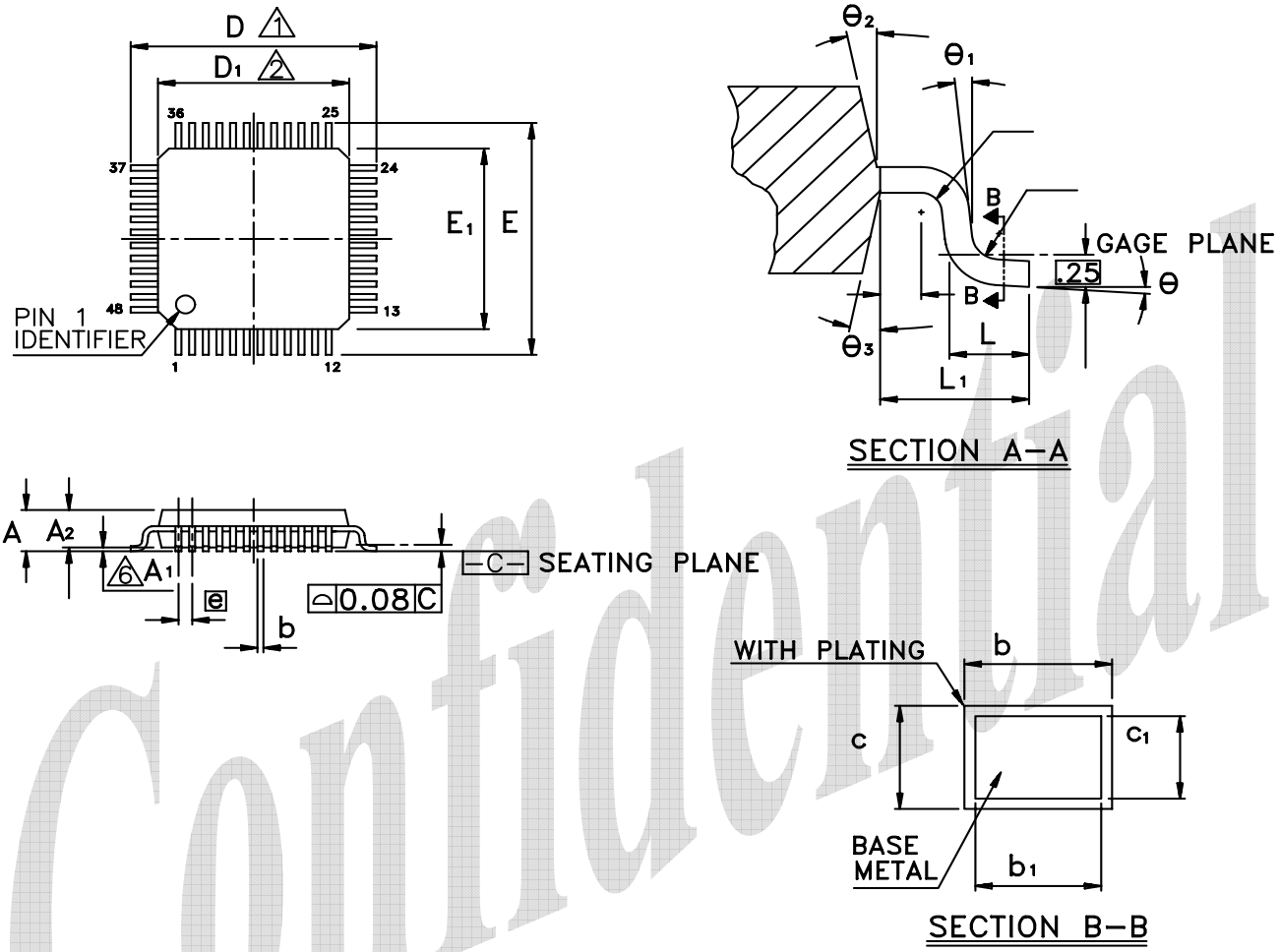
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ih}	Input High Voltage	2.0	-	-	V
V_{il}	Input Low Voltage	-	-	0.8	V
V_{oh}	Output High Voltage	0.9Vcc	-	-	V
V_{ol}	Output Low Voltage	-	-	0.1Vcc	V
I_{ih}	Input High Leakage Current	-	-	50	µA
I_{il}	Input Low Leakage Current	-	-	-10	µA

10.5. USB Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{fr}	Rise Time	9.6	12	14.4	ns
T_{ff}	Fall Time	12.8	16	19.2	ns

11. Mechanical Dimensions

11.1. RTL8150L (48-Pin LQFP)



11.2. Mechanical Dimensions Notes (RTL8150L 48-Pin LQFP)

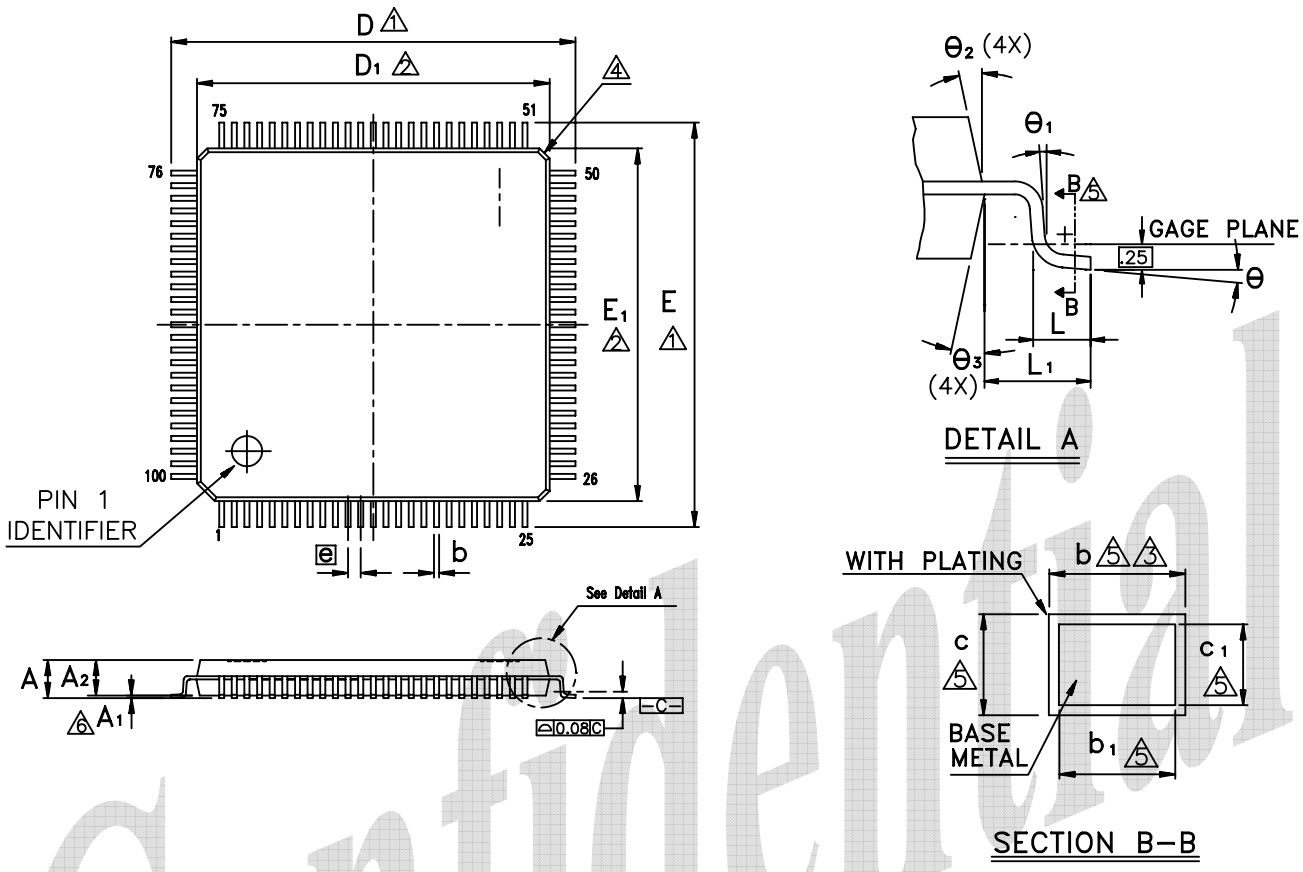
Symbol	Dimension in Inchs			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	0.1	0.20
A2	0.051	0.055	0.059	1.30	1.40	1.50
b	0.006	0.009	0.011	15	0.22	0.29
B1	0.006	0.008	0.010	0.15	0.20	0.25
c1	0.004	-	0.006	0.09	-	0.16
D	0.354 BSC			9.00 BSC		
D1	0.276 BSC			7.00 BSC		
E	0.354 BSC			9.00 BSC		
E1	0.276 BSC			7.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L1	0.039 REF			1.00 REF		
θ	0°	3.5°	9°	0°	3.5°	9°
θ1	0°	-	-	0°	-	-
θ2	12° TYP			12° TYP		
θ3	12° TYP			12° TYP		

Notes:

1. To be determined at seating plane – c-
2. Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference document: JEDEC MS-026, BBC

TITLE: 48LD LQFP (7x7x1.4mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL:		
APPROVE	DOC. NO.	
	VERSION	1
	PAGE	OF
CHECK	DWG NO.	SS048 – P1
	DATE	
REALTEK SEMICONDUCTOR CORP.		

11.3. RTL8150LM (100-Pin LQFP)



11.4. Mechanical Dimensions Notes (RTL8150LM 100-Pin LQFP)

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A_1	0.000	0.004	0.008	0.00	0.1	0.20
A_2	0.051	0.055	0.059	1.30	1.40	1.50
B	0.006	0.009	0.011	15	0.22	0.29
B_1	0.006	0.008	0.010	0.15	0.20	0.25
C	0.004	-	0.008	0.09	-	0.20
C_1	0.004	-	0.006	0.09	-	0.16
D	0.630 BSC			16.00 BSC		
D_1	0.551 BSC			14.00 BSC		
E	0.630 BSC			16.00 BSC		
E_1	0.551 BSC			14.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L_1	0.039 REF			1.00 REF		
θ	0°	3.5°	9°	0°	3.5°	9°
θ_1	0°	-	-	0°	-	-
θ_2	12°TYP			12°TYP		
θ_3	12°TYP			12°TYP		

Note:

1. To be determined at seating plane -c-
2. Dimensions D_1 and E_1 do not include mold protrusion. D_1 and E_1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A_1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference document: JEDEC MS-026, BED.

TITLE: 100LD LQFP (14x14x1.4mm)			
PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	LQ100-P1
		DATE	APR. 28. 1997
REALTEK SEMICONDUCTOR CORP.			

12. Ordering Information

Table 68. Ordering Information

Part Number	Package	Status
RTL8150L	48-pin LQFP	
RTL8150LM	100-pin LQFP	
RTL8150L-LF	48-pin LQFP Lead (Pb)-Free package	
RTL8150LM-LF	100-pin LQFP Lead (Pb)-Free package	

Note: See page 3 and 4 for lead (Pb)-free package identification.

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